Electrical Properties of High-k Ta_2O_5 Gate Dielectrics on Strained Ge-rich Layers

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Abstract - Thin films of Ta_2O_5 have been deposited on strained Ge-rich layers using tantalum pentaethoxide [$Ta(OC_2H_5)_5$] by plasma enhanced chemical vapor deposition (PECVD) at low temperature. Electrical properties of the deposited samples have been measured using high frequency capacitance-voltage (C-V), conductance-voltage (G-V), and current-voltage (I-V) techniques. The fixed oxide charge density (Q_f/q) and interface state density (D_{it}) are found to be 1.04×10^{12} cm^{-2} and 3.09×10^{11} $cm^{-2}eV^{-1}$, respectively. The leakage current is observed to be dominated by Schottky emission (SE) at low electric field. The stress induced leakage current (SILC) is found to be negligible, indicating the good reliability of the deposited thin films.

I. INTRODUCTION

The continuous reduction of the gate insulator (SiO_2) layer thickness in advanced metal-oxide-semiconductor (MOS) technology leads to an excessive gate leakage current. For SiO_2 films thinner than 1.5 nm have a high direct tunneling current of the order of 1 Acm^{-2} at 2 V gate bias [1]. Therefore, a thicker film of an alternative dielectric with a higher dielectric constant than SiO_2 must be used. Such high permittivity materials should have the potential to reduce the problems of extremely high leakage current while maintaining same equivalent oxide thickness (EOT). In addition, SiO_2 is not a good diffusion barrier for gate electrode dopants, such as boron. For these reasons extensive study are recently being made on high-dielectric constant metal oxides such as Ta_2O_5, Al_2O_3, Y_2O_3, HfO_2, ZrO_2, TiO_2, Zr- and Hf-silicates. Among these, Ta_2O_5 appears to be one of the most promising high-k gate dielectrics for MOS applications because of its high dielectric constant, low leakage current, low dielectric loss, low defect density, good temperature and thermal stability [2]. For high-speed CMOS technology, Ge is a better semiconductor than Si because it offers much higher electron and hole mobility at room temperature. The electron and hole mobility of Ge is two and four times higher than those of Si, respectively. But the main problem associated with the native germanium oxide (GeO_2) which is unstable, hygroscopic, water-soluble and even volatile at high temperature (> 800°C). Due to these unreliable features, GeO_2 has hindered its use for microelectronic applications. The strain-induced modification of Ge films is found to have a significant impact on the band structure and carrier transport. This includes the splitting of degenerate valence and conduction bands, reducing of effective mass of conduction holes, and also reducing of channel scattering [3]. This increases the hole mobility in the Ge channel. A higher mobility in the channel of a p-MOSFET will improve both circuit speed and the level of integration in Ge-based complementary metal-oxide semiconductor (Ge-CMOS). In this work, ultra-thin high-k Ta_2O_5 gate dielectric films have been deposited on strained Ge-rich layers using microwave plasma enhanced chemical vapor deposition (PECVD) technique at a low temperature (150°C) for the first time. Electrical properties are reported.

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II. EXPERIMENTAL

The starting substrate was n-type Si (100) having a resistivity of 10-20 Ω-cm. Relaxed graded-$Si_{1-x}Ge_x$ buffer layers (in 10 steps, x = 0.6)' were grown by UHV compatible LPCVD. Strained Ge-rich layers were then deposited at 800°C and the film thickness was 0.15-0.2 μm. The process gases used were germane (GeH_4) and silane (SiH_4) and the working pressure was kept between 0.092-0.150 Torr. In the plasma enhanced chemical vapor deposition (PECVD) process, Ta_2O_5 films were deposited from a vaporized organometallic precursor, tantalum pentaethoxide [$Ta(OC_2H_5)_5$] which was introduced in the quartz deposition chamber of the microwave (700 W, 2.45 GHz) cavity discharge system from a bubbler kept at a temperature (150°C). The wafers were cleaned in-situ using O_2-plasma for 30s prior to the deposition of Ta_2O_5 film. The Ta_2O_5 films deposited were amorphous, since they were not exposed to a temperature higher than 650°C (crystallization point) during film formation [4]. For the electrical measurements, metal-insulator-semiconductor (MIS) capacitors were fabricated using deposited Ta_2O_5 layers on strained Ge-rich with evaporated circular Al contacts of area 1.96×10^{-3} cm^2 through a shadow mask.

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The capacitance-voltage (C-V) and current-voltage (I-V) characteristics under constant voltage (3 V) stressing were studied using the HP-4061A semiconductor test system.

III. Results and Discussions

Raman spectroscopy (Fig. 1) shows that the peaks are present at 400 cm^{-1} and 465 cm^{-1} wave number due Si-Ge and Si-Si bonds, respectively.

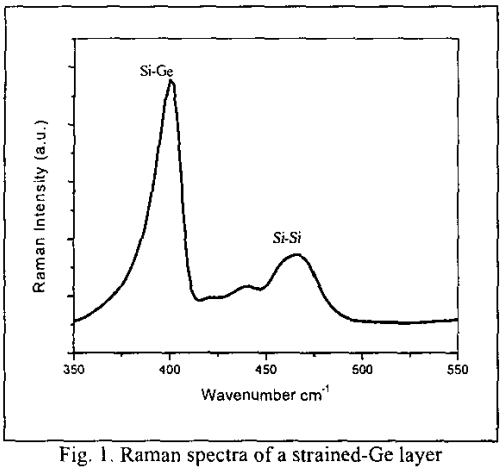

Fig. 1. Raman spectra of a strained-Ge layer

The phonon energy (and thus Raman shift) depends on the strain level in the films and can be used to determine the value of the strain. The strain in the layer is found to be 0.01688. A transmission electron micrograph (TEM)

Fig. 2. A cross-sectional transmission electron micrograph of a strained-Ge layer.

showing the complete heterostructure of the strained-Ge layer is shown in Fig. 2.

Fig.3 shows the frequency dispersion in the C-V characteristics. The capacitance in the accumulation region begins to roll-off. This is not a rare occasion for ultra-thin gate oxide layer. The degradation in the C-V characteristics may be due to the presence of the series resistance in conjunction with a leakage current, resulting in a significant reduction in the accumulation capacitance [5]. The C-V characteristics are also found to be stretched along the voltage axis. This is due to the presence of both donor and acceptor like interface traps accommodated in a portion of the bandgap [6].

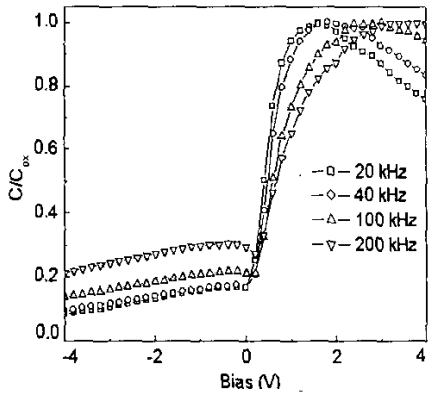

Fig. 3. Frequency dispersion in C-V characteristics of Ta_2O_5 films deposited on strained-Ge layer.

The interface trap density (D_{it}), at midgap calculated from the combination of a single frequency capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics using Hill's method [7]. Fixed oxide charge density extracted from C-V curve and interface trap density (D_{it}) extracted from both C-V and G-V curves for the strained Ge-rich sample are found to be 1.04×10^{12} cm^{-2} and 3.09×10^{11} $cm^{-2}eV,^{-1}$ respectively.

The amount of the oxide charges does not vary with the applied bias. These charges either add or subtract the electric field value from the applied electric field at the interface and appear as an offset on the voltage axis of the C-V curves. If the presence of the mobile ionic charges is negligible, the horizontal shift of the flat-band voltage (V_{FB}) is the simplest way to determine oxide trap charge density. The high frequency capacitances (1 MHz) are measured from inversion to accumulation and back to inversion as shown in the Fig. 4. The arrows show the direction of the measurements. It is interesting to note that the values of the flat-band voltages for both cases are almost same. Consequently, the flat-band voltage shift is almost negligible, indicating the presence of a negligible amount of trap charge in the dielectric.

To explain the current transport in ultra-thin dielectrics, the Schottky emission (SE), Poole-Frenkel (PF) emission, Fowler-Nordheim (FN) tunneling, direct tunneling and space charge limited current mechanisms are commonly invoked. In order to determine the leakage current conduction mechanism in the Ta_2O_5 films, the logarithm of the current is plotted against the square root of electric field as shown in Fig. 5 at room temperature.

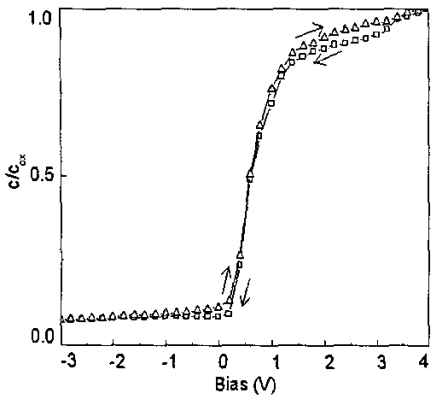

Fig. 4. High frequency C-V characteristics measured from inversion to accumulation and back to inversion.

A straight line, obtained at low electric field (< 1 MV/cm), implies the Schottky emission [8] and is given by

$$\ln\left[I_{SE}\right]=\frac{\beta}{kT}\sqrt{E}+\left[\ln\left(AT^{2}\right)-\frac{q\Phi}{kT}\right] \qquad (3)$$

where A is a constant, Φ is the Schottky barrier height, q is the electronic charge, k is the Boltzmann's constant and E is the electric field. The constant β is given by

$$\beta=\sqrt{\frac{q^{3}}{4\pi\varepsilon_{0}\varepsilon_{r}}} \qquad (4)$$

where ε_r is the dielectric constant of the insulator, ε_0 is the permittivity of the free space. The slope (M) of the straight line is proportional to β and can be employed to determine the dielectric constant of the high-k material. The value of M from Fig. 5 is found to be 2.917×10^{-3}. With this value of M, we have calculated dynamic permittivity of deposited Ta_2O_5 films as ~25.3 which is similar to the reported results [9].

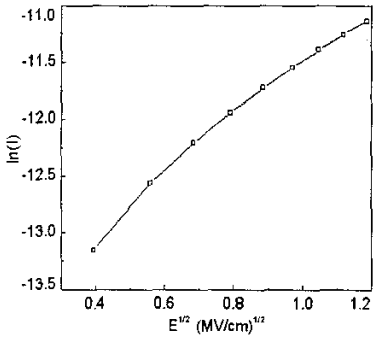

Fig. 5. The ln(I) vs. $E^{1/2}$ plot for Ta_2O_5 at room temperature.

Fig. 6 shows the current-voltage characteristics of the MOS capacitors before and after constant voltage (3 V) stressing for 50 seconds. It is observed that there is no significant stress induced leakage current (SILC), which shows the good reliability for the deposited Ta_2O_5 films.

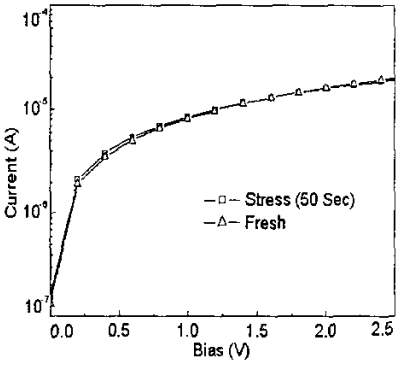

Fig. 6. I-V characteristics of Ta_2O_5 films before and after constant voltage (3 V) stressing.

IV. Conclusion

Electrical properties of high-k Ta_2O_5 dielectric films on strained Ge-rich layer have been measured using I-V, C-V and G-V techniques. The dominant conduction mechanism for the deposited films is found to be governed by Schottky emission in the low electric field region (< 1 MV/cm), which is electrode limited. The dynamic permittivity has been calculated (~25.3) and found to be similar to that of the amorphous tantalum pentoxide films, which is generally formed at low temperature. A low leakage current ($<10^{-5}$ A at 1 V gate bias) has been observed and the stress induced leakage current is found to be negligible.

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