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Multilevel resistance in ZnO nanowire memristors enabled by hydrogen annealing treatment

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In non-volatile memory technology, various attempts to overcome both technology and physical limits have led to development of neuromorphic devices like memristors. Moreover, multilevel resistance and the potential for enhanced memory capability has attracted much attention. Here, we report memristive characteristics and multilevel resistance in a hydrogen annealed ZnO nanowire device. We find that the memristive behavior including negative differential resistance arises from trapped electrons in an amorphous ZnO interfacial layer at the injection electrode that is formed following hydrogen annealing. Furthermore, we demonstrate that it is possible to control electrons trapping and detrapping by the controlled application of voltage pulses to establish a multilevel memory. These results could pave the way for multifunctional memory device technology such as the artificial neuromorphic system. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4971820]

Memristors are two-terminal devices with a metal-insulator-metal (MIM) structure that operate as electrical resistance switches and exhibit memory behavior controlled by the direction of current flow and the integrated charge. Since the first experimental demonstration by Williams and co-worker, memristors have emerged as a leading candidate for the next-generation devices, including the resistance-based memory and the neuromorphic device applications.[1–4] Memristors are particularly attractive for mobile application because of their non-volatile properties in power-off modes. In addition, the simple two-terminal MIM structure has benefited greatly from the scaling of complementary metal-oxide semiconductor (CMOS) technology.[5] Various materials such as semiconductors and insulators with switchable and sustainable resistance have been used to realize the memristive behavior; including proteins,[6] silicon (Si),[7] Ag/Si mixtures,[8] phase change materials,[9,10] transition metal dichalcogenides[11,12] and metal oxides.[13–19] Recently, one dimensional nanostructures such as nanowires (NWs) have attracted significant attention not only because of their unique physical properties in confined dimensions, but also due to the benefit for mass production and potential for high density integration circuits.[20,21] Controlling NW dimensions may also provide new insights into the memristor phenomenon, in particular the roles of bulk and surface mediated conduction.[22]

Binary metal memristors oxides such as TiO_2, NiO, and CuO have been considered as materials of great interests due to their rapid speed of resistive switching, high storage density, thermal/chemical stability and compatibility with CMOS circuits.[23–26] Among these, the properties of ZnO have attracted particular interest, due to its wide bandgap, adjustable doping and potential in application in the areas of photodiodes, piezoelectric devices and solar cells.[27–29] Many researchers have

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investigated the memristive behavior of ZnO in various structural motifs,[30–33] and from which it has been established that the drifts of oxygen ions (or oxygen vacancies) induced by surface treatment can enhance resistive switching in ZnO.[34]

Here in this work we investigate the effect of surface modification on the memristive properties of ZnO NWs and demonstrate hysteresis in current-voltage response that is dependent on the history of the device. We investigate the multilevel resistance switching properties of ZnO NWs that have been exposed to a hydrogen (H_2) annealing treatment (HAT). We show that these treated ZnO NW devices exhibit unexpected memristive characteristics, in which robust multilevel resistance properties in response to a controlled sequence of unipolar pulses are shown, in addition to a reset at the opposite polarity. We suggest that the treated surface of the ZnO NW plays an important role in the observed resistance switching behavior. These results will pave the way for, not only the application of ZnO memristors, but also potential combinations with conventional memristors for various bit memory applications.

Fig. 1(a) shows the representative scanning electron microscopy (SEM) image at low magnification of as-synthesized ZnO NWs having a high density on a Si substrate grown via the vapor-liquid-solid (VLS) method. The high magnification SEM image (inset in Fig. 1(a)) and transmission electron microscopy (TEM) image (Fig. 1(b)) clearly show that the NWs have a clean and smooth surface. The diameters of the NWs normally range from 50 to 150 nm and their lengths are from 5 to 15 μm. The presence of the alloy tip is a clear indication of the VLS growth mech-

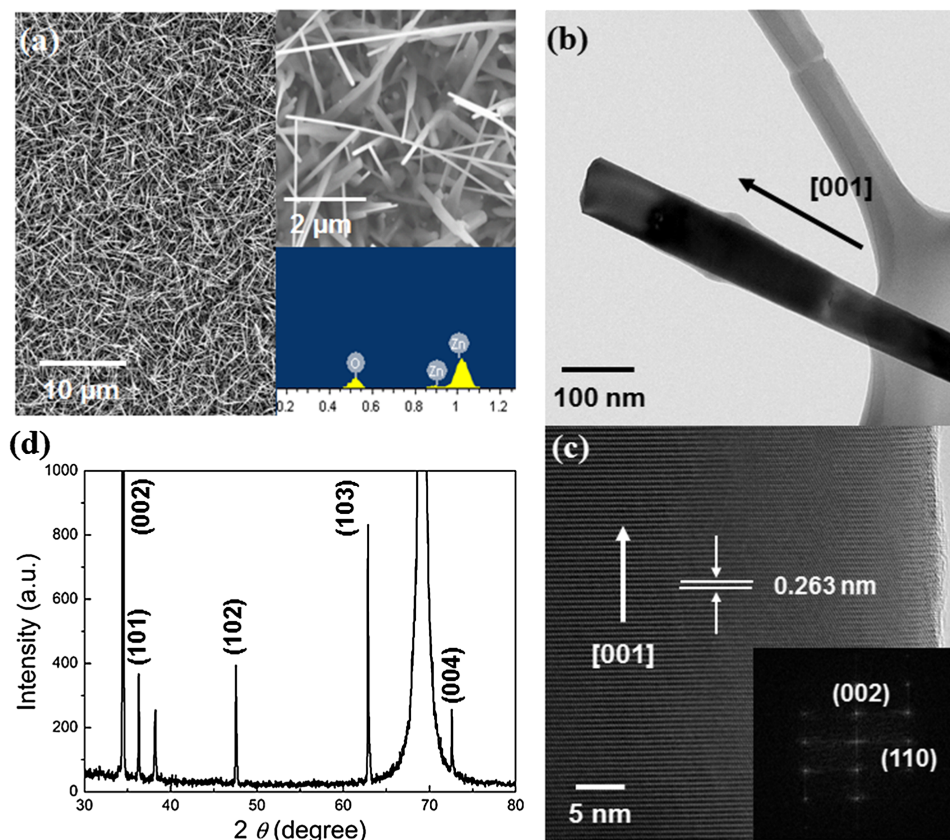

FIG. 1. Morphology of as-grown ZnO NWs. (a) SEM image of as-grown ZnO NWs on Si. Top inset indicates high magnification SEM image, and bottom inset shows EDS for characterization of chemical composition. (b, c) Representative TEM and HRTEM image of the single ZnO NW, showing the clean and smooth surface. NW is grown along the [001] direction. The lattice spacing between the (002) atomic planes is 0.263 nm. FFT of lattice-resolved image from HRTEM is shown in the inset of (c), indexed to the wurtzite structure. (d) The XRD pattern obtained from as-grown ZnO NWs on Si substrate. All the diffraction peaks are indexed to the wurtzite crystal structure, except large Si substrate and holder peaks near 38 and 69 degree.

anism (Fig. S1a of the supplementary material). High angle annular dark field (HAADF) scanning TEM image shows the perfect crystalline with well-oriented Zn and O atoms (Fig. S1b of the supplementary material). Energy dispersive X-ray spectrometry (EDS) attached to SEM is used to characterize the chemical composition (inset of Fig. 1(a)), showing the Zn/O atomic ratio of almost 1:1 (51:49), and which was confirmed by several samples.

To characterize the structure of the ZnO NWs, we performed high resolution TEM (HRTEM) analysis. No secondary growth or extra structures as well as a straight and smooth NW were observed as shown in Fig. 1(b). HRTEM image of a 100 nm diameter NW exhibits clear lattice fringes as shown in Fig. 1(c), confirming the single crystalline nature of the NWs. The observed lattice spacing between the planes is reckoned to be 0.263 nm, being consistent with the (002) planes of a wurtzite ZnO structure and the [001] growth direction down the [110] zone axis. The corresponding fast Fourier transform (FFT) pattern obtained from the HRTEM (inset in Fig. 1(c)) also demonstrates that the ZnO NW is single crystalline with the wurtzite structure. XRD patterns were recorded to examine the crystal structure of the ZnO NWs. As shown in Fig. 1(d), the observed XRD patterns of the ZnO NWs grown on the Si substrate are well matched with the wurtzite crystal structure of ZnO (CAS no. 1314-13-2) with lattice parameter a = 3.249 Å and c = 5.206 Å of a space group P63mc. In contrast to bulk ZnO, in which the (101) peak shows the strongest intensity, the (002) peak is the most dominant one in NW dimension, owing to asymmetric growth of the NWs along the c-axis.[35] The peaks near 38 and 69 degrees originate from the sample holder and Si substrate (CAS no. 7440-21-3), respectively.

Fig. 2(a) shows the schematics of a HAT ZnO NW device and SEM image. After the ZnO NW device was fabricated as described above, the sample was exposed to a thermal annealing treatment in H_2/Ar gas mixture ambient. This treatment involved an anneal at a temperature of

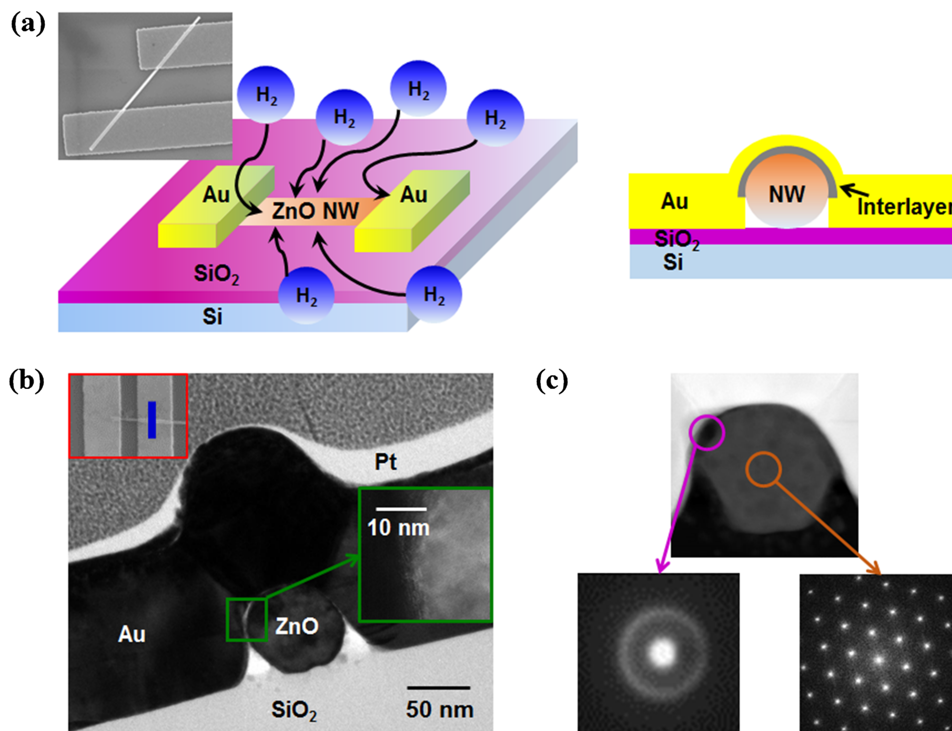

FIG. 2. HAT ZnO NW device. (a) Schematic illustration of thermal hydrogen (H_2) anneal process (HAT) to ZnO NW device. H_2 can interact with ZnO NW surface. As a result, amorphous interfacial layer between Au metal electrode and ZnO NW is formed. Inset shows the HAT ZnO NW device used to measure. (b) Cross-sectional TEM image of HAT ZnO NW device. Before FIB milling, HAT ZnO NW device is shown in top left inset (red rectangular box). The amorphous interfacial layer with ~5 nm thickness is confirmed by magnified TEM image in right inset (green square box), might react H_2 and O atoms on ZnO NW surface. (c) SAED patterns of interfacial layer (magenta open circle) and ZnO NW (orange open circle). Diffusive halo pattern from a-ZnO and regular spots pattern from ZnO NW indicate amorphous and single crystalline nature, respectively.

350°C, with simultaneous H_2 and Ar gas flow rates of 10 sccm and 190 sccm, respectively, for period of 30 min. Electrical transport measurements of the ZnO NW device with Au metal contacts have been investigated in air by Keithley 4200 SCS measurement system at room temperature.

Fig. 2(b) shows the cross-sectional TEM image of a HAT ZnO NW device. As shown in the right inset of Fig. 2(b) (green square box), an amorphous interfacial layer of ~5 nm thickness is formed. To investigate the interface between Au metal electrode and ZnO NW in detail, selective area electron diffraction (SAED) patterns measurements were performed. Fig. 2(c) reveals cross-sectional HAADF TEM image of ZnO NW used to measure and SAED patterns taken from the surface and core of ZnO NW. While we observed the diffusive halo due to scattering from an amorphous interfacial layer on the surface, SAED patterns corresponded to ZnO with wurtzite crystal structure are shown in the center of ZnO NW, confirming the single crystalline nature. This amorphous interfacial layer plays a crucial role in overall electrical transport properties in this system.

Fig. 3(a) shows the current versus voltage (*I*-*V*) characteristics of one representative HAT ZnO NW device. Positive biases correspond to electron injection from the Au contact into the ZnO NW. As the voltage increases, the current increases gradually in a non-linear manner (region I). With further bias (> ~ 2.2 V), a negative differential resistance (NDR) regime is observed (region II), which is commonly reported in memristive behaviors.[36,37] When the voltage is increased, there is a sudden current increase to the set compliance level of 1 μA (region III), indicating what is generally believed to be the formation of highly conducting filaments inside ZnO NW (i.e., soft breakdown).[38]

Fig. 3(b) shows the current response corresponding to voltage sweep from -5 V to +5 V after the reset process in the same HAT ZnO NW device shown in Fig. 3(b). Despite slightly different current level, there is no change of peak voltage (~2.2 V) where the NDR regime begins. During a first positive voltage sweep, the ZnO NW device displays the non-linear behavior previously reported

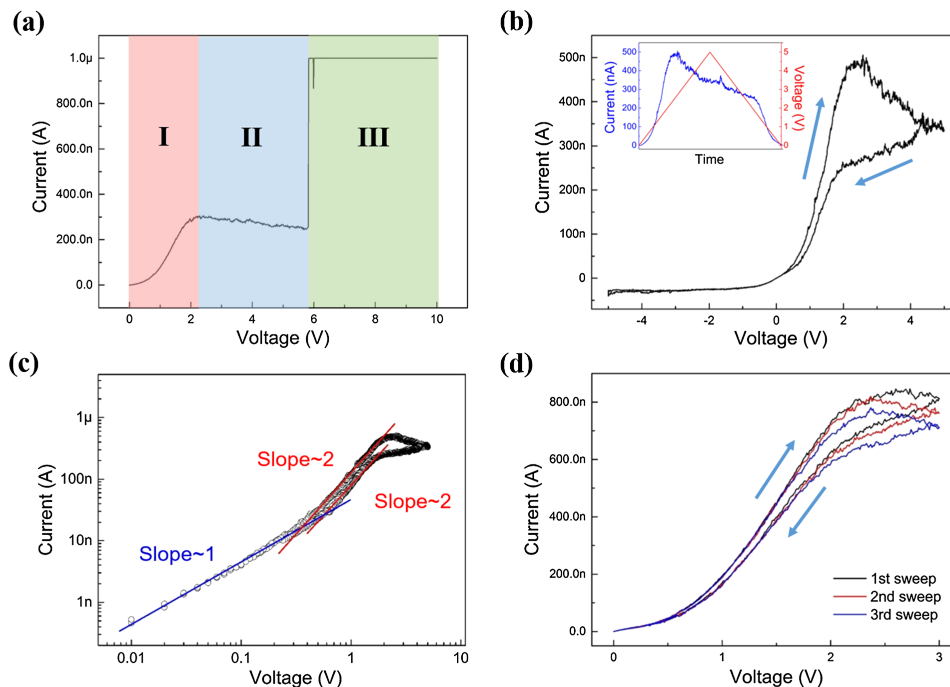

FIG. 3. *I*-*V* characteristics of HAT ZnO NW device. (a) Three regions with different transport mechanism are tracked in NW device: for I region, the non-linear characteristic is dominated due to a-ZnO interfacial layer; for II region, NDR behavior due to trap sites formed in a-ZnO layer and band bending of ZnO NW is exhibited; for III region, the change into LRS is revealed, indicating to form the conducting filaments bridge. (b) *I*-*V* curve from -5 to +5 V. Prominent NDR behavior is observed, but no current level is shown in the negative bias range. Overall features are similar with diode-like bipolar memristor. Inset indicates *I* and *V* traces for time. (c) *I*-*V* curve fitted in log-log scale using (b). *I*-*V* relationship is well agreed with the trap-controlled SCLC mechanism. (d) Consecutive *I*-*V* curves from 0 to 3 V. Current level decreases as increase of *I*-*V* sweep, indicating memristive characteristics.

followed by the NDR regime from ~2 to 5 V. When the voltage is applied in the reverse direction (5 V → 0 V), the current decreases instead of retracing the NDR branch. On the other hand, no significant current level is observed over the negative voltage range shown, consistent with diode-like behavior. Our device therefore shows characteristics of memristive diode, and we will illustrate below that the application of a negative voltage bias or pulse can be used to systemically step down the conductance recorded at positive voltages.

To investigate further the underlying conduction mechanism in region I, we rescaled the *I-V* in Fig. 3(b) into a double-logarithmic plot (Fig. 3(c)). Several conduction models, such as thermionic emission, Schottky emission, Poole-Frenkel emission, and Fowler-Nordheim quantum tunnelling, are consistent with nonlinear *I-V* curves of the type shown in Fig. 3(b).[39] The rescaled *I-V* characteristics exhibit a linear relationship between the voltage and the current ($I \propto V$) at a low voltage region (< 0.3 V), indicating that conduction is initially Ohmic. However, at higher voltages, the *I-V* relationship scales as $I \propto V^2$, which is consistent with a trap-controlled space charge limited conduction (SCLC). In the SCLC mechanism, assuming the presence of shallow traps, the *I-V* characteristics as a function of V successively follows Ohm's law and then the Mott-Gurney square law, where the latter trap-filled-limited behavior is described by

$$J = \frac{9}{8}\varepsilon_0 \varepsilon_r \mu \frac{V^2}{L^3} \tag{1}$$

where ε_0 is the vacuum permittivity of free space, ε_r is the dielectric constant of the material, μ is the free carrier mobility, L is the distance between the electrodes.[40] In region I, the assumptions of electrons injection from the contacts and the presence of shallow traps can lead to only dependence of the carrier mobility, not depend on the equilibrium carrier concentration. These traps are likely due to the presence of oxygen vacancies which are known to create states just below the conduction band edge in semiconducting oxides;[41] in this case, within the oxygen deficient amorphous ZnO (a-ZnO) interfacial layer.

The band energy diagrams, including band-bending and defect states present at Au/ZnO NW interface are shown schematically in Fig. 4. The conduction band edge in ZnO is about 2 eV below the vacuum and charge transfer to the Au contact result in upward band bending. Fig. 4(a) depicts the band diagram of the HAT ZnO NW device in the equilibrium state, and the red open circles represent trap sites in a-ZnO between the Au electrode and the ZnO NW. At low voltages the a-ZnO interfacial layer presents a minimally blocking contact and at low currents the number of injected electrons from the Au contact is much less than the available number of free electrons within the layer itself, and the *I-V* behavior is consistent with by the Ohmic conduction mechanism. However, when the voltage applied to the ZnO NW device is increased, the traps sites become energetically accessible and injection leads to the development of a space charge layer that is characterised by the well-known Mott-Gurney V^2 dependence.

The Mott-Gurney V^2 dependence strictly holds only when conduction is characterised by a well-defined mobility; the presence of traps is accounted for by the exponential term in Eq. (1). When the applied bias is increased further beyond 2 V, the device enters the NDR regime (region II). Although the precise origin of the NDR behavior and hysteresis is unknown, it is likely related to the trapping/detrapping kinetics of electrons at interfacial defect states in the a-ZnO interfacial layer[42] and which is not accounted for in Eq. (1). A steady state current is possible only when the rates of trapping and detrapping are equal. When a positive voltage is applied to the ZnO NW, it results in downward shift in the conduction and valence bands of ZnO, leading to an increased density of accessible trap sites at the a-ZnO interface region (Fig. 4(b)). The behavior we observe is consistent with a rate of trapping that is faster than that of detrapping, which accounts for the decreasing conductance and the NDR behavior of the device. In Fig. 4(c), the black and red solid line indicate the energy band structures of pristine (before the voltage sweep) and final state (after the voltage sweep), respectively. As the bias is ramped back down (5 V → 0 V), the current is reduced over that observed in the forward direction due to the faster trapping kinetic, resulting in the hysteresis loops as seen in Fig. 3(b). In this model, the number of electrons in trap sites during subsequent voltage sweeps is determined by the detrapping rate, and which is accelerated at the negative bias due to the expulsion of trapped charge

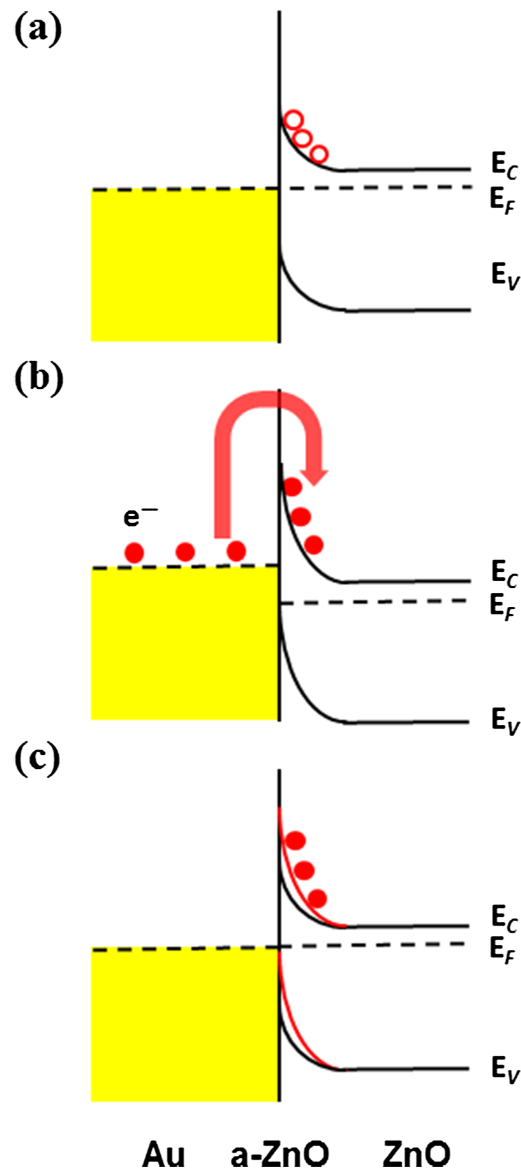

FIG. 4. Band diagram schematics of the HAT ZnO NW device before and after applying positive voltage to the ZnO NW side: (a) before voltage sweep ($V = 0$ V), (b) during positive voltage sweep to the ZnO NW ($V = 0 \sim 5$ V), and (c) after removing the bias ($V = 0$ V). The red open and solid circles represent unoccupied trap sites and electrons occupying states, respectively. In schematic (c), the red and black solid lines indicate conduction and valence band of ZnO NW with and without trapped electrons, respectively.

from the ZnO interface into the Au electrode. When the trapped electrons are completely detrapped, the energy band structure returns to the initial state.

Finally, at sufficiently high voltage (region III), where the electrons fully occupy trap sites, an abrupt surge of current is observed, similar to the formation phenomena reported in numerous resistive switching devices.[4–7,11–14,31–34,36–45] In the present system, this abrupt turn-on is likely associated with a large local concentration of oxygen vacancies or to the development of a conducting metal (Zn) filaments with the a-ZnO layer.[33]

To test the model, we have subjected HAT ZnO devices to different voltage pulse sequences. Interestingly, we find that three consecutive positive voltage sweeps decrease the current level continuously in the NDR region as shown in (Fig. S2a of the supplementary material), whereas almost constant current response is observed when the positive and negative voltage pulses are applied

alternatively (Fig. S2b of the supplementary material). Moreover, the decrease in current level becomes saturated after several voltage sweeps (Fig. S3 of the supplementary material). This behavior contrasts with typical memristors, for which it known the conductance continuously increases during consecutive positive voltage sweeps.[2,3,7,12,16,22–24,32] In that case, the increase in conductance is due to the progressive diffusion of mobile oxygen vacancies across the device under the influence of the applied field.[24] The measured *I-V* characteristics of the HAT ZnO NW device, however, exhibit decreasing conductance as the voltage sweeps are repeated, demonstrating that oxygen vacancies and their associated conduction electrons are trapped at a-ZnO interfacial layer formed between Au contact metal and ZnO NW.

Fig. 5 shows the measured current characteristics during different voltage pulse sequences. The application of consecutive positive pulses (+10 V, 4 s) following by one or more negative pulse (-5 V,

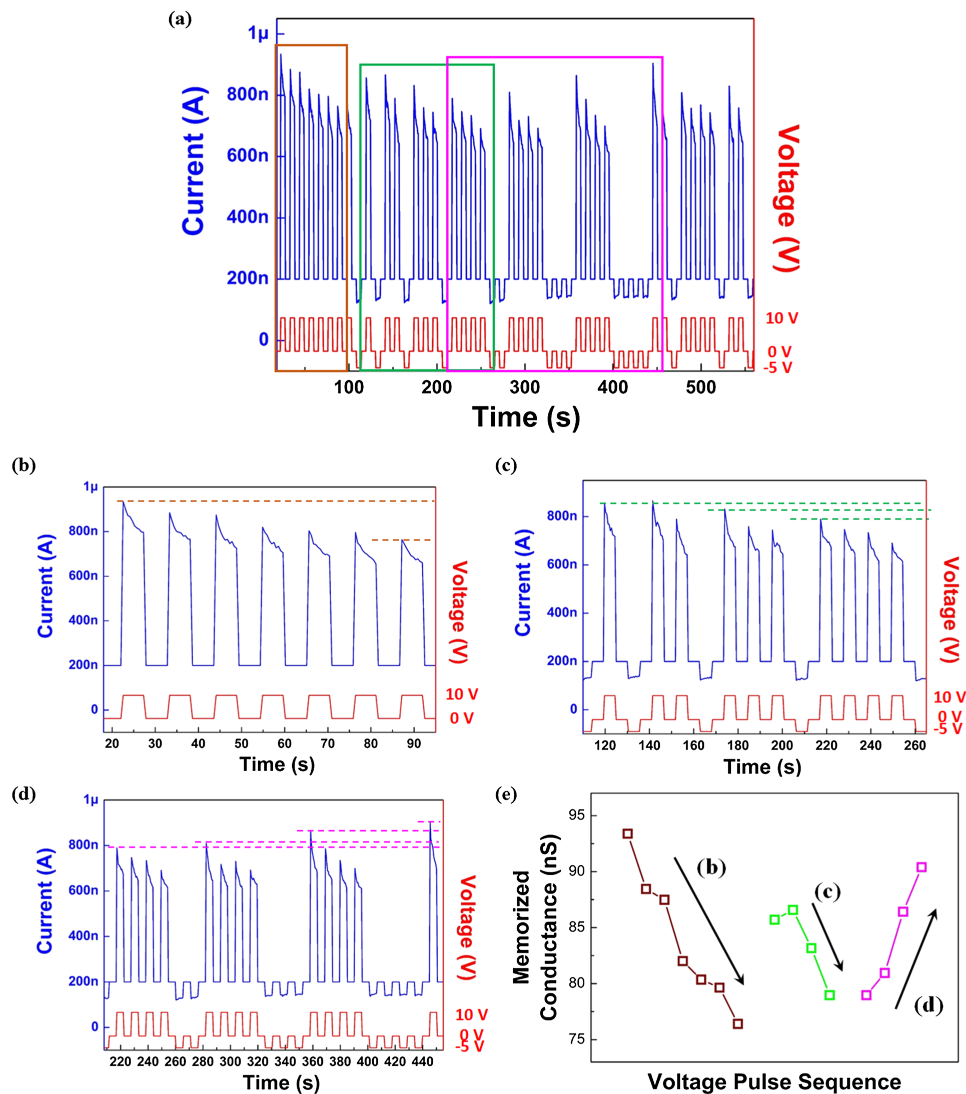

FIG. 5. Multilevel resistance characteristics of HAT ZnO NW device (a) Responded current levels corresponding to successive positive/negative voltage pulses with different numbers. (b-d) Enlarged current responses of brown (b), green (c) and magenta (d) rectangular box in (a). (b) First current peaks (brown dot line) decrease as the number of positive voltage pulses increase. (c) First current peaks (green dot line) still decrease as increasing positive voltage pulses number despite applying one negative pulse. (d) It shows that first current peaks (magenta dot line) increase due to step back to the partial detrapping when the number of negative voltage pulses are increased. (e) Continuous memorized conductance downward or upward changes after applying continuous different pulse sequences.

4 s) was studied. The corresponding conductance decreases steadily at first as shown in Fig. 5(a), and then settles into a steady state value. This behavior is attributed to an initial imbalance between the rates of trapping and detrapping, the former initially dominates leading to the reduction in the current response during consecutive pulses, consistent with Fig. 3(d). Ultimately, for any given repetition sequence the current become self-limiting and the rates of trapping and detrapping balance out to yield a state current response. Fig. 5(b) exhibits the current responses as several consecutive positive pulses are applied, consistent with the presence of trapped conduction electrons in the a-ZnO interfacial layer (enlarged brown rectangular box in Fig. 5(a)).

The application of a negative bias -5 V causes the trapped electrons to be extracted to Au contact metal, such that the subsequent application of a positive pulse results in an increased current response. This is clearly seen in Fig. 5(c) (enlarged green rectangular box in Fig. 5(a)), which is a close up of a pulse sequence from Fig. 5(a). Increasing the number of negative pulses enhances detrapping and results in an increased current response during subsequent positive pulses. Fig. 5(d) (enlarged magenta rectangular box in Fig. 5(a)) demonstrates the forward response following 1-4 negative pulses. To clearly record the multilevel resistance (or conductance), we summarize in Fig. 5(e) the gradual memorized conductance (MC) behavior following different voltage pulse sequences. The values and tendencies of MC depend on the polarity of the applied consecutive voltage pulses. When only positive voltage pulses are applied, the MC continuously decreases with increased numbers of positive pulses (curve b). The incorporation of a single negative pulse still allows the MC to decrease following subsequent positive voltage pulses (curve c). However, if the number of intervening negative pulses is gradually increases, the MC increases (curve d). The combined response to positive and negative pulses allows this device to not only enable the partial suppression and restoration of the conductance, but also to function as a unique multilevel memory device.

In summary, we demonstrated that the a-ZnO interfacial layer created following the HAT process plays a critical role in the memristive characteristics of ZnO NWs, and the ability to define multilevel resistance states. Both pronounced NDR behavior and memristive hysteresis of *I-V* curves are explained by the trapped electrons at the a-ZnO interfacial trap states. The observed multilevel resistance states depend on the direction and the number of positive/negative voltage pulses and can be controlled due to the partial detrapping (trapping) electrons, leading to the conductance restoration (suppression). Looking to the future, we expect to open the opportunity to build up crossbar structures combined with conventional memristors for multi-bit memristors, and that HAT ZnO NW may pave the way for the multifunctional memory device technology such as the artificial neuromorphic system.

SUPPLEMENTARY MATERIAL

See supplementary material for the complete electronic structure of the TEM data, current level via successive voltage pulse applications, and time and cycle dependence of the device current.

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