LEABHARLANN CHOLÁISTE NA TRÍONÓIDE, BAILE ÁTHA CLIATH | TRINITY COLLEGE LIBRARY DUBLIN
Ollscoil Átha Cliath | The University of Dublin

Terms and Conditions of Use of Digitised Theses from Trinity College Library Dublin

Copyright statement

All material supplied by Trinity College Library is protected by copyright (under the Copyright and Related Rights Act, 2000 as amended) and other relevant Intellectual Property Rights. By accessing and using a Digitised Thesis from Trinity College Library you acknowledge that all Intellectual Property Rights in any Works supplied are the sole and exclusive property of the copyright and/or other IPR holder. Specific copyright holders may not be explicitly identified. Use of materials from other sources within a thesis should not be construed as a claim over them.

A non-exclusive, non-transferable licence is hereby granted to those using or reproducing, in whole or in part, the material for valid purposes, providing the copyright owners are acknowledged using the normal conventions. Where specific permission to use material is required, this is identified and such permission must be sought from the copyright holder or agency cited.

Liability statement

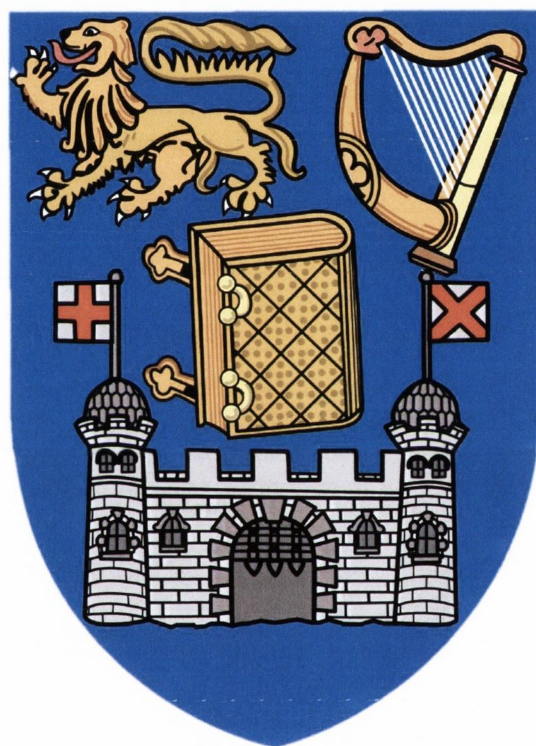
By using a Digitised Thesis, I accept that Trinity College Dublin bears no legal responsibility for the accuracy, legality or comprehensiveness of materials contained within the thesis, and that Trinity College Dublin accepts no liability for indirect, consequential, or incidental, damages or losses arising from use of the thesis for whatever reason. Information located in a thesis may be subject to specific use constraints, details of which may not be explicitly described. It is the responsibility of potential and actual users to be aware of such constraints and to abide by them. By making use of material from a digitised thesis, you accept these copyright and disclaimer provisions. Where it is brought to the attention of Trinity College Library that there may be a breach of copyright or other restraint, it is the policy to withdraw or take down access to a thesis while the issue is being resolved.

Access Agreement

By using a Digitised Thesis from Trinity College Library you are bound by the following Terms & Conditions. Please read them carefully.

I have read and I understand the following statement: All material supplied via a Digitised Thesis from Trinity College Library is protected by copyright and other intellectual property rights, and duplication or sale of all or part of any of a thesis is not permitted, except that material may be duplicated by you for your research use or for educational purposes in electronic or print form providing the copyright owners are acknowledged using the normal conventions. You must obtain permission for any other use. Electronic or print copies may not be offered, whether for sale or otherwise to anyone. This copy has been supplied on the understanding that it is copyright material and that no quotation from the thesis may be published without proper acknowledgement.

An Introduction to Surface Energy Driven Growth Nanoparticle Synthesis & The Development of Single TiO_2 Nanowire Devices as Memristors



A thesis submitted to the University of Dublin, Trinity College,

in application for the degree of Doctor of Philosophy

School of Chemistry

2015

Curtis O'Kelly

Under the Supervision of Prof. John J. Boland

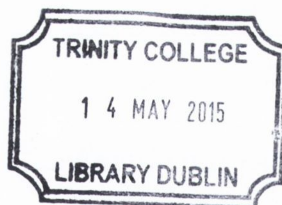
Declaration

I declare that this work has not previously been submitted as an exercise for a degree at this, or any other University, and that unless otherwise stated, is my own work.

I agree to deposit this thesis in the University's open access institutional repository or allow the library to do so on my behalf, subject to Irish Copyright Legislation and Trinity College Library conditions of use and acknowledgement.

15/1/2015
Date

Curtis O'Kelly



Thesis 10493

Acknowledgements

I wish to acknowledge my supervisor Professor John Boland for his help and guidance throughout the course of my Ph.D. I would also like to sincerely thank John for giving me the opportunity and challenge of perusing a PhD. Under his tutelage I have realised many personal life goals and gained invaluable experience.

I would also like to acknowledge Dr. Soon Jung Jung (Mrs. Lutz) for her help during the start of my research. She was instrumental in my training and developing my research ability. A special thanks to Dr. Jessamyn Fairfield for her help and input since she joined the group. Her input at the start and throughout a recent paper was invaluable.

The help of my peers is greatly appreciated including Alan Bell, Eoin McCarthy, David McCloskey, Allen Bellew, Hugo Nolan, Shaun Mills and Hugh Manning. The help and support of the AML staff is also appreciated.

On a personal note I would like to thank my fiancée Katarzyna who has been supportive of my research work despite the long hours. My work and successes would not have been possible without you. I am eternally grateful for all the help my parents gave me throughout my time in Trinity College.

And to my daughter Sonia who makes everyday the greatest day – this work is for you.

Abstract

In this thesis aspects of a novel nanoparticle synthesis method and a unique multi-level resistance switching memory device are introduced. The dichotomy of the two programmes is addressed and a rationale for the transition between the projects is presented based on practical instrumental and material limitations. The nanoparticle synthesis method referred to as the surface energy driven growth (SEDG) is introduced and its physical principles explained. The SEDG method is especially suited for producing single-crystal metallic nanowires that cannot be produced via the similar vapour-solid-liquid method. The method has various applications in new nanomaterial discovery, binary alloy phase diagram dynamics and real time crystal growth kinetics.

The development and realisation of a single TiO_2 nanowire based multi-level memory device is also presented. TiO_2 has commanded much interest as a resistance switching material due to its intrinsic self-doping ability under applied bias voltage. When electrically stressed, oxygen molecules are liberated from the lattice leaving n-type oxygen vacancies behind. These vacancies are mobile and may drift in response to an applied voltage which offers a degree of control on their distribution throughout the material. In this work a single TiO_2 nanowire contacted with Au electrodes is developed into a multi-level resistance device through electroforming and pulsed voltage application. The device can be tuned to display either six individual conductance states or a continuum of conductance levels defined by the user. Finally, UV light which is also known to produce oxygen vacancies in TiO_2 is synchronously pulsed with voltage bias to produce an emergent neuromorphic learning response not previously reported for dissimilar pulse stimuli. The response can be likened to that of associative learning – a phenomena predominantly observed in biological neural systems.

Summary

To advance the field of nanoscience it is necessary to develop novel synthesis methods that can increase the catalogue of unique nanoparticles. It is not sufficient to simply produce new nanoparticles however. They must be incorporated into functioning devices before their inherent properties can be used to the benefit of wider society. The scope of this thesis captures both synthesis and nanoparticle device topics. There are two main topics covered in this thesis including single crystal nanoparticle synthesis and single nanowire semiconducting device characterisation as unique memory resistors (memristors).

In Chapter 3 a relatively new nanoparticle synthesis method is introduced in the wider context of nanoparticle synthesis. A general design flow is also presented to enable the wider community begin to synthesize particles with this method. The surface energy driven growth (SEDG) method is a stand alone synthesis technique that has some similarities to the various stages of vapour liquid solid (VLS) growth. The SEDG method exploits the inherent difference in surface energy of coupled binary alloys that display a deep eutectic point. The eutectic point in the binary alloy phase diagram represents a fully miscible liquidus alloy composed to both alloy components. By their nature these eutectic points are often far below the melting point of the pure components individually which means the SEDG method can be realised at moderately high temperatures. After forming the liquidus binary alloy a spontaneous complex enrichment process manifests to ultimately produce a single crystal of the high surface energy alloy component. The SEDG method also offers new opportunities to study nucleation phenomena in real time.

In Chapter 4 the SEDG method is applied to the Fe-Nd binary alloy system. As predicted by the SEDG design flow introduced in Chapter 3, single crystal Fe nanocubes are produced. We demonstrate that the size of the nanocubes can be controlled by the initial film thickness of Fe. TEM and selected area electron diffraction confirmed the crystalline nature of cubes. Real time cube growth is observed during growth using SEM hot stage annealing. In less than 120 seconds the cube approaches 300 nm in size – an eight fold increase in size from that of its initial observed size. High resolution magnetic force microscopy (MFM) was carried out on single cubes to probe their magnetic properties. The MFM data revealed the presence of two distinct magnetic domain patterns including 'bow-tie' and 'windmill' patterns. The patterns are not induced by grain boundaries in the cubes but may be linked to the dimensions of the cubes.

Fabrication and characterisation of individual TiO_2 nanowire devices are the focus of Chapters 5 and 6. Dilute solutions of TiO_2 nanowires are spray deposited before being electrically contacted using e-beam lithography (EBL). The choice of contact metal was found to affect the ability of the device to display a dynamic evolutionary response. Gold electrodes proved the most successful at producing consistent device characteristics with Ti electrodes suffering from electro-induced deformation. Once the devices are formed, it is possible to define an arbitrary number of conductance states in the device via the voltage pulse amplitude and width. The continuum resistance of the device is leveraged to demonstrate six individual conductance states in a single nanowire device. The six conductance states in the wire may be used as six level memory device which could be developed into a new six state computational logic to replace current two state binary logic used in computers today.

The device behaviour is based on the dynamic introduction of intrinsic defects into the device during forming. These defects are thought to be oxygen vacancies which are reported to act as n-type dopants in TiO_2. When generated at the metal interface, these defects dynamically dope and alter the band structure of the metal-wire interface which displays characteristics of a Schottky barrier. The voltage pulses alter the defect concentration at the interface which in turn sets the ability of the barrier to conduct current.

In Chapter 6 the single nanowire devices are exposed to UV laser stimulus as a mechanism for developing additional oxygen vacancy defects within the wire. Applying both UV laser light and voltage during forming is shown to bring the device to saturation current faster than holding voltage alone on the device. The dynamic response of UV stimulus is catalogued. When the device is brought to a steady state using voltage the laser stimulus is used to generate an excess photocurrent in the device. The magnitude and length of time this excess current persists is shown to be related to applied bias with higher voltages causing the current to decay faster. We also note a saturation of photocurrent at high voltages.

Finally, in what is perhaps the most profound result in this thesis we demonstrate associative memory and learning in the TiO_2 nanowire. The nanowire essentially behaves similarly to a biological neuron in its response to correlated stimuli. UV laser pulse stimulus is coupled with voltage pulse stimulus to produce this memory effect which produces a greater current response from the device than the sum of each stimuli applied individually. Associative memory is demonstrated when a subsequent voltage only stimulus produces a high current response from the device.

List of Publications

Curtis O'Kelly, Jessamyn A. Fairfield, and John J. Boland. *A Single Nanoscale Junction with Programmable Multilevel Memory,* ACS Nano, 2014. 8(11): p. 11724-11729.

O'Regan, C, Biswas, S, O'Kelly, C, Jung, SJ, Boland, JJ, Petkov, N, Holmes, JD, *Engineering the Growth of Germanium Nanowires by Tuning the Supersaturation of Au/Ge Binary Alloy Catalysts*, CHEMISTRY OF MATERIALS, 25, (15), 2013, p3096-3104

P.N. Nirmalraj, A.P. Bell , A.T. Bellew, J.A. Fairfield, E.K. McCarthy , C. O Kelly, L/F.C Pereira, S. Sorel , J.N. Coleman, M.S. Ferreira and J.J. Boland, "Manipulating Connectivity and Conductivity in Metallic Nanowire " , Nano Lett, 12, (11), 2012, p5966 – 5971

Curtis O'Kelly, Soon Jung Jung, Alan P. Bell and John J. Boland, "Single Crystal Iron Nanocube Synthesis via the Surface Energy Driven Growth Method" , NANOTECHNOLOGY, 23, (43), 2012, p1 - 6

Contents

Declaration i

Acknowledgements ii

Abstract iii

Summary iv

List of Publications v

Chapter 1 Introduction

1.1 Historical Context 1

1.2 Size Dependent Phenomena – Why Nano? 2

1.3 Semiconductor Materials 3

1.4 Metal-Semiconductor Contacts 7

1.5 Interaction of Light with Semiconductors 11

1.6 Microelectronic Nanotechnology: Smaller, Cheaper, Faster 13

1.7 Scope & Summary 18

1.8 References 19

Chapter 2 Methods

2.1 Introduction 23

2.2 Electron Microscopy 23

2.3 Transmission Electron Microscopy 26
2.4 Lithography 29
2.4.1 Electron-Beam Lithography 29
2.4.2 Ion-Beam Lithography 32
2.4.3 FIB Lamella Preparation 34
2.5 Material Processing 35
2.5.1 Physical Vapour Deposition 35
2.5.2 Sputter Deposition 36
2.5.3 Spray Deposition 38
2.6 References 39

Chapter 3 Surface Energy Driven Growth: A General Introduction

3.1 Introduction 40
3.1.1 Nanoparticles 41
3.1.2 Colloidal Nanoparticle Synthesis 42
3.1.3 Vapour-Liquid-Solid Growth 45
3.2 Features of the Surface Energy Growth Method 47
3.3 Generalisation of SEDG Method 48
3.4 Thin Film Stability 51
3.5 Agglomeration & Crystal Nucleation 56
3.6 Real Time Nucleation & Metastable Crystal Nucleus 59
3.7 Summary and Outlook of SEDG 61
3.8 SEDG Continuity 62
3.9 References 62

Chapter 4 Single Crystal Fe Nanocubes Synthesised via the SEDG Method

4.1 Introduction 65

4.2 Experimental Details 67

4.3 Fe Nanocubes Grown with SEDG by Design 68

4.3.1 Design Flow 68

4.3.2 Fe Nanocube Growth 69

4.4 Real Time Nanocube Growth 72

4.5 Cube Morphology and Size 73

4.6 Physical Properties 76

4.7 Conclusions and Outlook 81

4.8 References 83

Chapter 5 Single TiO_2 Nanowires as a Unipolar Memristor Device

5.1 Introduction 85

5.1.1 Random Access Memories 86

5.1.2 Resistance Switching RAM 87

5.1.3 Memristors 92

5.2 Device Fabrication 95

5.2.1 Sample Preparation 95

5.2.2 Hand Spray & Contacting 97

5.2.3 Electrical Characterisation 97

5.3 Results 98

5.3.1 Basic Electrical Behaviour 98

5.3.2 Effect of Electrode Metals 100

5.3.3 Dynamic Current Response 102

5.3.4 Multi-level Memory Device 104

5.4 Memristance Mechanism 107

5.5 Conclusions & Future work 111

5.6 References 113

Chapter 6 Neural Learning and Memory Behaviour at a Single Nanojunction in Response to Heterogeneous Stimuli

6.1 Introduction 115
6.2 Experimental 122
6.3 Results and Discussion 123
6.3.1 Interaction of TiO_2 with Static UV Light for Assisted Forming 123
6.3.2 Dynamic Interaction of Optical Stimulus with Voltage Stimulus 126
6.3.3 Correlated Voltage and Light Pulse Stimuli 132
6.4 Summary and Outlook 137
6.5 References 138

Chapter 1

Introduction

1.1 Historical Context

The field of nanoscience began to rise to prominence in the last half of the 20th century. The roots of the concept may be attributed to Richard Feynman who, in 1959 attempted to rally his peers in a talk about the scaling effects of different physical phenomena [1]. Despite his talk the field of nanoscience did not gather much interest until the 1980s, when several key enabling tools reached maturity. This toolset included the scanning tunnelling microscope (STM), transmission electron microscopy (TEM) and the atomic force microscope (AFM). STM and AFM were introduced in 1981 and 1986 respectively with early commercial TEM available from 1940 [2]. Together these tools succeeded in overcoming the optical diffraction limits to reveal for the first time rows of atomic planes, crystalline defects and even individual atoms themselves [3].

Nanosized objected could now be directly visualised. This enabled researchers to gather precise detailed information about their experiments that would in turn allow them to produce viable devices and demonstrate novel phenomena. Thus the field of nanoscience was born. The field was embraced by governments and funding bodies around the world, most notably with the $500 million National Nanotechnology Initiative (NNI) president Bill Clinton announced at the turn of the century [4]. Since then nanoscience has grown in popularity across all scientific disciplines. The term nanotechnology was coined originally by Norio Taniguchi and popularised by Eric Drexler in 1981 [5]. It describes any technology or device whose operation or functionality is dependent on nanosized objects. Today nanotechnology is an incorporated element of many aspects of modern living including smart TVs, laptops, mobile phones and tablets. Beyond electronics, nanotechnology is becoming increasingly important in the field of medical diagnostics and the development of new devices for lab on chip applications in healthcare as well as novel methods for drug delivery and the treatment of disease. Overall, the societal impact that the development of nanoscience has had cannot be understated. Further still, the field is set to flourish over the rest of the 21st century as there is a growing convergence

that will see micro and nanoscale electronics become increasingly incorporated in medical, energy and environmental applications.

1.2 Size Dependent Phenomena – Why Nano?

Nanosize particles display many unique properties when compared to bulk objects made of the same material. Their inherent low dimensionality has a dramatic effect on the electronic structure of the particle as the electrons are confined by the critical dimensions of the particle. This confinement produces unique distribution of energy states for so called 0D quantum dots, 1D wires and 2D atomic layer nanomaterials. Shown in Figure 1.1, is the relevant density of states for each dimensionality compared to that of the bulk. Particles consisting of tens (up to thousands) of atoms are considered pseudo-zero dimensional. Their electronic structure reflects that of a molecule with discrete energy levels but with energy level spacings determined by the size of the quantum dot. The size dependent electronic structure of QDs gives them unique optical properties while displaying many solid-like properties of metals, semiconductors and insulators. This effect is best captured by the CdS semiconductor QDs whose inherent colour is solely due to their size which affects the electronic structure of the particle and how it interacts with light [6].

For the case of 1D nanowires, the electrons movement is constrained in two axes (x-y) but has unbounded movement along the length of the wire (z-axis). This translates to a continuum of states along the wire length with highly quantized states in the two directions. Physically, the wires are defined by their high aspect ratio (length/width) which is typically upwards of ~ 1000. 1D materials are attractive for many electronic devices due their channel-like character and the ability to modulate the conductivity along the length of the wire. This is achieved either through a back gate electrode or surface adsorption onto the wire which disrupts and scatters carrier movement [7]. Other applications include lasers [8], sensing and drug delivery [9, 10]. In 2D materials, the movement of carriers is free in two dimensions and confined in the other. 2D materials have become the subject of intense research interest over the last decade since the discovery of atomically thin sheets of carbon known as graphene [11]. Hailed as a wonder material with high strength, graphene also has exceptional electrical properties and ultra-high electron mobility [12]. Since graphene's discovery, the breadth of 2D material systems has increased with MoS_2 and GaS the topic of much research at the moment [13]. The promise of 2D materials stems from their 'all surface' characteristics. This leads to unique carrier transport

characteristics, enhanced sensitivity and some anomalous properties only observed in 2D materials such the quantum hall effect.

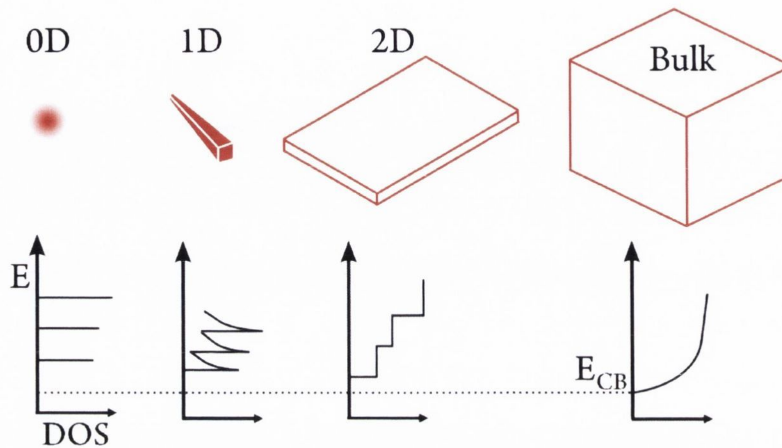


Figure 1.1 Electronic density of states for each dimensionality of semiconductor nanoparticle compared to that of bulk material where E_{CB} is the conduction band.

1.3 Semiconductor Materials

Semiconductor materials technology is the cornerstone of the microelectronic industry, as evidenced by its role in field effect transistor technology and the original bipolar device technology first introduced 1948 [14]. A semiconducting material has electronic conduction properties between that of a conductor (metal) and an insulator (SiO_2). A semiconductor is unique in its ability to offer precise control over its levels of conduction in relation to conductors and insulators. This stems from the ability to control the electronic band structure via doping - the deliberate introduction of extrinsic atoms into the semiconductor material. It is well established that solid crystal materials form a distinct energy band structure which is generated from the combination of individual atomic orbitals of each atom within the solid lattice [15]. In semiconducting materials, an energy gap exists between the highest energy valence electrons that contribute to the solid bonding from the energy band with the lowest energy conduction comprised of anti-bonding energy levels. The separation is called the bandgap of the semiconductor and is one of the most important properties of a semiconductor. The presence of a bandgap prohibits electrons from moving freely through the lattice under lowest temperature conditions.

Above zero Kelvin there remain a small but non-negligible number of electrons with sufficient energy to traverse the energy gap into the unoccupied conduction band, creating the corresponding number of electron holes in the valence band. The number of electrons in the conduction band can be determined statistically via the Fermi-Dirac distribution with the systems thermal energy (kT) greatly affecting the free electron distribution. The concentration of carriers may be estimated using the concept of the Fermi energy level and its relative position in the energy gap. Insulating materials also possess an energy gap that is relatively larger than semiconductors and as a result there are an insignificant number of electrons in the conduction band at room temperature. Figure 1.2 captures the differences between the three types of energy band structures. Some bandgap energy values for common semiconductors include Si – 1.12 eV, GaAs – 1.52 eV with insulator band gaps typically larger than 4 eV, e.g. SiO_2 – 9 eV.
Conduction is defined as the movement of electrons in a material that gives rise to current, depends heavily on the band structure of the material. In the case of metals, the Fermi energy level lies within the valence band itself or the overlapping of the valence and conduction bands. Thus the electrons at the Fermi energy are free to respond to an applied field and gain energy by transitioning into any number of nearby empty states. The energy gap in semiconductors and insulators separates the valence band from the conduction band. Since the valence band is completely full of electrons, electrons cannot move and contribute to conduction as there are no unoccupied states for them to move into. Only electrons promoted to the conduction band by thermal energy or another external stimulus, such as light, can contribute to the measured current in the material. The Fermi energy level is a very important reference energy used to illustrate the population distribution of electrons (and holes) in a material. It is defined at thermal equilibrium as the energy level of the state whose occupancy by an electron is equal to one half. Its position can be used to estimate the concentration of carriers in the conduction band or valence band and also how the concentration changes as extrinsic atoms known as dopants are introduced to the lattice of the semiconductor material.
There are two types of dopant atoms that may be introduced into a semiconductor. They are characterised by the number of valence electrons they contain relative to the host semiconductor. Donor atoms including group V materials such as As and P are termed n-type dopants because when they are incorporated into the Si crystal lattice, they have one loosely bound electron that is easily removed from its parent atom, allowing it to move freely about the lattice. Physically an n-type atom introduces an energy level in the bandgap slightly below the conduction band of the bulk material. The energy difference between the conduction band and the dopant impurity energy level is small, 0.054 and 0.046 eV respectively for As and P

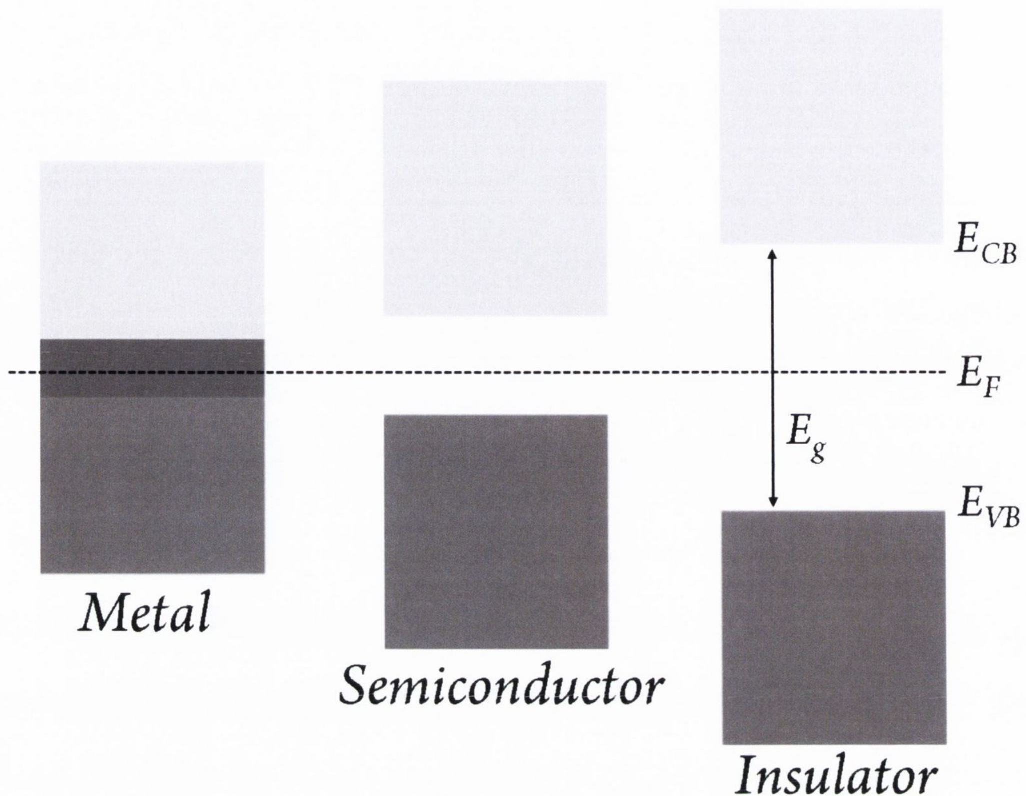


Figure 1.2 Comparison of the band structure of metal, semiconductor and insulator materials. The presence of a bandgap E_g differentiates semiconductors and insulators from metals. E_{CB}, E_{VB} and E_F are defined as the conduction band, valence band and Fermi level.

dopants in Si. Thermal energy is sufficient to ionise electrons from dopant atoms to the conduction band leaving a positive ion remaining in the lattice (E_{kT} = 0.04 eV at 300 K).

The second extrinsic dopant is an acceptor or p-type atom. P-type dopant atoms consist of group III materials such as Ga and B. When incorporated into a semiconductor lattice, the atom captures an electron from the semiconductor bulk to satisfy its own valence bonding requirement. This electron is supplied by the valence band and its absence is often called an electron hole. The hole has many inherent properties similar to that of an electron but with opposite charge and distinct mobility. P-type dopants set up energy levels band in the bandgap above the valence band, where again the energy required to ionise a valence band electron to these impurity states is on the order of thermal energy. In the absence of doping the number of electrons and holes is identical; n-type doping provides additional electrons, whereas p-type doping provide additional holes. The free electrons and holes that are the charge carriers in semiconductors are characterised by various parameters describing how they behave in the

lattice material. The drift velocity v_d or speed of carriers in a material under low field is proportional to the strength of the electric field E through the mobility μ:

$$v_d = \mu E \tag{1.1}$$

Mobility can be defined in relation to mean free time by:

$$\mu = \frac{q\tau_m}{m^*} = {q\lambda_m}\Big/{\sqrt{3kTm^*}} \tag{1.2}$$

Where τ_m is the mean free time between collisions, m^* is the effective mass of the carrier, q is the elementary charge of an electron and λ_m is the mean free path defined as:

$$\lambda_m = v_{th}\tau_m \tag{1.3}$$

Thermal velocity v_{th} is given by:

$$v_{th} = \sqrt{{3kT}/{m^*}} \tag{1.4}$$

These elementary equations are used to determine two important parameters: the drift velocity and mobility of the carrier. GaAs doped with 10^{14} dopants at 300 K has an electron and hole mobility of 1×10^4 and 3×10^2 $cm^2/V\text{-}s$ respectively.

The total drift current under an applied field is due to both electrons and holes. The current density of mobile carriers is given by the relation:

$$J = \sigma E = \frac{I}{A} \tag{1.5}$$

Where I is the measured current, A is the cross sectional area and the conductivity σ is,

$$\sigma = q(\mu_n n + \mu_p p) \tag{1.6}$$

With n and p the concentration of electron and hole carriers respectively. However if n is much greater than p, which is the case for n-type semiconductors, the conductivity can be expressed as:

$$\sigma = q\mu_n n \tag{1.7}$$

Typically, the conductivity and resistivity ($\rho=1/\sigma$) are measured and reported for new material systems. These equations will be relevant in chapters 5 and 6 where carrier mobility and current density of semiconductor like devices will be discussed.

1.4 Metal-Semiconductor Contacts

Every semiconducting material must be contacted with a metal for integration into a working circuit. Connecting a metal to a semiconductor is a simple prospect but the contact between the two may display some undesired effects which detract from the function of the overall device. To form an electrical contact between the semiconductor and metal they must be brought into physical contact with each other. If current is allowed to flow between the two, electrons will move into the metal from the semiconductor conduction band (provided the Fermi energy is higher relative to the metal) until thermal equilibrium is obtained. At thermal equilibrium the Fermi level should be uniform throughout the contact and into the bulk materials on either side. For this to be the case the energy of the semiconductor bands must shift and bend relative to the vacuum energy level. This process is described in Figure 1.3 and includes many relevant parameters such as the metal work function $q\phi_m$ which is the difference in energy between the vacuum level and the Fermi level, the semiconductor work function $q(\chi+\phi_n)$ with $q\chi$ defined as the electron affinity measured from the bottom of the semiconductor conduction band to the vacuum level and $q\phi_n$ is the difference between the conduction band energy and the Fermi level.

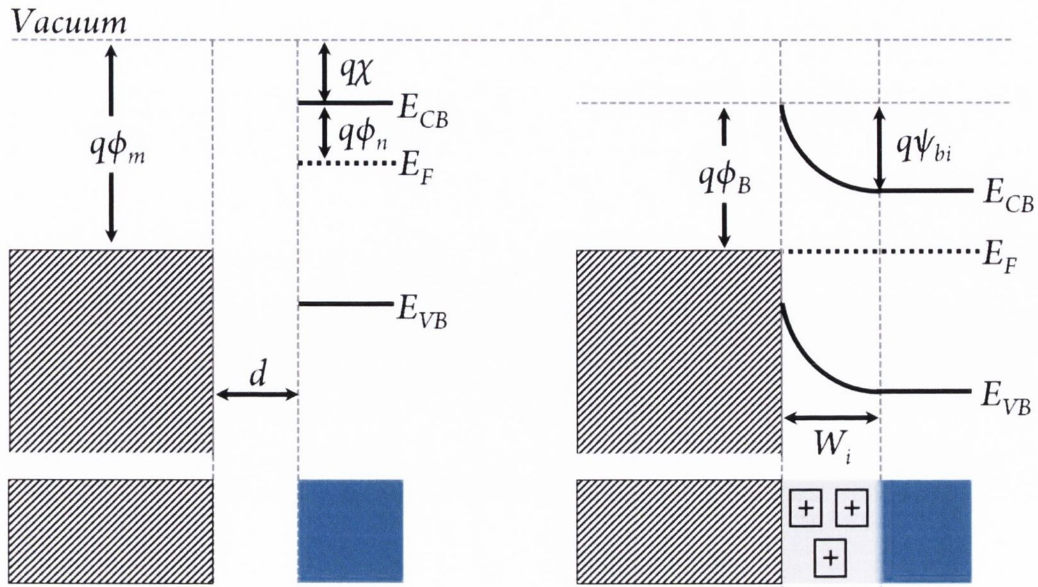


Figure 1.3 Energy band diagram of a metal (black) semiconductor (blue) contact formation for an n-type semiconductor. As the distance d between the two materials approaches zero electrons in the conduction band of the semiconductor move into the metal until thermal equilibrium is established and the Fermi level is continuous through the contact. Band bending occurs in the semiconductor as a large negative charge is built up on the metal for which an equal but opposite positive charge must exist in the depletion region of the semiconductor. The depletion layer has a corresponding width W_i and built in voltage $q\psi_{bi}$.

The final important parameter is the ideal barrier height $q\phi_B$ which is equal to $q(\phi_m - \chi)$. The ideal barrier height is rarely realised in a metal-semiconductor contact however and is typically less than the value calculated by the previous equation. The deviation from ideal behaviour is due to Fermi level pinning by interface states between the metal and the semiconductor contact. Electrons from the metal occupy interface states which pin the Fermi level prior to full contact formation. The pinning alters the calculated barrier height of the contact, of particular importance as it represents a potential energy barrier electrons must overcome to be injected into the metal from the semiconductor.

Electrons captured by the metal during contact formation leave ionised dopants at the interface region which generate the depletion layer in the semiconductor at the interface region. It is these positively ionised dopants and the negative charge at the metal interface that is responsible for the band bending. The high electric field produced via the separation of charge has an intrinsic built in voltage $q\psi_{bi}$. The contact type shown in Figure 1.3 is described as a

Schottky barrier (for n-type Si). For many practical purposes such as microelectronic fabrication, the presence of this type of contact interface is detrimental to the overall function of the wider device. The Schottky barrier may be reduced by introducing a thin layer of heavily doped material between the metal and semiconductor. This decreases the barrier height and increases band bending such that electrons can tunnel through the barrier, producing an ohmic electrical contact.

The Schottky barrier can be useful however as it displays some current rectifying behaviour similar to that of a P-N diode with subtle differences. As a device its operation is based on a single charge carrier (electrons in the case of n-type) which make it useful for fast switching operation as there are no stored charge effects like that of a P-N junction. The operation of the Schottky diode under an applied external is are described in Figure 1.4. By convention the forward bias direction is defined as the direction in which the Schottky diode produces the greatest current response (for both n and p type diodes). This convention will be challenged by the device introduced in chapter 5 which can have 'forward bias' current levels at both positive and negative polarities. Nevertheless, the application of a forward bias (positive bias to a n-type Schottky diode) increases the current though the device. A positive bias applied to the metal reduces the energy barrier in the semiconductor by $q(V_{bi} - V_F)$ which allows more electrons to overcome the barrier and appear in the metal as current. The depletion layer width is narrower relative to the initial state with no bias applied ($W_i > W_{VF}$), as more electrons from the bulk of the semiconductor diffuse up to the contact to replace those that are extracted as current.

Under reverse bias the energy barrier height for the electron in the semiconductor is increased to $q(V_{bi}+V_R)$. In turn, the increased barrier height prevents electrons in the semiconductor moving through the contact. The applied reverse bias voltage increases the depletion layer width and number of ionised donors as electrons drift away from the contact. It is important to note that the ionised donor atoms are frozen in the lattice throughout operation and despite their charge, do not drift under applied. The depletion layer width changes in response to applied bias for reasons mentioned above. The implications of donor atoms that are mobile in the lattice are considered in chapters 5 and 6, and how donor atom mobility affects the built in voltage and width of the depletion region.

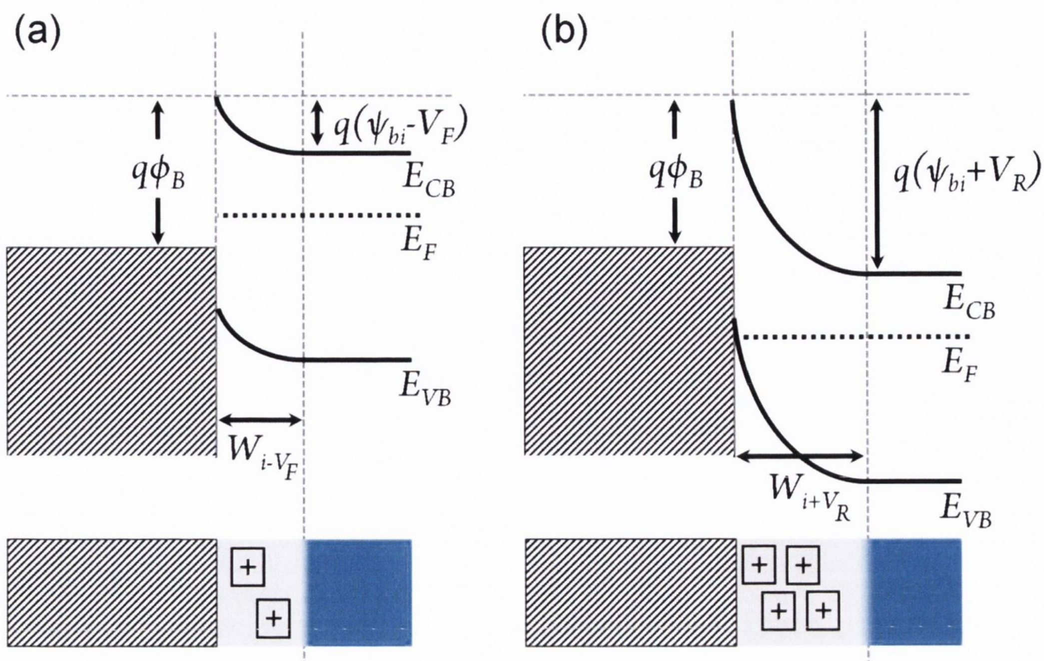


Figure 1.4 Schematic illustration of a Schottky diode under forward bias V_F (a) and reverse bias V_R (b). Under forward bias (positive bias applied to the metal) the energy of the semiconductor is shifted upwards. As a result the barrier for injection into the metal is lowered allowing more carriers to reach the metal for current conduction. There is a decrease in depletion layer width and built in voltage as the number of ionised donor atoms in the depletion region is decreased. Under reverse bias (negative bias applied to the metal) the barrier for injection into the metal is increased which prevents electrons moving across the contact inhibiting current. The number of donor atoms increases as the depletion region width increases, as electrons are drawn away from the contact under the applied voltage.

Carrier transport mechanisms present in a Schottky diode under applied bias include emission of carriers over the potential barrier height into the metal – thermionic emission (TE). Quantum mechanical tunnelling of carriers through the barrier into the metal – field emission (FE). TE and FE processes together – thermionic field emission (TFE). Recombination of charge carriers and diffusion of electrons and holes. For moderately doped Schottky diodes TE captures the device operation adequately. FE and TFE are more prevalent in heavily doped Schottky diodes and provide ohmic conduction. Recombination and diffusion of carriers are present largely in p-n diodes. Current density in Schottky diode under the TE conduction mechanism is described by:

$$J = A^{*}T^{2}exp\left(\frac{-q\phi_B}{kT}\right)\left[exp\left(\frac{qV_F}{nkT}\right) - 1\right] \quad (1.8)$$

With A^* the Richardson constant and n the ideality factor which captures non ideal contact deviations such as barrier height inhomogeneity or the presence of an interfacial layer. Conduction is heavily dependent on the barrier height ϕ_B of the contact which is assumed to remain constant regardless of applied bias. This is not always the case however due to image force lowering and the Schottky effect which are discussed in chapter 5.

1.5 Interaction of Light with Semiconductors

Photoexcitation is the mechanism by which light incident on a semiconductor creates an electron-hole pair. Light photons with energy equal to or greater than that of the semiconductor bandgap energy can excite a valence band electron into the conduction band to produce the electron-hole pair. It offers an additional route to increase the number of charge carriers in a semiconductor which is typically given by the temperature dependent statistical distribution (Fermi-Dirac distribution) mentioned in the previous section. Electron-hole pairs may become bound to each other by their attractive Coulombic interaction. In this case the pair are collectively known as an exciton which can exist as either weakly bound essentially free carriers (Wannier-Mott excitons) or tightly bound highly localised carriers (Frenkel excitons) [16]. In most cases they behave similarly to other carriers with unique effective mass, mobility and lifetimes.

Semiconductor materials that display strong absorption of light are known as photoconductors. Typically photoconductors are used in solar cells as a mechanism to convert light energy into solar power. The excess current these materials produce under illumination is called the photocurrent I_{Ph} which is defined as the difference between device current without light stimulus (I_{Dark}) and the current when light is incident on the device $I_{Illuminated}$, ($I_{Ph}=I_{Illuminated} - I_{Dark}$). Before the electron-hole pair can contribute to the device current the pair must be separated and extracted from the device before they recombine. The carrier lifetime τ is defined as:

$$\tau = \frac{n}{G_e} \qquad (1.9)$$

n is the excess carrier density and G_e is the carrier generation rate:

$$G_e = \eta\left(\frac{P_O}{h\nu}\right) \Big/ AD \qquad (1.10)$$

Where η is the quantum efficiency, P_{Opt} is the optical power, A is the device area under illumination and D is the depth or height of the device. The separation of charge occurs readily for electron-hole pairs created in the depletion region of the semiconductor and also for carrier pairs that diffuse into it. The intrinsic electric field in the depletion region sweeps the carriers away from each other and into the circuit generating the photocurrent. Therefore a wide depletion region increases device sensitivity as more of the photogenerated carriers in the material are extracted. A large depletion region however will increase the transit time - the time it takes carriers to traverse the depletion region. This will slow the response of the photodetector. Thus there is a trade-off in photodetectors between speed (response time), sensitivity and gain.

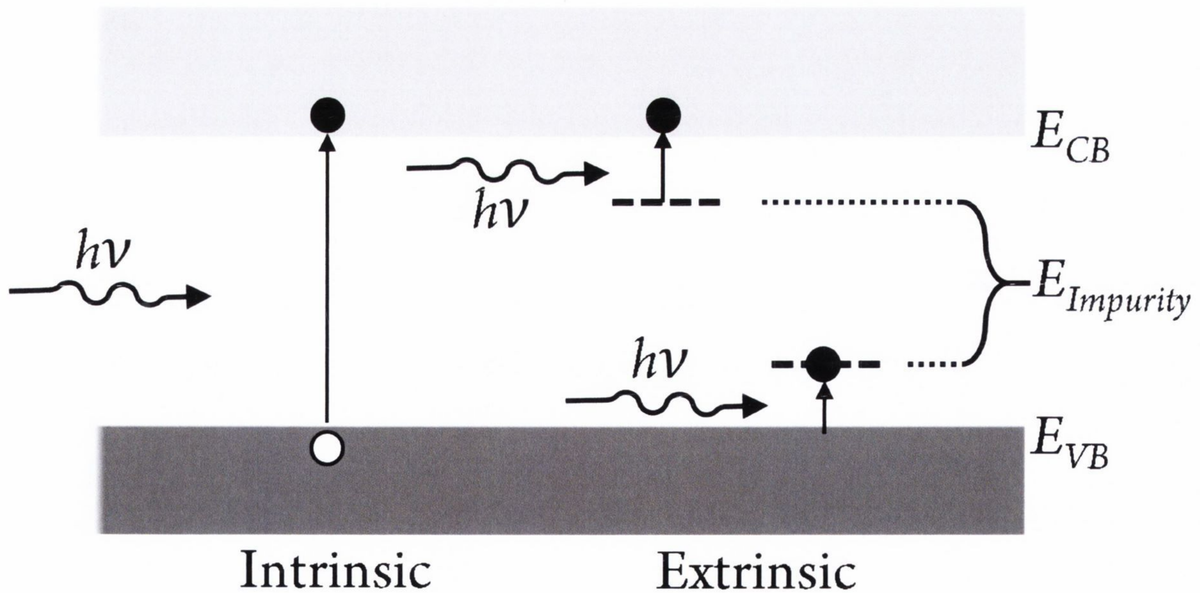


Figure 1.5 An illustration of the two types of photoexcitation in semiconductors by the interaction of light. Intrinsic band to band photoexcitation takes place at photon energies equal to or greater than the bandgap of the semiconductor. Extrinsic photoexcitation takes places between impurity energy levels in the bandgap of the semiconductor and accounts for spectral absorption at sub bandgap photon energies.

Typically photoexcitation occurs as band-to-band transitions of carriers in a process known as intrinsic photoexcitation. Photoexcitation may also take place between impurity energy level states within the semiconductor bandgap as illustrated in Figure 1.5. This process of photoexcitation between the impurity level and energy band is called extrinsic photoexcitation. Extrinsic photoexcitation is an important process for evacuating carriers defect states and other states within the forbidden energy zone such that they can contribute to conduction.

The concentration of charge carriers in a semiconductor can be increased above levels established under thermal equilibrium when external stimulus such as light or voltage bias are applied to the material. There are processes within the material that act to restore the thermal equilibrium concentrations which are known as recombination process. Band-to-band electron-hole recombination is the inverse of intrinsic photoexcitation. An electron-hole pair can recombine in a radiative process to emit a photon with energy equal the bandgap of the semiconductor. Electron-hole recombination may also occur radiatively between impurity or trap levels. Non-radiative recombination occurs when the energy of an electron in transition from the conduction band to the valence band is conserved by the generation of a phonon or by transfer of energy to another free electron or hole.

1.6 Microelectronic Nanotechnology: Smaller, Cheaper, Faster

The microelectronics industry has perhaps benefitted the most from embracing nanotechnology. The iterative increase in computational power over the past 50 years is a direct result of successfully scaling down transistor components to the nanoscale. This process is best captured by Moore's law, which predicts the number of transistors per chip doubling every two years [17]. Additionally, the increased number of transistors per wafer produced also drives down the price of each individual chip. Moore's law has proved remarkably accurate over many decades, with the International Technology Roadmap for Semiconductors (ITRS) predicting the introduction of 5 nm nodes by the year 2020 based on conventional technology [18]. Beyond 5 nm nodes, the industry has yet to produce an action plan with some speculators foreseeing the end of Moore's law [19].

Current state of the art processors use a six transistor configuration with metal oxide semiconductor field effect transistor (MOSFET) transistors as the base unit. The technology is known as static random access memory (SRAM) and is the fastest type of semiconductor

memory currently available. It is attractive because of its speed and low power consumption due to of its flip-flop transistor configuration. Scaling this technology is becoming increasingly difficult however. As a result, SRAM remains relatively expensive and reserved only for use in desktop/high power computing. Smaller size features (nodes) in the MOSFET unit cells will continue to develop this technology but short channel effects such as drain induced band bending and gate induced drain leakage will become increasingly prominent as the node size decreases.

Currently there are many other RAM technologies under development which have the potential to surpass the functionality of the SRAM processor. Resistance switching RAM (RRAM) is the frontrunner for low power, low cost processing. RRAM devices operate a non-volatile memory (NVM) - an inherent property that retains information without consuming external power. This type of technology is therefore perfect for emerging mobile platforms, including tablets and mobile phones. Together these markets are set to increase rapidly over the coming years as the proliferation of mobile technology continues.

The original reports of resistive switching were in 1960 for insulator materials sandwiched between metal contacts (MIM) [20, 21]. It was recognised early on that there was some controlled breakdown phenomena taking place in the insulator under large applied electric fields producing a measured change in device resistance (resistance switch). The mechanisms behind these transitional effects was not well understood at the time. As these breakdown phenomena were studied, a class of so-called resistance switching phenomena were identified based on device characteristics [22]. These characteristics primarily included current-voltage hysteresis loops that were pinched at the origin [23]. As more and more devices were reported, resistance switching emerged to have two basic modes of operation in devices – bipolar and unipolar device operation [24].

Bipolar switching involves actively changing the device resistance by applying a voltage with polarity (positive or negative in magnitude) opposite to that of the polarity used to produce the initial resistance change. Unipolar switching takes place under one polarity (either positive or negative). Figure 1.6 captures this process schematically for both switching types. Typically a pristine resistive switching device will be in a high resistance state known as the 'off' state. In order to switch to the low resistance state a sufficient voltage must be applied to the device to induce or 'set' the transition. The set operation is prevalent in both bipolar and unipolar switching. The difference between the two becomes apparent when the device is switched back into the high resistance state or 'reset' of the device. With unipolar resistance switches, reset occurs once a certain threshold current level is reached under one bias polarity applied in the

same direction as the set bias. With bipolar devices, reset must occur at the opposite polarity to that to the set bias polarity. The nature of each is defined by the material and the type of mechanism causing the change in resistance.

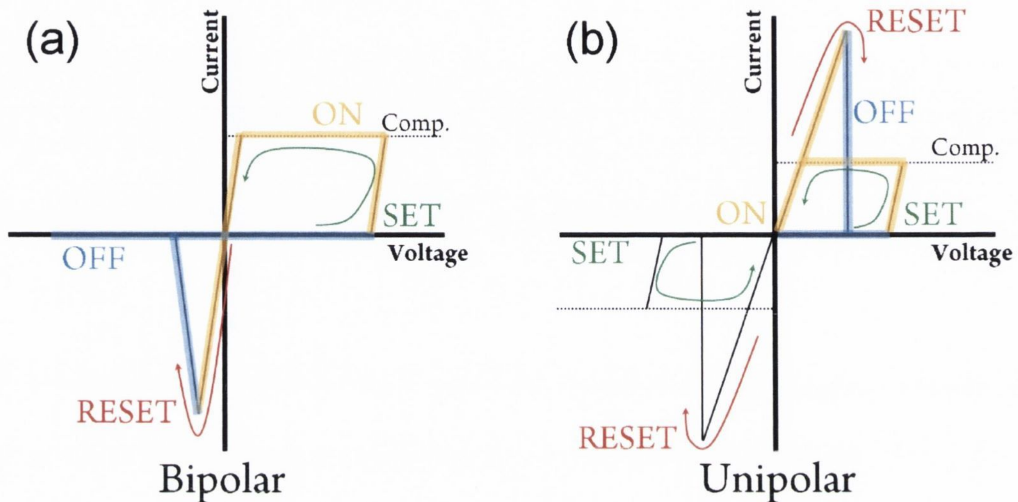


Figure 1.6 (a) Bipolar switching. The device is reset under opposite polarity of the set bias. (b) Unipolar switching display switching between set and reset at one polarity. Comp. is a user defined compliance current used to prevent device damage.

There are various physical phenomena that can induce a large resistance change within a material including phase change, magnetic polarisation and magnetoresistance change [25, 26]. For this introduction our discussion will be confined to the main three phenomena reported to be responsible for RRAM switching however. Each of these is driven by the application of an external voltage. The first type of phenomena that can induce resistance switching is the so called 'thermochemical mechanism' (TCM), which involves current induced heating in a material known as Joule heating. Joule heating is a process by which heat is dissipated by current flow, the movement of electrons in a material causes them to exchange energy with lattice atoms in the material. The amount of heat released via Joule heating P, in Watts is proportional to the resistance of the material times the square of the current $P=RI^2$. Many resistance switching materials are transition metal oxides (TMO) that display high levels of resistivity in the pristine state, typically between 10^{7-12} Ohm/m. Therefore, any modest current

through the device will produce a large build up of local heat in the material. The local heat promotes electromigration of lattice atoms (from the metal or TMO) under the applied electric field leading to the formation of low resistance pathways called conductive filaments (CF). In this switching regime the CF may be composed of electrode metal transported into the TMO or a partially dielectrically broken down TMO. The device is Reset by allowing sufficient current to pass along the CF such that the heat ruptures the CF, switching the device back to the off state.

TCM resistive switching is considered unipolar. The strength of the filament is determined by the compliance current manually assigned by the user during the initial forming set step. Forming the device is non-trivial and is often performed iteratively. Attempting to produce a strong filament with low resistance in one step can result in huge power dissipation spikes the instant the filament bridges the electrodes resulting in damage to the probing setup and the device. This effect can be offset by driving the forming with current as opposed to voltage [27]. This type of RS has been predominately reported for NiO materials although there are many reported instances where other TMOs are reported to switch via a Joule heating mechanism [28-30].

The next type of RS mechanism that will be discussed is commonly referred to as electrochemical metallization or ECM. It is realised by the reduction of anode metal atoms followed by their deposition on the cathode to again form a conductive filament bridging the two electrodes of a MIM device. Of the two cell electrodes one is made of an electroactive metal (Ag, Ni, Cu) that contributes atoms to the insulator. The insulator is considered a solid electrolyte that facilitates mobile ionic transport to each electrode. To complete the cell an inert metal such as Au or Pt is required that is not consumed or degraded by the redox reactions taking place in the cell. Typically only electron exchange reactions take place at this electrode. Mobile ions are introduced at the anode where they are oxidized and liberated from the electroactive metal. These ions drift under the applied bias and are reduced upon contact with the inert cathode. The filament continues to grow out from the cathode as more metal ions are deposited onto it. As before in TCM, the device is considered set or on once this filament has bridged the two metal contacts. To reset the device the CF is destroyed by the dissolution of ions from the filament under an applied bias of the opposite polarity of that used to form the filament. Hence this switching process is bipolar in nature. To date, there is much work published on this type of resistive switching for various ECM ion/electrode pairs [31-35] .

The final RS process that will be introduced is the valence change mechanism (VCM). With VCM, the semiconductor layer spanning the two metal contacts is the active material undergoing change. It is perhaps a more difficult concept of switching to describe whose physical origin is also more contested than the ECM and TCM RS mechanisms. To introduce this mechanism binary TMOs such as TiO_2 and NiO are considered as the prototypical VCM RS cells [27, 36-41]. In their pristine state, they are high resistance materials. Only through introducing defects do they become somewhat conductive. Intrinsic defects, that is anions or cations generated in the lattice matrix of the TMO and alter the stoichiometry of the material. Electrode metals act as catalysts in this instance, and play an important role in the reset by adsorbing defects from the TMO lattice [42].

Intrinsic defects generated in the semiconductor lattice will not only alter the stoichiometry of binary TMOs, but also the valence of the lattice metal and/or lattice oxygen. For the case of hypo-stoichiometric binary TMOs (MO_{x-d} ,d>0) oxygen is removed from the lattice producing two electrons and an intrinsic cation with an equal but opposite charge. The most common cation formed is the oxygen vacancy with cationic metal interstitials also considered. Often it is difficult to precisely assign the switching action of the cell to one defect or the other. Both hypo-stoichiometric defects generate two delocalised mobile electrons to the lattice and thus they can be considered n-type dopants. On the other hand, hyper-stoichiometric binary TMOs (MO_{x+d} ,d>0) result from the formation of oxygen interstitials or metal vacancies both of which have an associated -2 charge. They accept two conduction band electrons from the lattice and therefore leave two delocalised holes free to contribute to conduction within the material. These defects are commonly referred to as p-type and have been shown prevalent for CoO, MnO and FeO [43].

Hyper and hypo-stoichiometric defects are introduced into the TMO lattice via an electroforming step. Two processes have been reported for VCM. The first includes the formation of a CF composed of defects in the TMO similar to TCM and ECM has also been proposed for VCM. The intrinsic defects created during electroforming the TMO have an associated charge and thus drift under applied bias. The device is set when the defects form a CF between the two electrodes as before. The device is reset through local CF redox reactions that break the conduction path in the material. The second proposed mechanism does not involve a CF at all, rather charged defects generated during electroforming homogeneously build up at a contact interface locally altering the composition of the interface TMO at the contact. The process is analogous to doping the contact interface discussed previously which alters the local electronic band structure of the contact. To reset the device some ions captured

by the electrode metal are reintroduced into the doped TMO interface layer when the bias polarity is changed. This re-establishes normal stoichiometry locally thereby reproducing the pristine high resistance state.

1.7 Scope & Summary

The motivation of this thesis is presented in the context of gaining an appreciation of modern aspects of nanoscience and nanotechnology. The emergence of nanoscience in the latter half of the 21st century has led to many new scientific discoveries that have helped society as a whole. This has helped secure public funding in the field of nanoscience ensuring its future as a dynamic and innovative field. Industry has also helped drive research and innovation in nanoscience, not least in the drive for maintaining Moore's scaling law in semiconductor devices now ubiquitous in modern technology. An introduction to the technical aspects of maintaining this scaling law are given in chapter 1 along with the fundamental aspects of semiconductor physics. Chapter 1 concludes with a detailed description of emerging RRAM technologies that can not only offset the decreasing size requirements of Moore's law but also offer relatively low power consumption.

Chapter 2 gives an overview of the various experimental techniques and methods used throughout the thesis. These techniques include SEM, TEM, EBL, FIB and metal deposition that makeup the basic toolsets used by nanoscientists to fabricate and characterise experiments. Aspects of the technical measurements such as relevant parameters used to generate data and characterise samples are also given for the purpose of continuity with new and similar devices in future work.

Chapters 3 and 4 introduce the first major research section of the thesis that focuses on a novel nanoparticle synthesis technique that is unique in the major role the surface energy plays throughout synthesis. Chapter 3 begins with a summary of conventional synthesis techniques such as solvothermal and vapour-liquid-solid synthesis. Both methods are relevant for the appreciation of the novel surface energy driven growth (SEDG) that has many shared growth principles defining crystal saturation and growth. Chapter 3 then describes in detail the relevant physical phenomena that uniquely define the SEDG method at each separate stage of the synthesis. The detailed description of the physical phenomena is accompanied with a shorter seven step process overview that captures the relevant steps necessary to design and produce a

new nanoparticle using the SEDG method. The seven step process overview will allow new readers in the area to quickly begin experimentation with new materials in future work.

Chapter 4 follows the design and production of single crystal iron nanocubes using the SEDG method introduced in the preceding chapter 3. Iron was chosen as the candidate synthesis material due to its desirable magnetic and catalytic properties. Neodymium was chosen as the alloy material due to the relatively simple binary alloy phase diagram and the wealth of FeNd alloy material properties available in literature due to its popularity as a strong magnetic material. Initially, the goal was to produce single crystal wires of iron that would display an inherent magnetisation anisotropy due to the aspect ratio of the wire. The lowest energy crystal surface which defines the equilibrium shape of an iron nanoparticle is given as <100> in literature [44]. The resulting iron nanocubes produced following the SEDG synthesis confirms <100> surface as the lowest energy crystal surface at the 700 °C process temperature. Interestingly, the cubes were formed with an intermetallic capping layer consisting of an FeNd crystalline alloy. Although it proved difficult to fully characterise is it still a noteworthy observation which may serve to inhibit oxidation of the iron nanocube core improving its potential applications in catalysis. The size of iron cubes produced depends heavily on the amount of iron material deposited in a thin film prior to processing. This offers a degree of control over the size of nanocube produced providing more design and production choices for their application in devices.

Chapters 5 and 6 capture the second research section in this thesis with a focus on semiconductor device fabrication and characterisation. The relevant background for the principles of nanoscience and semiconductor physics are given in chapter 1. These principles are built on in chapter 5 with the introduction of a specific type of resistance switching semiconductor memory known as the memory resistor or memristor. The device, based on a single nanowire of TiO_2 in contact with a metal electrode displays dynamic and evolutionary electrical properties in response to the same voltage pulses. The dynamic creation of oxygen vacancies at the cathode under voltage bias that alter the electronic band structure of the metal semiconductor interface adequately explains the device evolution. The population of oxygen vacancies in the wire responds to an applied voltage field by drifting about the wire allowing their position to be defined during testing. Switching the polarity of the voltage can eliminate the generated vacancies by pushing adsorbed oxygen back into the wire, this effectively established a small pristine region of TiO_2 at the interface that displays a high resistance or off state. Taking this phenomena to its conclusion we display a six memory level logic cell that can be reset easily. When fully realised, such six or more level logic cells could increase the

density of information stored per bit in the cache memory of a processing unit for faster execution and data recall.

In chapter 6 similar single TiO_2 nanowire devices are used. TiO_2 is a well known photovoltaic material and its interaction with UV light is well documented in literature for producing energy from sunlight. Chapter 6 follows the electrical characterisation of UV light with the single nanowire devices. Under steady state conditions, the device responds like a photoconductor with a small increase in current detected when the UV light is impingent on the wire. Interestingly, the UV light was observed to introduce oxygen vacancies into the wire at a faster rate than that of the electroforming given in chapter 5. Finally, using the two separate stimulus of UV laser light and electrical voltage pulses it is possible to show associative memory in the wire. This is the first instance an inorganic material has displayed this memory association for separate stimulus and provided an exciting and promising outlook for a new class of neuron like resistors or neuristors that display biological like learning and adaptability.

1.8 References

1. *'Plenty of room' revisited.* Nat Nano, 2009. **4**(12): p. 781-781.
2. Binnig, G. and H. Rohrer, *Scanning tunneling microscopy.* IBM J. Res. Dev., 1986. **30**(4): p. 355-369.
3. Toumey, C., *35 atoms that changed the nanoworld.* Nat Nano, 2010. **5**(4): p. 239-241.
4. *"President Clinton's Address to Caltech on Science and Technology". California Institute of Technology.* 2000.
5. Drexler, K.E., *Molecular engineering: An approach to the development of general capabilities for molecular manipulation.* Proceedings of the National Academy of Sciences, 1981. **78**(9): p. 5275-5278.
6. Viet Ha, C., et al., *Synthesis and optical properties of water soluble CdSe/CdS quantum dots for biological applications.* Advances in Natural Sciences: Nanoscience and Nanotechnology, 2012. **3**(2): p. 025017.
7. Li, Y., et al., *Nanowire electronic and optoelectronic devices.* Materials Today, 2006. **9**(10): p. 18-27.
8. Chu, S., et al., *Electrically pumped waveguide lasing from ZnO nanowires.* Nat Nano, 2011. **6**(8): p. 506-510.
9. Chen, X., et al., *Nanowire-based gas sensors.* Sensors and Actuators B: Chemical, 2013. **177**(0): p. 178-195.
10. Peng, F., et al., *Silicon-Nanowire-Based Nanocarriers with Ultrahigh Drug-Loading Capacity for In Vitro and In Vivo Cancer Therapy.* Angewandte Chemie International Edition, 2013. **52**(5): p. 1457-1461.
11. Novoselov, K.S., et al., *Electric Field Effect in Atomically Thin Carbon Films.* Science, 2004. **306**(5696): p. 666-669.
12. Geim, A.K. and K.S. Novoselov, *The rise of graphene.* Nat Mater, 2007. **6**(3): p. 183-191.
13. Butler, S.Z., et al., *Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene.* ACS Nano, 2013. **7**(4): p. 2898-2926.
14. Brattain, W.H., *Genesis of the Transistor.* The Physics Teacher, 1968. **6**(3): p. 109-114.
15. Sze, S.M. and K.K. Ng, *Physics of Semiconductor Devices*. 2006: Wiley.
16. Fox, M., *Optical Properties of Solids*. 2010: OUP Oxford.
17. Moore, G.E., *Cramming More Components Onto Integrated Circuits.* Proceedings of the IEEE, 1998. **86**(1): p. 82-85.
18. *International Technology Roadmap for Semiconductors 2013 Edition*. Available from: http://www.itrs.net/Links/2013ITRS/Summary2013.htm.
19. *"End of Moore's Law: It's not just about physics". CNET. August 28, 2013.*
20. Simmons, J.G. and R.R. Verderber, *New Conduction and Reversible Memory Phenomena in Thin Insulating Films.* Proceedings of the Royal Society of London. Series A. Mathematical and Physical Sciences, 1967. **301**(1464): p. 77-102.
21. Gibbons, J.F. and W.E. Beadle, *Switching properties of thin Nio films.* Solid-State Electronics, 1964. **7**(11): p. 785-790.
22. Dearnaley, G., A.M. Stoneham, and D.V. Morgan, *Electrical phenomena in amorphous oxide films.* Reports on Progress in Physics, 1970. **33**(3): p. 1129.
23. Chua, L., *Resistance switching memories are memristors.* Appl. Phys. A 2011. **102**(4): p. 765-783.
24. Sawa, A., *Resistive switching in transition metal oxides.* Mater. Today, 2008. **11**(6): p. 28-36.
25. Jeong, D.S., et al., *Emerging memories: resistive switching mechanisms and current status.* Rep. Prog. Phys., 2012. **75**(7): p. 076502.
26. Waser, R., et al., *Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges.* Adv. Mater. , 2009. **21**(25-26): p. 2632-2663.

27. Jeong, D.S., et al., *Characteristic electroforming behavior in Pt/TiO2/Pt resistive switching cells depending on atmosphere.* J. Appl. Phys., 2008. **104**(12): p. 123716.
28. Yun, J.-B., et al., *Random and localized resistive switching observation in Pt/NiO/Pt.* physica status solidi (RRL) – Rapid Research Letters, 2007. **1**(6): p. 280-282.
29. Shima, H., et al., *Resistance switching in the metal deficient-type oxides: NiO and CoO.* Applied Physics Letters, 2007. **91**(1): p. -.
30. Inoue, I.H., et al., *Nonpolar resistance switching of metal/binary-transition-metal oxides/metal sandwiches: Homogeneous/inhomogeneous transition of current distribution.* Physical Review B, 2008. **77**(3): p. 035105.
31. Kozicki, M.N., P. Mira, and M. Mitkova, *Nanoscale memory elements based on solid-state electrolytes.* Nanotechnology, IEEE Transactions on, 2005. **4**(3): p. 331-338.
32. Sakamoto, T., et al., *Nanometer-scale switches using copper sulfide.* Applied Physics Letters, 2003. **82**(18): p. 3032-3034.
33. Terabe, K., et al., *Quantized conductance atomic switch.* Nature, 2005. **433**(7021): p. 47-50.
34. Kaeriyama, S., et al., *A nonvolatile programmable solid-electrolyte nanometer switch.* Solid-State Circuits, IEEE Journal of, 2005. **40**(1): p. 168-176.
35. Naoki, B., et al., *Effect of Ion Diffusion on Switching Voltage of Solid-Electrolyte Nanometer Switch.* Japanese Journal of Applied Physics, 2006. **45**(4S): p. 3666.
36. Kwon, D.H., et al., *Atomic structure of conducting nanofilaments in TiO2 resistive switching memory.* Nat Nanotechnol, 2010. **5**(2): p. 148-153.
37. Jeong, D.S., H. Schroeder, and R. Waser, *Mechanism for bipolar switching in a TiO2 resistive switching cell.* Phys. Rev. B, 2009. **79**(19): p. 195317.
38. Yang, J.J., et al., *Memristive switching mechanism for metal/oxide/metal nanodevices.* Nat Nanotechnol, 2008. **3**(7): p. 429-33.
39. Joshua Yang, J., et al., *The mechanism of electroforming of metal oxide memristive switches.* Nanotechnology, 2009. **20**(21): p. 215201.
40. Oka, K., et al., *Resistive-Switching Memory Effects of NiO Nanowire/Metal Junctions.* Journal of the American Chemical Society, 2010. **132**(19): p. 6634-6635.
41. Kim, D.C., et al., *Electrical observations of filamentary conductions for the resistive memory switching in NiO films.* Applied Physics Letters, 2006. **88**(20): p. -.
42. Li, W.X., et al., *Oxidation of Pt(110).* Physical Review Letters, 2004. **93**(14): p. 146104.
43. Chiang, Y.M., D.P. Birnie, and W.D. Kingery, *Physical Ceramics: Principles for Ceramic Science and Engineering*. 1996: Wiley.
44. Vitos, L., et al., *The surface energy of metals.* Surface Science, 1998. **411**(1–2): p. 186-202.

Chapter 2

Methods

2.1 Introduction

The principles behind many of the experimental techniques used throughout this thesis are introduced in this chapter including electron microscopy, lithography and fabrication techniques. Specific techniques are introduced in the relevant chapters as needed.

2.2 Electron Microscopy

Electron microscopy or Scanning Electron Microscopy (SEM) is the most common and simple method of imaging nanoscale objects and is performed using an in house Carl Zeiss Ultra SEM. It offers a facile and non-destructive way of studying the surface topography and characterising the composition of nanostructures. Over the years it has grown in popularity to become the staple characterisation tool in many laboratories.

To produce an image an electron beam is created with an electron 'gun'. The 'gun' or electron source can be made from three types of materials including thermionic emission sources Tungsten and Lanthanum hexaboride (LaB_6) as well as Field Emission Gun (FEG) materials. Cost, resolution and application are the driving factors in determining which electron source is used [1]. Source brightness, which is directly related to resolution, is a measure of current density per unit solid angle of the source in units of A/m^2sr. FEG sources offer the greatest brightness ~ 10^{12} A/m^2sr at 100kV, whereas Tungsten has the lowest, 10^{10} A/m^2sr at 100kV. FEG sources operate in high vacuum, ~ 10^{-6} Pa, Tungsten requires a much lower vacuum, ~10-2 Pa, which makes Tungsten more suited for low cost setups and imaging biological samples which outgas significantly in a modest vacuum.

Figure 2.1 is a schematic showing the column of an SEM. The electron source is held at a negative bias to emit electrons and form the beam. The anode is positioned close to the emitter. The sample is connected to ground to prevent sample charging which results in poor resolution. The energy of the emitted electrons can be altered by changing the acceleration voltage of the

source. The optimal acceleration voltage for good resolution is sample specific with typical source acceleration voltages for SEM ranging between 1-30 keV. The emitted electrons pass through a series of electromagnetic lenses and apertures which serve to focus and condense the beam onto the sample. A user will commonly change aperture sizes to increase the electron flux, thereby creating a stronger signal but with reduced spatial resolution.

To create an image the electron beam is rastered across the sample in a stepwise fashion. A detector collects electrons after they have interacted with the sample and obtains contrast via the relative differences in energy the electrons possess. There are many signals generated following the interaction of an electron with the sample. The most common signals are schematically shown in Figure 2.2. Detectors have been specifically developed to capture each separate signal produced from the beam interaction with the sample. Backscattered electrons – electrons that have been scattered through a large angle are detected with a detector close to the incident electron beam. The in line detector (Inlens) signal contains both topographical and compositional information.

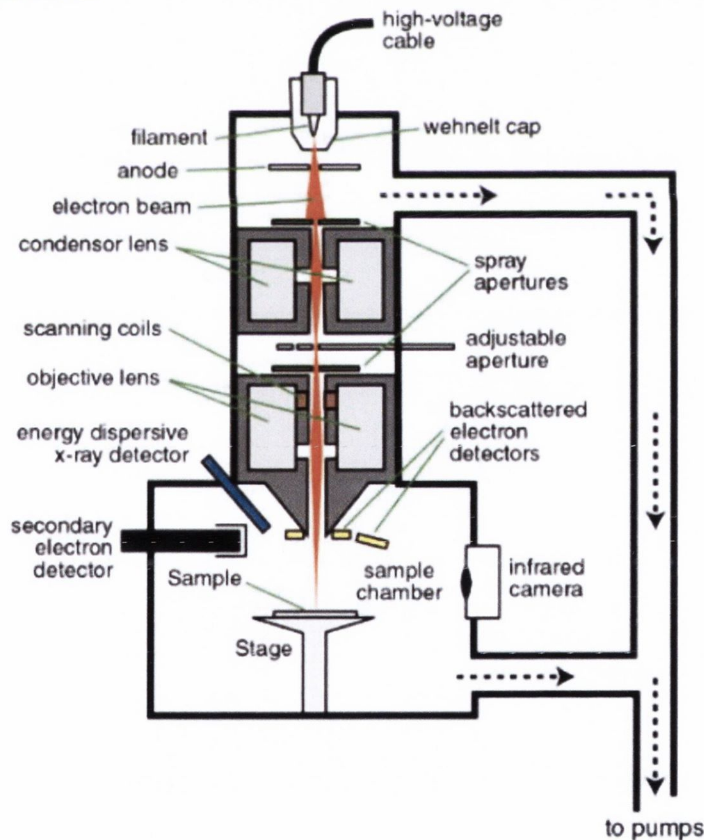


Figure 2.1. Schematic describing the main elements of a Scanning Electron Microscope [2]. The filament is used to produce a beam of electrons that travel down the length of the column. Electromagnetic lenses shape and deflect the beam while apertures control the flux of electrons. Various detector lenses are placed around the sample to pick up electrons that have interacted with the sample.

The strength of the backscattering signal depends greatly on the atomic number of the atom as heavier atoms will more efficiently scatter incident electrons through a large angle, thus compositional information about the surface can be obtained from the scattering intensity and thus the contrast in the image. The resolution of backscattered electrons is worse than that of secondary or Auger electrons due to the greater penetration depth and interaction area of backscattered electrons. Hence the energy of the backscattered electrons is more disperse resulting in poor resolution. Secondary electrons are created when the incident electron beam ionises the surface atoms of the specimen, allowing loosely bound electrons to be emitted. They are created throughout the sample, but due to their low energy (3-5 eV) they can only escape the surface and reach the detector within a depth of a few nanometers. The secondary electron signal contains topographical contrast information about the sample with the best resolution of ~ 10 nm. The Auger electron signal is relatively more complicated to interpret. The energy contained within Auger electrons is characteristic of the bonding within the atomic or molecular orbital structure. This gives element specific compositional information about the material. They are created when an electron from an ionised atom loses energy by relaxing back from an excited outer shell to fill an inner shell vacancy. The X-ray signals produced from the incident beam can be used to obtain more quantitative information about the elemental makeup of the sample being probed. X-ray photons are created when an electron in the outer orbital shell radiates energy to relax and fill the core level hole created by an incident electron. Thus the energy of the X-ray photon can be correlated to the specific atomic transitions between energy levels of an atom thereby, allowing elemental analysis. [3]

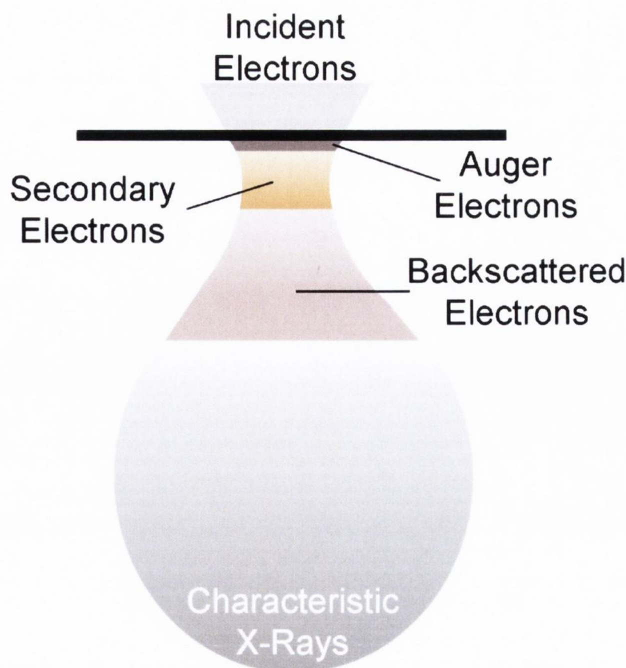


Figure 2.2. Schematic depicting the various interactions incident electrons produce on striking the sample.

2.3 Transmission Electron Microscopy

Ground breaking work by Knoll and Ruska in 1932 laid the foundation for transmission electron microscopy TEM. Their invention allowed the user to observe objects for the first time with resolution below that of contemporary light microscopes whose resolution is set by the optical diffraction limit. Building on their discovery, modern transmission electron microscopy (TEM) has developed as the premier method for characterising materials at the nanoscale.

The method is fundamentally different to SEM described in the previous section as electrons interact with and pass through the specimen. Detectors on the opposite side of the specimen collects these electrons which contain information about the sample. Typically specimens less than 100nm thick are required for effective TEM, thicker samples will scatter the incident electrons too much thus reducing resolution. Many nanomaterials are be easily examined with TEM provided they can be dispersed in solution for facile deposition on a TEM grid. Bulk

materials, thin films, specific interfaces or surface features etc. need to be isolated from their growth/operation substrate for analysis. This requires an extra processing step known as lamella preparation (described in a later section) to thin the desired cross section of the sample to less than 100nm in thickness.

The resolution of the final TEM image is related to the electron signal which interacts with and passes through the sample. The transmitted signal is dependent on factors such as the acceleration voltage, sample thickness, the atomic mass number of the atoms in the sample, sample density and crystallinity. Resolution can be boosted by increasing the acceleration voltage and using thinner samples, both of which are readily under the operator's control. However, at higher acceleration voltages samples are easily damaged by the electron beam itself which makes sample thickness and the lamella preparation quite important. Typically acceleration voltages between the 50-300 keV range are used for most samples. It is worth noting the ultimate resolution of the TEM is not set by the electron energy emitted by the gun. A 100 keV electron has a corresponding wavelength of 4 pm, this translates to a theoretical resolution of 2 pm [1]. But the resolution limit of the TEM is in practice determined by the quality of the electromagnetic lenses and their ability to interact with the beam.

A schematic describing the TEM column is shown in Figure 2.3. The electron gun and condenser lenses used to focus the beam before it interacts with the specimen are not shown. By changing the strength of the intermediate lens and adding or removing the objective aperture it is possible to interchange between diffraction imaging mode and imaging mode. Selected area diffraction (SAD) may be required when the sample area illuminated with the beam has different crystal orientations or grains. The SAD aperture allows the operator to define which illuminated area of the sample will produce the diffraction pattern and is used extensively for characterisation in Chapter 4.

Diffraction imaging in TEM (FEI Titan) is a powerful tool for characterising crystalline samples. It is analogous to standard X-ray diffraction with the advantage of being extremely site specific. This allows the crystal structure of individual grains within a sample separated by a few nanometers to be resolved using SAD. Electrons elastically scattered by the regular repeating lattice of a crystalline specimen with interfere with each other to produce bright spots in a diffraction pattern that represent the reciprocal crystal lattice of the specimen. The relative distances and angle between these spots are used to assign a crystal structure to (index) the pattern as shown in Figure 2.4.

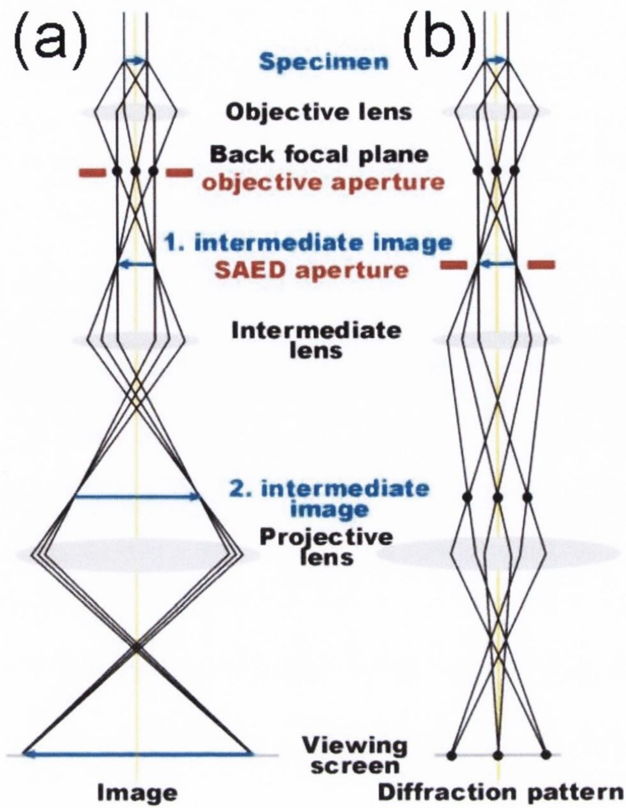


Figure 2.3 Schematic setup of the TEM column in two specific modes [4]. (a) Imaging mode, (b) diffraction pattern mode.

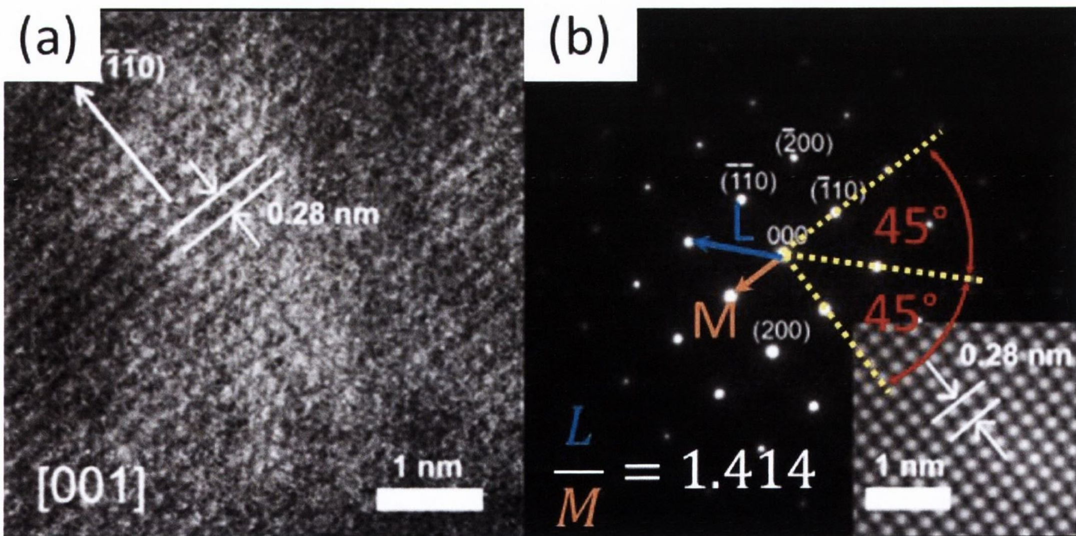


Figure 2.4 Indexing a Fe bcc crystal sample using TEM image (a) and its corresponding diffraction pattern (b). (a) The interplanar distance or lattice constant between adjacent lattice rows is measured and compared to reported literature values for bcc Fe. (b) The relative distance and angle between diffraction points can be compared with standard indexed diffraction patterns for characterisation.

2.4 Lithography

2.4.1 Electron-Beam Lithography

Electrons are a form of ionizing radiation. This is due to the fact they are electrostatically charged and behave as both particles and waves. When an electron beam is focused onto a sample covered in an electron sensitive material the beam can induce chemical changes in the material. The chemical changes taking place in the material under electron beam interaction sufficiently alter its properties to differentiate it from parts of the same that have not interacted with the beam. A substance sensitive to electrons is typically called the photoresist or simply resist. By exposing an area of the resist to an electron beam its properties are altered in such a way to change solvent solubility of the material in that area. The exposed area can then be removed provided the resist is positive tone, or remain on the substrate if the resist is negative tone. Either way a material pattern is created on the substrate designated by the areas exposed to the electron beam.

As early as the 1960s electron beam (e-beam or EBL) lithography was explored using electron microscopes as a method of producing microelectronic circuits. Almost immediately integrated circuits with sub-μm resolution were realised. E-beam techniques have improved considerably since the 1960s with sub 10 nm feature resolution standard across many SEM tools. EBL is now an integral part of many universities research infrastructure due to its great flexibility.

The technique involves irradiating a substrate coated in resist in a specific user defined pattern called a mask. The mask is not physical but designed and laid out using specialist software which can be interpreted by electron beam blanking hardware in the SEM. A beam blanker dictates which areas of the SEM field of view (write field) are exposed to the e-beam. To ensure reliable patterns are produced all variable parameters (such as dose, dwell time and step size) of the technique are reproduced identically for each exposure. This starts with the sample preparation prior to e-beam exposure.

The substrate must be cleaned prior to resist deposition as contaminants on the surface will negatively impact the technique causing the resist film to be inhomogeneous in thickness across the sample. After the surface is cleaned a resist is deposited and spun for a set rpm and time necessary to produce the required thickness.

The resist itself is chosen to meet the required application of the mask design. Thickness, sensitivity, and dose among other parameters will dictate the chosen resist. Currently there are many polymer resists available, all of which are suited to various applications.

There are two general types of resists based on how the interaction with an e-beam alters the resist properties. A positive tone resist becomes more soluble after e-beam irradiation and is preferentially removed relative to the rest of the resist film in the developing solution. A negative tone resist becomes less soluble after e-beam irradiation meaning only the e-beam exposed area remains in the developing solution. Positive resist is suitable for defining metal deposition areas such as device metal contacts. Negative resist are typically used to prevent a specific area from an etching processing step during integrated circuit fabrication. The resist is drop cast onto a sample then spun to achieve a set thickness between 1-1000 nm, which will ultimately affect resolution. Resist concentration, molecular weight and dilution all affect the final thickness of the film. The sample is then baked to remove any remaining solvent in the polymer film increasing stability.

The sample is then transferred to the SEM chamber where it can be exposed to e-beam radiation. Parameters such as e-beam current, step size, dwell time and dose are important for realising fine features and are all subject to optimisation. The beam current is set by the acceleration voltage and aperture size. Step size is the smallest increment the beam moves between each pixel in the user pattern. Dwell time is the amount of time the beam will expose a particular spot. The dose is dependent on the three previous factors namely beam current, step size and dwell time. These parameters are user defined and are subject to optimisation dose tests.

For this technique the ultimate resolution of the mask design is not limited by the electron beam ($\lambda \sim 0.1$ nm @ 12.5 keV) but by backscattered electrons generated following the e-beams interaction with the resist coated substrate. Backscattered electrons were discussed previously in the electron microscopy section. Their interaction with the sample is modelled using Monte Carlo simulations shown in Figure 2.5. The figure describes the collision path way incident electrons may follow upon striking the resist. The degree of lateral pathways spreading from the incident beam is more apparent at low acceleration voltage (2 keV and 5 keV). These proximity effects are undesirable as they lead to non-uniform exposure doses. These effects can only be mediated by changing the electron acceleration voltage. High acceleration voltage will produce more high-resolution features at the expense of throughput. This is due to the dose being lower as there are less electron resist interactions. Low acceleration voltages will

maximise e-beam resist interaction lowering the dwell time required on a feature therefore increasing throughput. Obviously a balance must be struck between throughput and resolution. In the context of this study, ebl sample fabrication was primarily for producing metal contacts 0.1-1 μm in width and up 100 μm long that connected an individual nanowire to the large UV drawn contact pads. In this instance low accelerating voltages of ~ 5 keV with 10 μm aperture were sufficient for resolution and through put. However there were some instances when contact pads and connecting contacts were drawn with ebl together in one step. For this a greater sized aperture was used, 30-60 μm with acceleration voltages of 10-15 keV. This facilitated fabrication of large feature sizes at a reasonable rate with sufficient resolution to contact an individual nanowire.

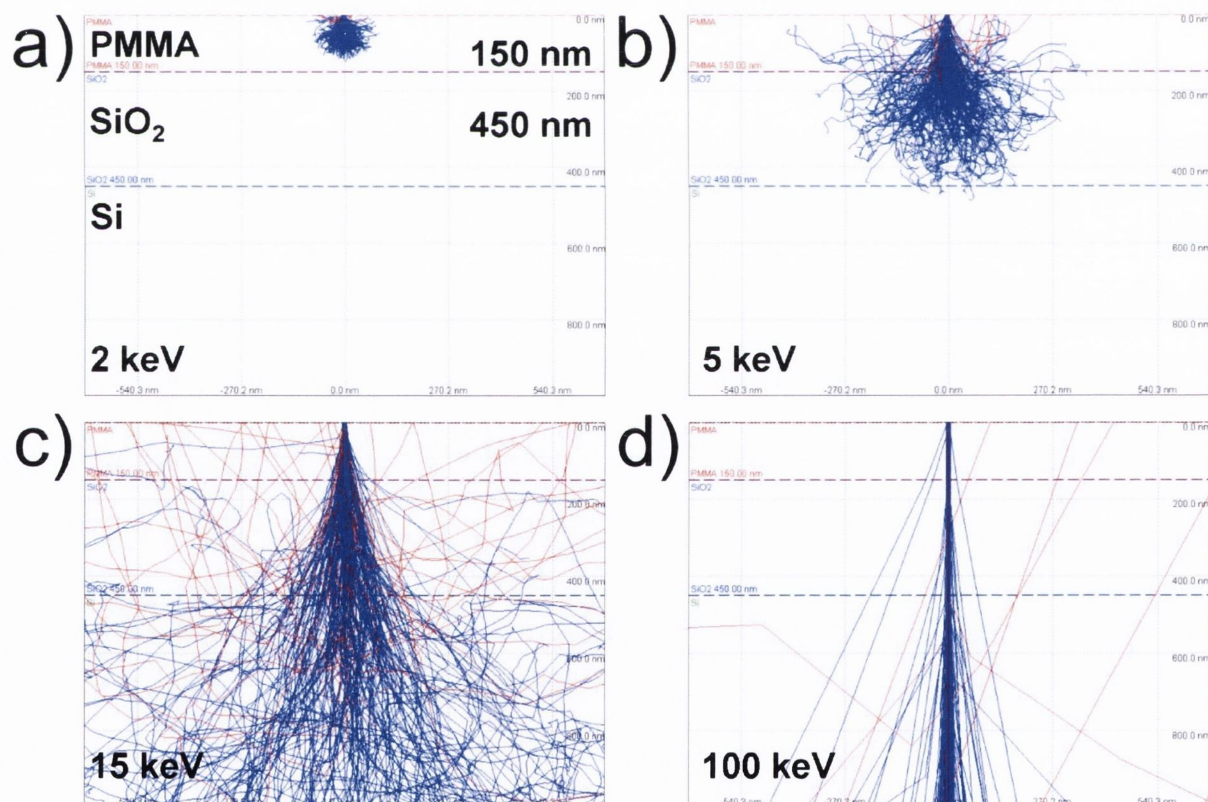


Figure 2.5 Electron trajectories through the resist and substrate at various acceleration voltages simulated by CASINO software [5]. (a) 2 keV profile with a denetration depth less than the thickness of the PMMA film. (b) 5 keV profile with lateral proximity effects. (c) 15 keV profile. (d) 100 keV profile showing minimal resist-ebeam interaction.

2.4.2 Ion-Beam Lithography

The ability to create a bright ion source from liquid metal ion sources (LMIS) was developed in the late 1970's [6]. This discovery lead to the development of ion beam columns similar to that of SEM. Ion beam techniques are used extensively throughout the semiconductor electronics industry for micro fabrication and failure analysis. The interaction of an I-beam with a sample is more complicated than an electron in SEM primarily due to the greater momentum the ions (typically Ga^{+}) have relative to electrons. The main advantages however is that an impinging I-beam can be used to locally remove (mill) material, the beam has relatively high current density, the beam can induce preferential deposition of metal, and the momentum of the impingent ion is great enough to break bonds in the surface. An image

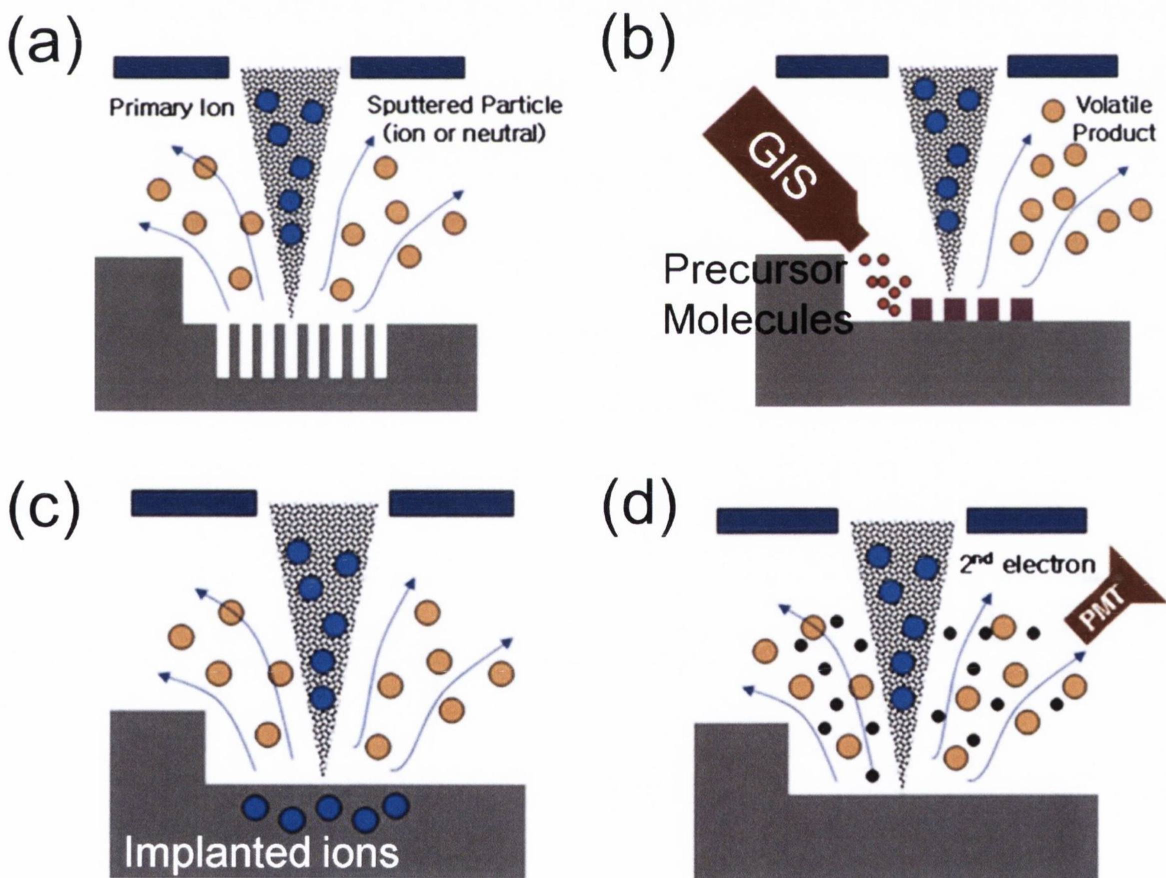


Figure 2.6. A schematic depicting the four I-beam interactions [7]. (a) Milling. (b) Gas assisted deposition. (c) Ion implantation. (d) Imaging with secondary electrons.

can also be produced in real time during milling as secondary electrons are produced as an artefact of the milling interaction. The interactions of the ion beam with the sample is shown schematically in Figure 2.6. These I-beam interactions are employed with traditional SEM to offer a wide range of material analysis techniques.

I-beam lithography has a similar set up to SEM except ions instead of electrons are focused onto the substrate and there is no need to use a resist. A LMIS serves as a reservoir of Ga. It is positioned in contact with a sharp W needle such that the liquid source can wet the needle. The Ga flows to the needle tip and is pulled under high field into a sharp cone shape where they are emitted as ionised atoms down the column. These ions bombard the surface transferring significant energy to the substrate. Imaging is achieved by the capture of secondary electrons generated at the surface of the material as the momentum of the ion is dissipated. However, even at low acceleration voltage some ion implantation from the beam is unavoidable as the I-beam is rastered across the sample.

Ion assisted deposition of metal and insulator materials is achieved through the dissociation of adsorbed precursor gases on the sample surface. Precursor molecules are introduced by a dedicated gas injection system (GIS). The molecules are directed to the substrate. The ion beam delivers sufficient energy to cause adsorbed molecules to decompose. After the precursor molecules decompose some material is left behind on the substrate while the volatile products enter the vacuum. Pt metal for example is introduced to the sample as a volatile organometallic molecule of $C_5H_4CH_3\ Pt(CH_3)_3$ that is then decomposed to form a Pt protective barrier.

The principle use of ion beams is the controlled removal of material from the substrate through ion milling. The milling process has similarities to sputtering – accelerated ions impact the substrate with enough energy to eject atoms from the substrate. Ion milling offers a more precise sputtering method which is used to define features on the sub-micron scale. Milling takes place where the ion beam is rastered across the surface, which can be imaged in real time by capturing the secondary electrons produced via the ion-substrate interaction which was discussed previously. The rate of removal of material from the substrate or sputter yield depends on several factors; channeling, angle of incidence, scan rate and redeposition.

2.4.3 FIB Lamella Preparation

Lamella preparation is a popular technique used to prepare samples for TEM analysis that cannot be easily deposited onto a standard TEM grid. In many cases it is necessary to take a small cross sectional piece of a sample in order to place it in a TEM [8]. This process is called sample lamella preparation. Producing a lamella is quite involved, requiring both long FIB tooling time and an experienced user for good results. The following is a generalised overview of producing one such lamella. Once a specific region of interest (ROI) is identified on the sample for TEM analysis it is necessary to coat it in a layer of W or Pt metal. Initially a thin layer of metal is deposited via e-beam assisted deposition before I-beam is used. E-beam deposition is slower relative to I-beam. The layer protects the ROI from I-beam induced damage over the course of preparing the lamella. Coarse thinning is performed either side of the ROI using high I-beam currents (3-5 nA). Finer cross sectional cuts performed with lower I-beam currents (1-2 nA) are used to thin the sample to 1 μm. The lamella is then undercut so it can be removed from the substrate.

Next a micromanipulator is brought into contact with the lamella and attached to it using GIS e-beam deposited W. The lamella is then lifted from the substrate and attached to a copper TEM grid using e-beam deposition. Once affixed to the copper TEM grid the micro manipulator is detached by milling the tip free. Further thinning of the lamella to a thickness of ~ 700 nm is performed using low I-beam currents (220 pA). Final thinning to sub 100 nm lamella thickness was performed using I-beam currents of 10–100 pA. Thinning at lower beam currents prevents structural/implantation damage to the ROI, allowing higher quality TEM analysis.

2.5 Material Processing

2.5.1 Physical Vapour Deposition

Physical vapour deposition (PVD) is a popular blanket deposition method for producing thin films and composite materials relatively easily. It is used extensively in research due to its versatility. It is often combined with top down fabrication techniques such as UV and e-beam lithography (top-down techniques) to produce intricate patterns for integrated circuits. The main drawbacks are the tremendous waste produced per deposition cycle, expensive raw materials (high purity gold), expensive high vacuum and temperature components. The list of materials that can be deposited using this technique is exhaustive. During this study it was used for the deposition of contact metals such as Au, Pd, Ti and Ag for TiO_2 nanowire devices.

The principle of PVD involves supplying enough energy to the target material to vaporise it. Energy is supplied to the material thermally by heating the material in a special crucible or by rastering an electron beam directly on the material to be vaporised. The vapour then condenses on the substrate (and the entire chamber) leaving a thin film of material on the surface. The substrate itself can be heated to promote diffusion of the condensed atoms on the surface which produces a smoother film.

Advantages of electron beam PVD (EBPVD) compared to thermal evaporation include low chamber contamination, higher deposition rates, more materials flexibility and higher maximum temperature [9]. EBPVD is a line of sight deposition method, meaning only samples directly above the vaporised material will deposit on the sample. Once the impingent vapour consisting of individual atoms or groups of atoms comes into contact with the surface it will move about the surface to an area of low activation energy site for nucleation. Further atoms impingent (adatoms) are incorporated into the nucleation sites as individual crystal growth proceeds. A structural reorganisation transition may occur to lower energy in the system once the film reaches a certain size but this is heavily surface/material dependent. The deposited material is typically amorphous or polycrystalline and is not well adhered to the surface. To combat this the substrate is often heated in an effort to increase the diffusion rates of adatoms allowing them to find a growing crystal before they condense and seed a new crystal. To combat delamination of poorly adhered films the substrate can be ionized with an ion gun breaking some bonds of the surface atoms such that they then bond with adatoms. Additionally an intermediate layer or adhesion layer can be deposited on the surface prior to deposition of

the material of interest. The adhesion layer is chosen such that it is well adhered to the substrate surface but also so the material of interest will adhere well to it.

2.5.2 Sputter Deposition

Sputter deposition is a popular physical vapour deposition method used for producing thin films. It is principally used to coat insulating objects in a thin film of metal for SEM imaging to prevent charging. The method can also be used to coat cutting tools for wear resistance and to deposit reflective coatings on transparent substrates or glass. The various elements of a magnetron sputter coater used in this study are shown in Figure 2.7. Its mode of operation is similar to that of a diode plasma device except with the addition of a static magnetic field present at the cathode generated by a permanent magnet. By applying a sufficiently large voltage across the electrodes an inert gas (Ar) within the vacuum chamber will break down into a plasma. Ions are accelerated across the potential and strike the target material at the cathode. The ions strike the surface of the target material with energy ranging between 60 - 1000 eV (in the knock-on energy regime), a range is practical for most sputtering uses. Higher energies become impractical for sputtering use due to the large voltages required. At energies above 50 keV the incident ion particle has sufficient energy to penetrate the surface of the target material resulting in ion implantation with little or no sputtering.

In the knock-on energy regime the incident particle has sufficient energy and momentum to break the bonds of the target surface atoms and dislodge them from the surface. Any atom removed from the surface by this interaction is considered to be sputtered. Secondary electrons can be created and emitted from the surface as a consequence of this high energy interaction. The static magnetic fields at the cathode captures these electrons at the surface of the target producing the so called 'racetrack'. The electronic and magnetic field are calibrated in such a way that these electrons drift perpendicular to both the E and B fields using an effect known as the Lorentz force. Electrons captured in this drift can ionise more gas with the advantage that ions created in this drift region have a high probability of striking the cathode. This effect results in greater sputtering efficiency when compared to diode or rf sputtering [10].

The film thickness is monitored in real time during deposition using a quartz crystal microbalance. The quartz crystal is coupled to an electric circuit within the sputter device that causes it to vibrate at its resonant frequency. As material is deposited onto the microbalance the mass per unit area on the microbalance changes causing a shift in the resonant frequency

of the crystal. This shift in resonant frequency is then correlated to a thickness change based on the rate of arrival of material and its density. The accuracy of the microbalance depends on the density of the deposition material, for instance Au (ρ – 19.3 g/cm3) will alter the resonant frequency ~ 150 Hz per nanometer of material deposited. Al (ρ – 2.7 g/cm3) however has a much less pronounced resonant frequency shift ~ 20 Hz per nanometer.

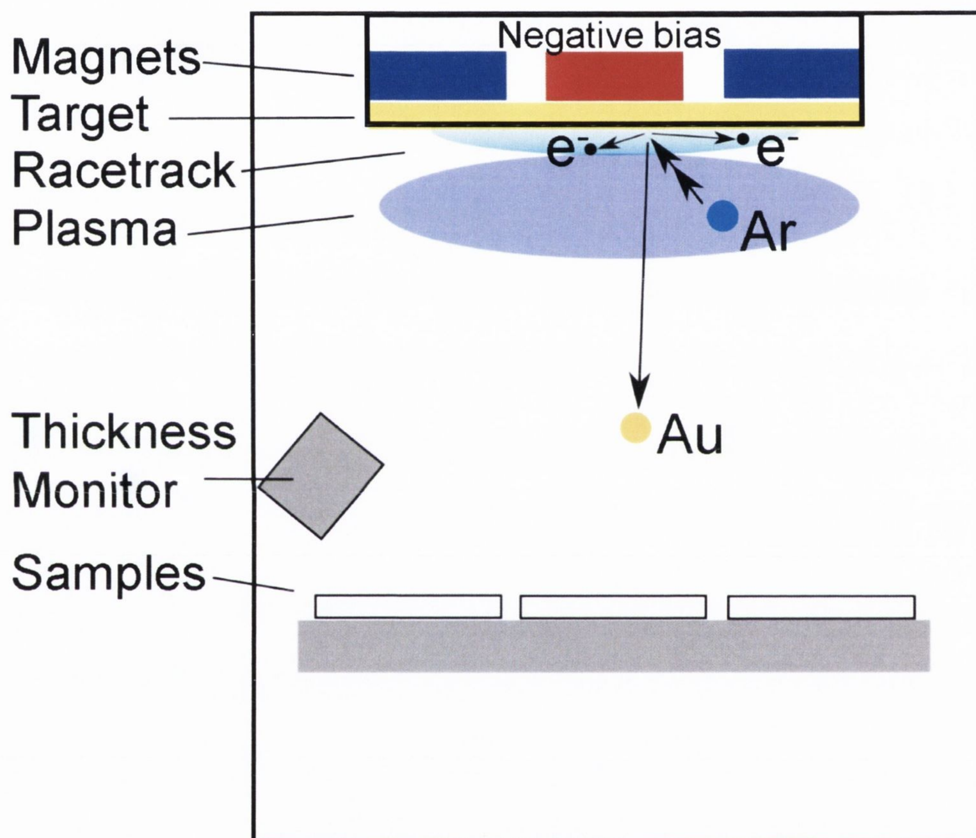


Figure 2.7. Schematic illustration of the sputter deposition process. Argon gas (Ar) is ionised under a large negative bias and directed to the target bombarding it, exchanging energy and momentum with the surface atoms of the target. The bombardment process ejects target atoms (Au) from the surface of the target creating the deposition material. The permanent magnetics capture and confine secondary electrons created from the impact collision in a drift racetrack around the surface of the target which increases plasma density.

2.5.3 Spray Deposition

Spray deposition is a simple technique used to deposit nanomaterials on a substrate [11]. It has the advantage of being cheap and robust. With a modest time investment in parameter optimisation of spraying conditions, high quality films of nanoparticles are readily produced. Firstly a dispersion of the nanomaterial is made. The solvent and particle concentration will determine the quality of the final film as well as the spray time required. The dispersion is then nebulized with a common hand spray gun. Ideally, each droplet of the sprayed dispersion will contain only one nanoparticle. This is optimised by varying the back pressure used to spray the dispersion. Furthermore the evaporation rate of the solvent will be quicker than the spray rate such that droplets do not accrue additional material and become subject to capillary drying effect. These drying effects are undesirable as they produce non-homogenous films. Volatile solvents such as propan-2-ol (IPA) are typically used for spraying. Substrate heating (140 °C) is required when using a water solvent however. The technique can be compared to other inexpensive deposition methods such as drop casting, dip casting and spin casting. Drop and dip casting methods are perhaps the most accessible method as they require no special apparatus. These methods however are susceptible to drying effects heavily dependent on capillary forces [12]. The familiar 'coffee ring' pattern is reproduced as a result of these forces even at the nanoscale, which is not desirable. Spin casting is the act of drop casting material on a substrate then spinning the droplet to promote droplet coverage and even solvent evaporation. It has been demonstrated that a fine film of Ag nanowires can be produced using this method in a short time with low rpm <1000 [13].

2.6 References

1. Williams, D.B. and C.B. Carter, *Transmission Electron Microscopy: A Textbook for Materials Science*. 2009: Springer.
2. *SEM Overview*. Available from: http://www4.nau.edu/microanalysis/microprobe-sem/instrumentation.html.
3. Zhou, W. and Z.L. Wang, *Scanning Microscopy for Nanotechnology: Techniques and Applications*. 2007: Springer.
4. ; Available from: http://www.microscopy.ethz.ch/TEMED.htm.
5. Hovington, P., D. Drouin, and R. Gauvin, *CASINO: A new monte carlo code in C language for electron beam interaction —part I: Description of the program.* Scanning, 1997. **19**(1): p. 1-14.
6. Orloff, J.H. and L.W. Swanson, *Study of a field-ionization source for microprobe applications.* Journal of Vacuum Science & Technology, 1975. **12**(6): p. 1209-1213.
7. Kim, C.-S., S.-H. Ahn, and D.-Y. Jang, *Review: Developments in micro/nanoscale fabrication by focused ion beams.* Vacuum, 2012. **86**(8): p. 1014-1035.
8. Giannuzzi, L.A. and F.A. Stevie, *A review of focused ion beam milling techniques for TEM specimen preparation.* Micron, 1999. **30**(3): p. 197-204.
9. Singh, J. and D.E. Wolfe, *Review Nano and macro-structured component fabrication by electron beam-physical vapor deposition (EB-PVD).* Journal of Materials Science, 2005. **40**(1): p. 1-26.
10. Kelly, P.J. and R.D. Arnell, *Magnetron sputtering: a review of recent developments and applications.* Vacuum, 2000. **56**(3): p. 159-172.
11. Scardaci, V., R. Coull, and J.N. Coleman. *Spray deposition of Silver Nanowire transparent conductive networks*. in *Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*. 2012.
12. Deegan, R.D., et al., *Capillary flow as the cause of ring stains from dried liquid drops.* Nature, 1997. **389**(6653): p. 827-829.
13. Chung, C.-H., et al., *Solution-processed flexible transparent conductors composed of silver nanowire networks embedded in indium tin oxide nanoparticle matrices.* Nano Research, 2012. **5**(11): p. 805-814.

Chapter 3

Surface Energy Driven Growth: A General Introduction

3.1 Introduction

The advanced processes used today in nanotechnology fabrication can be broken down into roughly two categories, the so called 'top down' and 'bottom up' approaches. Many of the top down fabrication techniques that exist as nanofabrication methods including electron beam lithography (EBL), physical vapour deposition (PVD) and etching techniques are the extension of technologies first developed for use in the micron-scale electronics before nanometer scale transistors were developed but operate on the similar principles. Lithography is used to define a pattern or mask in a resist which is then selectively removed by a solvent. Successive steps of etching and metal deposition through the mask then develop the nanostructures of the device that define its function [1]. The second approach for nanofabrication – the bottom up approach, requires significantly less costly equipment to perform (in contrast to top down techniques) which is attractive for small scale synthesis and research projects. In this approach atoms or molecules provide the building blocks for defining features on the nanoscale. Bottom up synthesis techniques leverage physical growth phenomenon such as phase separation and self-assembly to produce various nanoparticles and allotropic nanostructures [1]. Popular bottom up approaches include the vapour-liquid-solid (VLS) technique and solution phase or colloidal synthesis both of which can be applied successfully to produce sub 100 nm particles.

Despite these established techniques there remains a niche in metal nanoparticle synthesis that neither top down nor bottom up approaches can address. Namely a facile synthesis method that facilitates the production of single crystal metal nanoparticles whose size and shape can be readily controlled without the need for further post synthesis isolation and re-deposition steps. In this chapter the surface energy driven growth (SEDG) method is introduced in the context of a novel bottom up metal nanoparticle synthesis technique that can address the shortcomings

of metal nanoparticle synthesis. The theory behind some distinctive features of the SEDG method including film breakup, dewetting, agglomeration and crystal nucleation are presented in a general introduction to the growth method.

3.1.1 Nanoparticles

Throughout history there are many examples of what are now know as gold nanoparticles used in ancient artefacts such as stained glass windows and lustrous ceramic pots. They were used as a unique dye to add a special red hue. In Roman times the ability of gold nanoparticles to scatter red light was wonderfully captured by the craftsman of the Lycurgus cup (Figure 3.1) [2]. In a distinctly nano-phenomena the Lycurgus Cup appears green in natural daylight but a special red glow emanates from the cup when light is transmitted from inside the vessel. At the time craftsmen used an empirical recipe of mixing certain materials together to produce the nanoparticles they used in their works. In the eighteenth century Michael Faraday accidently synthesised colloidal gold nanoparticles during his experiments. By the end of the 1850's Faraday was able to synthesize colloidal gold reproducibly using a more scientific approach in what was perhaps the first intended nanoparticle synthesis [3].

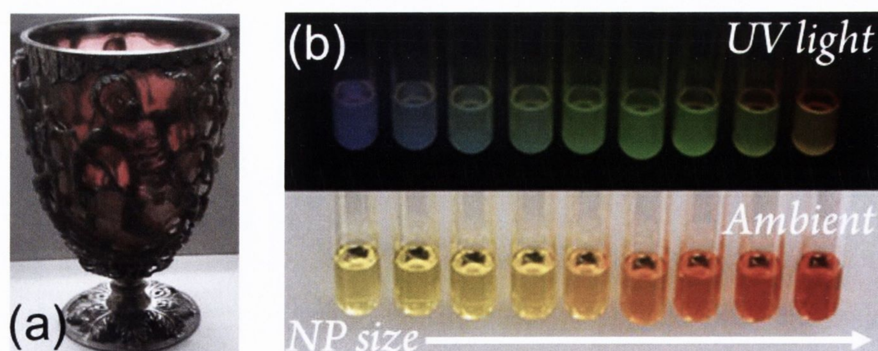


Figure 3.1 The size of nanoparticles dictates how they interact with light and determines their colour. (a) The Lycurgus Cup appears red when light is transmitted through the cup due to the interaction of light with Au nanoparticles embedded in the glass. (b) CdSe nanoparticles of different size also display different colours in UV light and ambient light depending on their size.

It is now known that the effect Faraday and the craftsmen long ago witnessed was due to the nanoparticles size. Its size limited the ability of surface electrons to responds to incident light which enabling it to more efficiently scatter red light (~700 nm) [4]. The effect is known as surface plasmon resonance and it is quite pronounced in silver, platinum as well as gold nanoparticles [5]. It is an example of the many new phenomena nanomaterials display strictly due to their size. To date there are many examples of nanoparticles improving the quality of life in all aspects of science including biology, material science, semiconductor devices, optical waste treatment and even sun cream.

There is a wealth of top down and bottom up approaches to nanoparticle synthesis. The method of synthesis is dictated by the end function or application of the nanoparticle. Introducing and discussing the merits of all synthesis techniques is beyond the scope of this chapter. However the two main methods for nanoparticle synthesis, namely colloidal synthesis and VLS growth will be introduced.

3.1.2 Colloidal Nanoparticle Synthesis

Colloidal systems are defined as systems with particles dispersed in a medium of critical dimensions between 1 nm – 1 um. Colloidal synthesis is therefore a rather broad term that captures many areas of synthesis. More relevant to nanoparticle synthesis are hydrothermal and solvothermal methods. Hydrothermal synthesis refers to a chemical synthesis that takes place in water solvent above its boiling point while solvothermal growth refers to chemical reactions taking place in a non-aqueous solution such as Propanol. Both can be carried out a high temperature 100-1000 °C and pressure 1-100 MPa. At elevated temperature and pressure many aspects of the chemical reaction are enhanced such as higher solubility of solute and inorganic precursors as well as increased diffusion rates. These attributes allow certain chemical reactions to proceed favourably to produce a crystal solid product.

In a typically solvothermal synthesis a precursor molecule containing the desired element is added to a solution. The element must then be dissociated from its parent molecule and reduced to atomic species. There are various methods to achieve this in solution including metal salt reduction, thermal decomposition, photochemical methods, ligand reduction and electrochemical means [6]. Once the atomic species are produced in solution they must be stabilised against aggregation through their individual Van der Waal interaction. This can achieved through electrostatic stabilisation or steric stabilisation. Charged ionic species can be

introduced to the reaction solution medium such that they absorb onto the nanoparticles, Figure 3.2 (a). They then create an electrical double layer which repels two nanoparticles from each other by a repulsive Coulombic interaction. Steric stabilisation is the act of coating the nanoparticles in a material, typically a polymer to prevent aggregation. The long polymer chains attached to the nanoparticles act as a physical barrier that prevents two particles from coming within a critical distance of each other. Both these methods serve to stabilize atomized or growing nanoparticles in the solution medium.

Capping agents or surfactants can also be used to dictate/direct crystal growth of the nanoparticle in solution as shown in Figure 3.2 (b). Under thermodynamic equilibrium and without surfactants the shape of a nanoparticle is determined by its lowest energy crystal surface, typically (111,110 and 100) for metals. Using Wulff construction it is possible to estimate the shape a particle will adopt using knowledge of the surface energy values of the low index crystal planes of the growth material. Each crystal plane has a separate kinetic impact on the growth dynamics of the particle. Before they are incorporated into the crystal lattice adatoms are adsorbed onto the particle and move about its surface. The adatoms movement is relatively slower on low energy crystal planes in comparison to higher index planes. This results in the rapid growth of the high energy crystal planes thus exposing the lower energy planes on the boundary of non-growth directions Capping agents and surfactants alter the surface energy of the particle crystal planes by themselves adsorbing onto the surface. Their adsorption creates a stabilisation of the higher energy crystal planes changing the growth kinetics and also the shape of the grown particle [7]. This effect has been shown in great detail for silver nanoparticle synthesis, producing a great variety of particle shapes with unique physical properties [5].

Colloidal synthesis is an attractive method for chemists because there is great opportunity to tailor the parameters of a reaction process. Macroscopic parameters such as temperature and pressure influence the growth rate of the particles. Changing factors such as precursor, surfactant and stabilizer concentration may alter the final shape and size of the nanoparticle produced. Another strength of the method is the relatively low capital cost in the equipment and chemicals. These factors combine to make it a readily accessible method for research groups as well as industry. The list of nanoparticles produced via this method is exhaustive. Nobel metals such as Au, Ag, Pd and Pt were the first particles produced using colloidal synthesis. Transition metals, transition metal oxides, magnetic materials, semiconductor and alloy nanoparticles have all been produce successfully via this method.

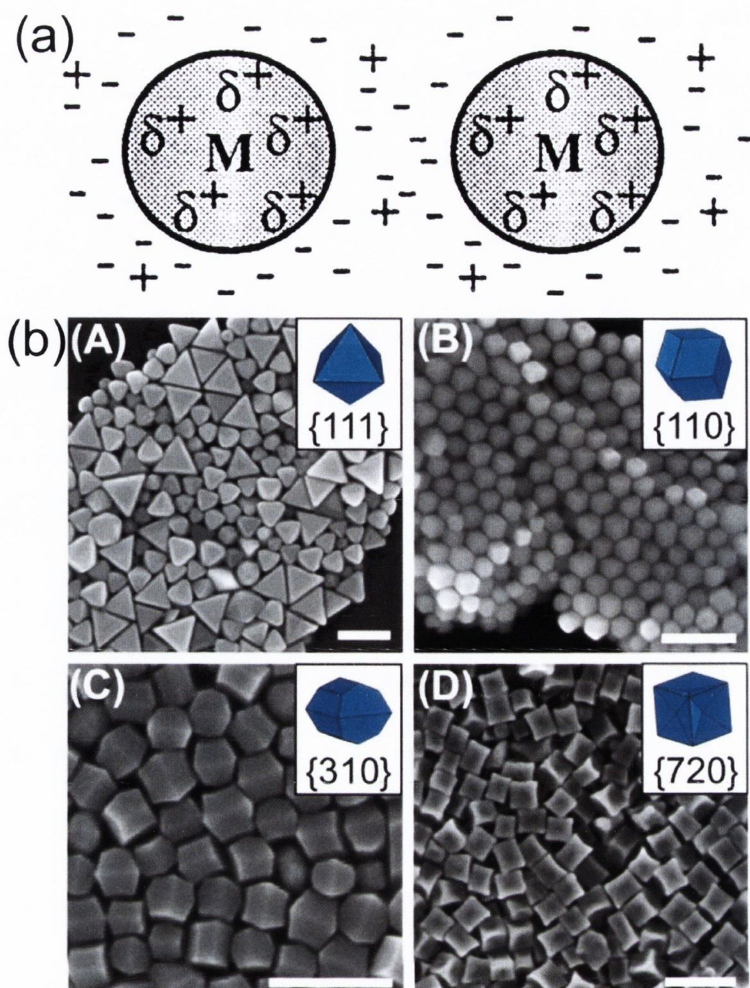


Figure 3.2 Colloidal nanoparticle growth. (a) Two metal ions (M) in solution are stabilised electrostatically against aggregation by ions adsorbed onto their surface [6]. (b) Au nanoparticles are grown with different shapes and crystal facets by varying the concentration of Ag^+ ions in solution, scale bar 200 nm [8].

It is difficult to capture the wealth of potential applications of colloidal nanoparticles. They are currently applied in many diverse fields such as healthcare, lab on chip screening devices, catalysis, electronic devices, surface coatings, advanced materials and photovoltaics. Despite these applications there remains inherent difficulties with the method. The main drawback from colloidal growth is that nanoparticles in solution are not very useful. They must be incorporated into an integrated structure before their properties can be leveraged to produce a novel technology. The first problem is particle size dispersion. While tight size dispersions are known in systems such as Au and Ag the majority of nanoparticles produced via this method have sizes up to 100s of nm from that of the mean size. This introduces an additional isolation/filtering step to selectively collect the required size of nanoparticle. Once isolated

they must be used in conjunction with a top down fabrication technique to precisely grab and position them within a structure which can be prohibitively difficult. As a result the main applications of nanoparticles continues to be based on their enhanced optical response in various biological solutions including blood through light interrogation.

3.1.3 Vapour-Liquid-Solid Growth

VLS growth was first presented in 1964 by Wagner and Ellis as a mechanism for describing the growth of Silicon nanowires (originally referred to as whiskers) with a Gold droplet present at the top of the structure [9]. They attributed the role of the Gold droplet to act as a preferential sticking nucleation site for the growth of Si crystals however the role of the Au catalyst in VLS growth is still debated today. A schematic depicting the central aspects of VLS is shown in Figure 3.3. Typically the synthesis is carried out at temperatures above the eutectic temperature of the constituents that make the binary alloy (for Au-Si alloy T_{growth} >363 °C). Precursor wire growth material is supplied to the reaction chamber in the form of a gas (or vapour) at a high flow rate (~1500 sccm). The precursor gas decomposes into the basic growth atoms which are absorbed into the liquid metal catalyst (usually Au) saturating the droplet. By maintaining a steady supply of growth material to the reaction chamber the metal droplet can become supersaturated with growth atoms ultimately resulting in the growth of crystals within the droplet. Nanowire growth then continues at the droplet-wire interface. Over the last 50 years tremendous advances have been made in expanding in the breath of anisotropic materials that can be produced by the method including elemental semiconductors [10, 11], II–VI semiconductors [12, 13], III–V semiconductors [14, 15], oxides [16, 17], nitrides [18] and carbides [19, 20].

Theory behind the growth mechanism has also been greatly developed over the years. Growth is believed to proceed via the decomposition of precursor molecules to produce the growth - species. The decomposition of the precursor is understood to be facilitated by the liquid droplet which then forms a eutectic alloy with the decomposed precursor material. However wire growth can proceed without the presence of a liquid droplet, indeed Wagner et al. were able to demonstrate that the activation energy for the growth of their whiskers with Au particles was the same as that for growth of Si without Au [21]. Such an observation does not support the catalytic role of the liquid droplet in VLS thus the liquid droplet is believed to provide an enhanced accommodation coefficient relative to the bear substrate promoting local surface

saturation of the droplet. The droplet then becomes enriched beyond the solubility limit of the liquid alloy facilitating precipitation of the wire material on the droplet/substrate interface. The liquid droplet remains at the top of the growing wire for the duration of the synthesis or until it is consumed [22]. The formation of a liquid alloy droplet is central to VLS growth but describing the kinetics of the droplet saturation/growth process becomes more complicated for two component wires such as GaAs or ZnO.

The great variety in materials grown using VLS was listed above however there remains an absence of published data on the application of VLS to produce metal anisotropic structures. The high melting temperature of metals is a direct consequence of their high surface energy making their incorporation into VLS unpractical. Issues with alloying with the Au catalyst may arise in the absence of a shared eutectic point with the metal vapour. While a another bottom up approach known as atomic layer deposition can be used to produce thin metal films with low index orientations - high vacuum, high capital cost and low throughput make it a poor a candidate for a bottom up method to synthesise single crystal metal nanoparticle prepositioned on a substrate.

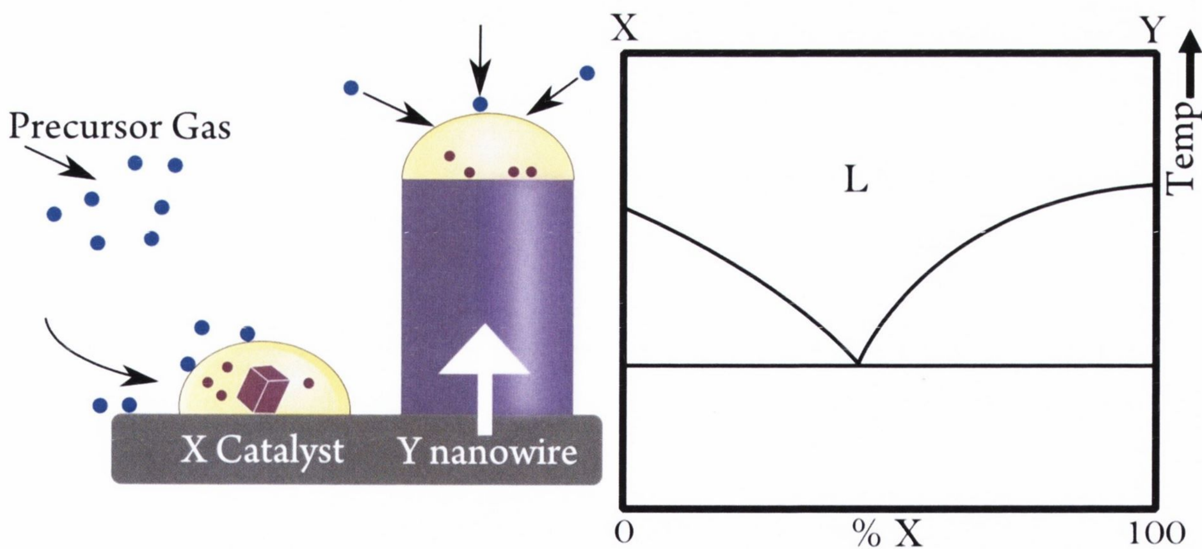


Figure 3.3 Schematic illustration of the VLS growth of nanowires using a liquid metal "X" catalyst with the corresponding X-Y binary phase diagram. Precursor material containing Y molecules is continuously supplied to the reaction chamber in the form of a vapour which decomposes into Y growth species on the catalyst. Continued saturation of the catalyst enables nucleation and growth Y nanowires. Growth temperature is usually carried out at temperatures above the eutectic temperature determined by the lowest temperature at which the liquidus exists before separating out into individual X and Y components.

3.2 Features of the Surface Energy Growth Method

The method was first introduced by Jung et al for the Au-Ge system when it was discovered that heating thin films of Au and Ge at their eutectic temperature produced small heavily faceted particles and some extremely long nanowires ~ 20 um in length [23]. The two materials form a binary alloy system with a eutectic temperature of ~ 350 °C. The system is commonly investigated for the VLS synthesis of Ge nanowires [24] using Ge precursor gas flux in the presence of a nanoscale Au film. It was therefore unexpected that Au nanowires should form upon heating a bilayer Au-Ge films. Heating the bilayer films resulted in a familiar pattern known as spinodal dewetting, forming agglomerated liquid phase particles. Many of the wires were observed to sprout from these agglomerated particles suggesting they were behaving as nucleation and crystal growth centres for the newly formed wires, in a manner similar to that of VLS. It was demonstrated that introducing ion beam lithography defined holes into the film prior to annealing made it possible to have a degree of control over the positioning and growth of the subsequent wires. The phenomena was introduced as 'agglomeration waves' but the physical origin behind them was not understood at that time. A discussion of the physical origin of these 'agglomeration waves' is presented in this chapter to developed the new insight developed over the course of this project. This includes using our understanding of these waves to better predict film breakup, crystal positioning and growth. The merits of the method will be discussed in light of its accessibility and potential for research in fundamental nucleation kinetics and morphology evolution measurements were performed in real time using a hot stage SEM platform.

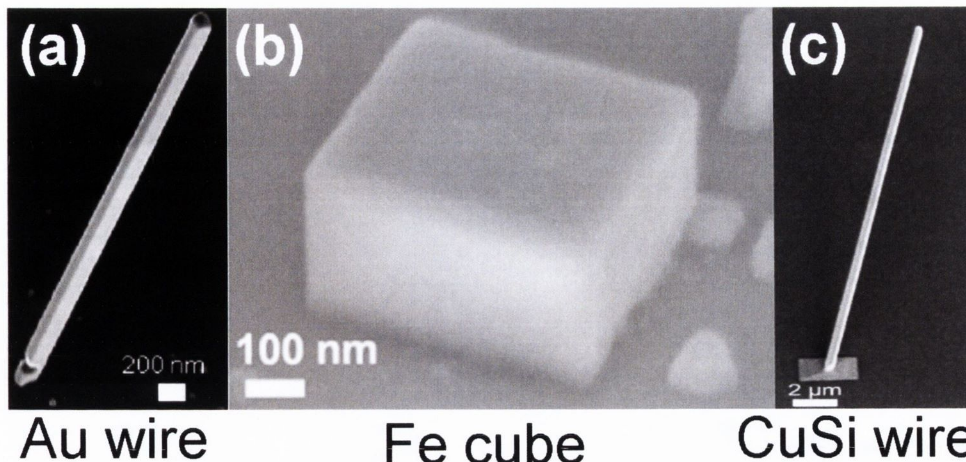


Figure 3.4 Three nanoparticles grown via the SEDG method. (a) Au single crystal nanowires grown with use of 'agglomeration waves' but not fully understood at the time [23]. (b) Single crystal Fe nanocubes [25]. (c) Cu_3Si nanowires [26].

3.3 Generalisation of SEDG Method

To introduce the details of the method we will apply the SEDG method to the synthesis of a generic material X with the goal of producing a single crystal X nanoparticles prepositioned on a substrate. Before experimental sample preparation begins the relevant physical properties of X must be collected and reviewed for SEDG suitability. The list of important parameters is described in the flow chart below - Figure 3.5 The most critical parameter in determining candidate materials is the surface energy of its most stable crystal plane (the crystal plane with the lowest surface energy value). This value will determine the ultimate shape of the crystal X as prescribed by Wulff construction of the nanoparticle. For low index crystal planes such as <100>,<110> and <111> the final form of the crystal formed will be square, pyramidal and wire like respectively under equilibrium conditions. The next step in the design flow is finding a suitable alloy material for X. The surface energy of X must be greater than that of the alloying material Y for SEDG to be realised. Computational and experimental surface energy values of

different materials along with their various crystal index planes are readily available throughout the literature [27].

The nature of the X-Y alloy is then scrutinized for the presence readily accessible eutectic points in the binary alloy phase diagram. The eutectic point represents a special point in the X-Y binary alloy phase diagram where a set composition of the alloy melts and freezes at one temperature. This temperature is typically well below that of the melting point of the individual X and Y components. It is attractive from a process point of view because it allows the alloy to melt to form a liquid at 100's C temperature instead of 1000's C. Finding a suitable alloy candidate with a eutectic point in the binary phase diagram is perhaps the most constraining factor for materials synthesis via this method. The literature remains limited in the breath of binary alloy phase diagrams or each combination of material X with rest of the elements. This is a consequence of the way binary phase diagrams are produced, through empirical data. The lack of binary alloy phase information may be offset by modelling and computer software which may help identify relevant eutectic alloy candidates for material X. It is worth mentioning that the nature of the binary phase diagram must be relatively simple. An overly complicated binary phase diagram with multiple eutectic points could potentially inhibit or frustrate the formation of the single crystal X nanostructure.

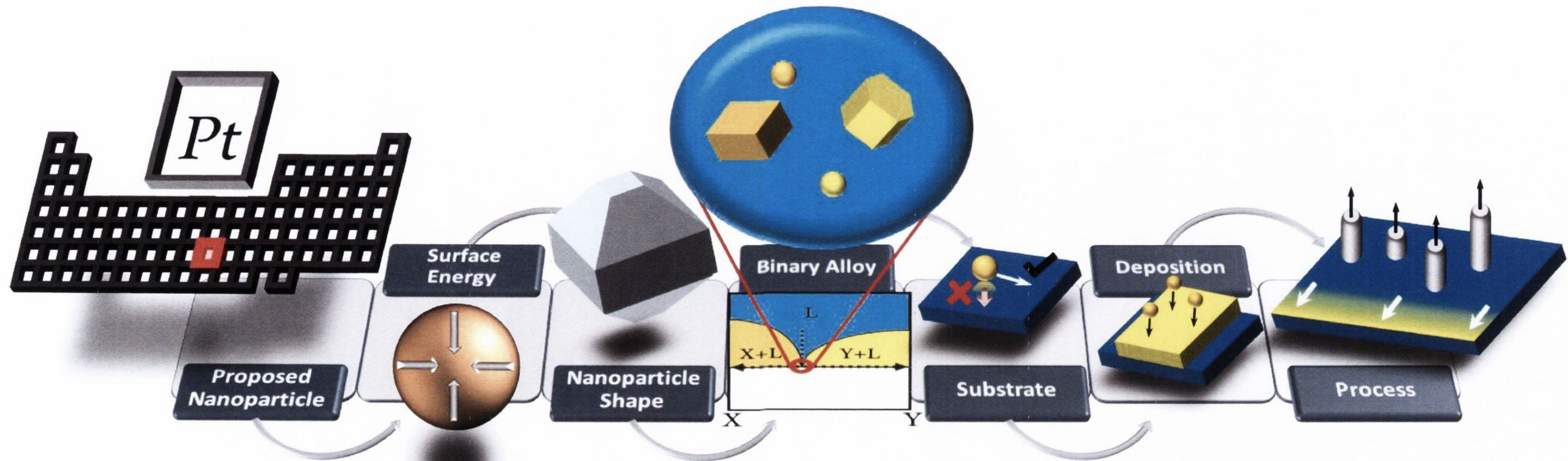


Figure 3.5 SEDG process flow chart depicting the various major stages involved in growing nanoparticles using this method. Step 1 - Involves choosing a material to grow via SEDG. Transition metals should be easily produced by this method and although not pursued in this study it may be possible to synthesize some alloy nanomaterials also. Step 2 - Involves collecting pertinent physical data about the candidate material. The most important of which is the surface energy of the material as it has an impact on the liquid dynamics and nucleation later in the process. Step 3 - The shape of the nanoparticle produced with SEDG is determined by the lowest surface energy crystal facet of the material. Using Wulff construction will allow the final shape of the particle be determined at this point in the process. Step 4 - The binary alloy candidate is now chosen for the nominated primary material. This is the most restrictive step in terms of accessibility to binary alloy phase diagrams. The candidate alloy material must have lower surface energy than that of the primary material. The binary alloy phase diagram also must contain a simple and accessible eutectic point. The eutectic point sets the process temperature which is chosen to be close the eutectic temperature of the two materials. Step 5 - A substrate is chosen to fill two criteria, the first is that its surface energy is lower than that of the two alloy components and also that of the liquidus alloy they will form. This promotes dewetting of the liquidus alloy, a crucial step prior to nucleation. The second is that it should be inert. This is required to stop detrimental etching of the substrate by the alloy materials. However as shown for the case of Cu_3Si substrate etching can be used to facilitate growth. Step 6 - Deposition of each alloy component can be performed by a variety of methods. Deposition methods that introduce defects into the film such as grain boundaries will help to promote dewetting and agglomeration. Step 7 - At this point prior to annealing the sample other top down processes such as FIB lithography can be used to introduce defects into the films. These defects can control and help position the growth of the nanoparticles.

3.4 Thin Film Stability

The final design stage prior to sample preparation is to choose the substrate such that the liquidus eutectic alloy of X-Y is morphologically unstable. This will promote film breakup followed by agglomeration. The morphological stability of a thin liquid film to breakup (dewet) or remain covering (wet) a given substrate is determined by the surface energy of the liquid film relative to the substrate. Youngs equation (3.1) is used to gauge the stability of liquids on a substrate either by directly measuring the equilibrium contact angle (θ_{CA}) the liquid makes with the substrate or by estimating it using the surface energies of the three interfaces.

$$\cos\theta_{CA} = \left(\frac{\gamma_{SV}-\gamma_{SL}}{\gamma_{LV}}\right) \tag{3.1}$$

Where γ_{SV}, γ_{SL} and γ_{LV} are the surface energies for the solid-vapour, solid-liquid and liquid-vapour interfaces, Figure 3.6 (a) depicts a liquid droplet on a substrate and the various elements of Young's equation. The equilibrium contact angle is used to estimate the tendency of a liquid to dewet a surface. By convention a large contact angle implies a greater tendency for the liquid to dewet the substrate. The value of contact angle may be interpreted as the liquids tendency to undergo a morphological transition from a film to an agglomerated/islanded state. Data on the surface energy of the eutectic liquidus alloy is extremely rare in almost all binary alloy liquids. This makes it difficult to predict the contact angle and therefore the stability of the liquidus eutectic alloy on a substrate. In the absence of this data using a very low surface energy substrate such as SiN, SiO_2 and Al_2O_3 can promote dewetting of the liquidus alloy. It is also helpful to choose the substrate such that it is the lowest surface energy system relative to material X and material Y.

For common liquids with a high contact angle the transition from film to islands/droplets is almost instantaneous. However such a transition in ultrathin liquid films at high temperature is an activation process that involves fluctuation in the film to drive the morphological transition. A thin liquid film represents a morphologic metastable state [28]. It has been shown that ultrathin films of silicon <50 nm are morphologically unstable when heated on silicon dioxide substrates with an estimated liquid contact angle of ~73° [29, 30]. In order to undergo the morphological transition from a wetting film to a dewetting agglomeration state a substrate-exposing perturbation is required.

This perturbation refers to the formation of a void via a fluctuation in the thickness of the thin film exposing a region of the low energy substrate. When the size of this region reaches a certain critical length (r_{crit}) there is a decrease in free energy as the void grows ($r_{void} > r_{crit}$). The activation energy required to nucleate such a void is estimated using the following equation (3.2) [30].

$$\Delta G_{void} = 2\pi r_{crit} t_{film} \gamma_{film} \quad (3.2)$$

Where ΔG_{void} is the activation energy for creating a void large enough to cause dewetting, r_{crit} is the size of the critical void ($r_{crit} = \frac{t_{Si}}{\sin \theta_{Si}}$), t_{film} is the thickness of the film and γ_{film} is the surface energy of the film. For Silicon on an Insulator (SOI) substrate, taking $r_{crit} = t_{film} = 1$nm, $\gamma_{Si} = 1.5$ J/m^2 the activation energy required to nucleate a critical void r_{crit}^{EA} ~ 60eV, such that homogeneous spontaneous nucleation of critical voids does not occur. Void nucleation therefore must be formed at either surface/film defects or film edges. Film edges represent pre-existing critical voids of infinite void thickness [30]. This film edge effect is leveraged during deposition to promote eutectic liquidus film dewetting - experimentally half covering X with Y material during deposition dramatically promotes dewetting at the film edge as seen in Figure 3.7. Intentionally milling I-beam defects into the XY thin film prior to liquidus alloy formation also promotes film rupture at that point.

This artificially introduced defect formation can be coupled with another thin film rupture mechanism driven by an attraction (predominantly Van der Waals) between the liquid film and the substrate to exercise greater control over the dewetting and agglomeration of the thin film. This spontaneous film rupture process is most strongly influenced by the thickness of the liquid on the substrate. Liquid surface perturbations occur spontaneously in the film and arise from thermal shock and vibration caused by external sources. Their interaction with the film introduces surface interfacial waves that have a characteristic wavelength λ. Any interfacial wave in the liquid causes a local change in thickness in the film, illustrated in Figure 3.6 (b), increasing the area of interfacial interaction between the film and substrate. The interfacial interaction is captured by the disjoining pressure Π (3.3) which can be thought of as a pressure applied at the boundaries of the film [31]. It is a function of the film thickness t and describes the intermolecular forces of interaction between the film and the substrate.

$$\Pi = \frac{A}{6\pi t^3} \tag{3.3}$$

Where A is the Hamaker constant. The disjoining pressure is used to derive the critical wavelength λ_{crit} for thin liquid film breakup given below (3.4).

$$\lambda_{crit} = \left(-\frac{2\pi^2\gamma}{\mathrm{d}\Pi/_{\mathrm{d}t}}\right)^{1/2} \tag{3.4}$$

The critical wavelength λ_{crit} is the shortest wavelength of an interfacial perturbation that satisfies the film rupture condition $\mathrm{d}\Pi/\mathrm{d}t > 0$ for a set film thickness. Its most general form is given in equation (3.5).

$$\lambda_{crit} = t^2\sqrt{\frac{c\gamma}{A}} \tag{3.5}$$

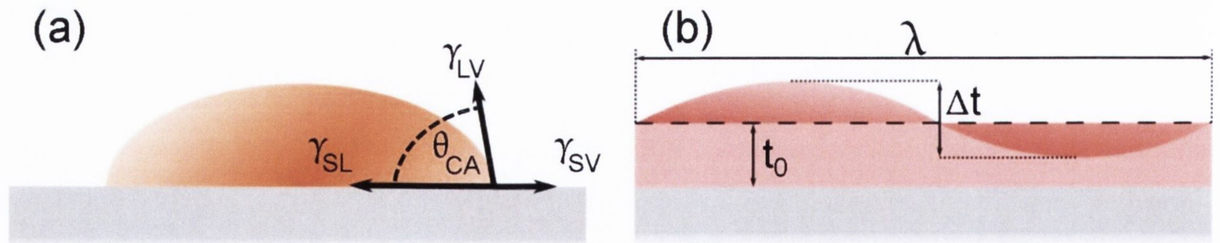


Figure 3.6 (a) The various surface energy interfaces and equilibrium contact angle considered in Youngs equation are shown. With γ_{SV}, γ_{SL} and γ_{LV} are the surface energies for the solid-vapour, solid-liquid and liquid-vapour interfaces and θ_{CA} is the equilibrium contact angle. (b) An illustration of a interfacial wave in a thin liquid film oscillating at a wavelength λ showing the change in film thickness Δt resulting from a perturbation, where t_0 is the initial film thickness. For any set thickness of an ultrathin film there is a range of wavelengths whose amplitudes will continue to grow resulting until $\Delta t > t_0$ causing film rupture.

Where c is a constant = $4\pi^3$ or 128π as derived by Vrij and Scheludko respectively [32, 33]. Perturbation wavelengths $\lambda \geq \lambda_{crit}$ are amplified resulting in spontaneous rupture of the film [34]. The critical wavelength tends to infinity when $d\Pi/dt = 0$, this condition is satisfied at the critical thickness t_{crit} where the film is stable against rupture by this mechanism. Equation (3.5) can be recast in a more simplified form.

$$t_{crit} = \left(\frac{A\lambda_{crit}^2}{c\gamma}\right)^{1/4} \tag{3.6}$$

Thus any liquid film thinner than the critical thickness described in (3.6), in the presence of an attractive interaction between itself and the substrate has a set of perturbation wavelengths which will be amplified leading to film rupture. The fastest growing perturbation wavelength is one slightly longer than the critical wavelength. While all wavelengths longer than the critical wavelength can cause film rupture not all wavelengths are likely to form [35]. Longer wavelengths have a greater driving force but require more of the liquid to be displaced encountering more viscous friction while shorter wavelengths encounter less viscous friction but have less driving force resulting in low liquid flow speed.

These interfacial waves are the physical origin of the agglomeration waves Jung *et al* first observed during processing [23]. Figure 3.7 (a), (b) captures how I-beam lithography can be used to dictate growth. The critical wavelength for film rupture can be calculated for a set thickness of thin film. Fingerprints of these wavelengths are observed post annealing as shown in Figure 3.7 (c) for a 20 nm thick film composed of 10 nm Au / 10 nm Ge. Using the I-beam milled points as the center, the distance from the center to the agglomerated crystal structures forms a circle of diameter 10 μm. This value is close to the calculated critical wavelength of 15 μm for a 20 nm thick AuGe film (Liquidus AuGe alloy $\gamma_{AuGe} = 1.1$ [36], J/m^2 $A = 10^{-20}$ J [37], $c = 124$). Interpreting this range of wavelengths in the context of controlling the dewetting process is a challenge, however it may be used to construct an I-beam milling pattern in the film prior to annealing that can drive dewetting and agglomeration to maximise wire positioning and growth. Figure 3.7 (d), (e) captures how the calculated critical wavelength for a given film thickness may be used in cooperation I-beam milled features to enhance dewetting control. Milling into the deposited films such that the substrate is not exposed (as shown in Figure 3.7 (d)) introduces defects into the film which act as crystal nucleation points for growth. However, by milling to a depth to expose the underlying substrate the though hole acts as a

dewetting site as seen in Figure 3.7 (e). When partially milling into the bilayer film - without exposing the base substrate, the latter case predominantly results. Only partially milling through some of the bilayer requires much I-beam lithography parameter optimisation.

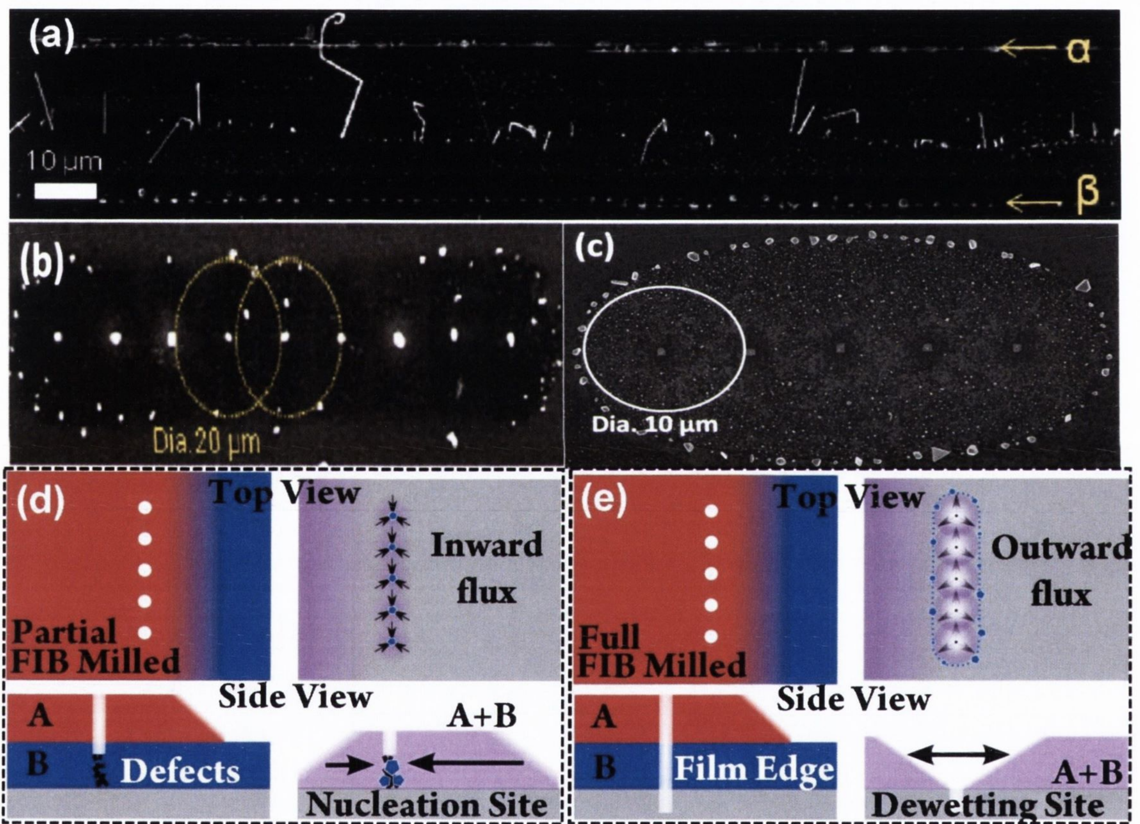


Figure 3.7 Interfacial waves as the origin of the agglomeration waves first observed by Jung et al [23]. (a) Two I-beam milled lines are used to direct dewetting in the bilayer film during annealing. (b) An array of partially I-beam milled holes act as crystal nucleation points for wire growth. (c) Full I-beam milled holes serve as dewetting sites. The ability of the holes to 'push' material about the substrate is given by λ_{crit} and can be roughly calculated using bilayer thickness, in this case for a 10 nm Au / 10 nm Ge bilayer the λ_{crit} is 15 µm. (d),(e) Schematics illustrating the difference between partially and full milled I-beam holes and the effect they have on dewetting during annealing.

3.5 Agglomeration & Crystal Nucleation

The role of surface energy in determining a thin films stability on a substrate as well as the dynamics of thin film break up have been discussed. These steps facilitate the formation of islands (droplets) on the chosen substrate. The islands share many similarities to the metal catalysts in VLS growth as they represent a low energy surface for adatoms and molecules to adsorb onto relative to the bare substrate. Nucleation and growth of the crystal phase nanoparticles proceeds in the islands which is driven by a reduction in free energy of the system.

Briefly, classical nucleation theory and the growth of a new phase is believed to proceed via collisions and the stepwise accretion of atoms to a growing nucleus until the nucleus is large enough and it continues to grow [38, 39]. The accretion and dissolution of particles to the nucleus is a dynamic in nature and can therefore be viewed as a statistical process. As a result there will be a distribution of sizes of unstable nuclei that form and an associated probability of each. Therefore it is easy to see that the simultaneous accretion of enough atoms or molecules to an unstable nucleus to make it stable against dissolution is highly improbable [38, 40]. The change in free energy relating to the formation of a stable spherical nucleus of radius r in a saturated system is determined by the sum of the energy change in surface free energy ΔG_S and volume free energy ΔG_V given below (3.7).

$$\Delta G = \Delta G_S + \Delta G_V \tag{3.7}$$

ΔG_S refers to the energy needed to create the surface on the solid phase in the growth medium and is defined as the surface area of the nucleus times the interfacial tension γ of the particle. ΔG_V is the energy needed to create the spherical volume of the nucleated particle and is equal to the volume of the nucleus times the associated free energy change ΔG_V which is negative in a saturated medium. An expression (3.8) for the change in free energy as a function of r is given by,

$$\Delta G = 4\pi r^2 \gamma + \frac{4}{3}\pi r^3 \Delta G_v \tag{3.8}$$

Both energy terms are a function of radius r. A plot of each term in (3.8) Figure 3.8 reveals how the two contribute to the overall free energy change as the size of the nucleus increases, mainly that ΔG_S is always positive and ΔG_V is always negative. There is a critical size (r_{Crit}) the nucleus must reach before the ΔG_V term overcomes the ΔG_S term which is dominant for nuclei smaller than r_{Crit}. Nucleus of the size (r_{Crit}) are deemed critical nucleus as any nucleus larger or equal to the size of the critical nucleus has an associated decrease in free energy as it grows.

When applied to the SEDG, classical nucleation takes place inside the islands that form after annealing the thin film to the liquidus eutectic temperature. Upon the initial breakup of the binary liquidus alloy its composition is assumed to be that of the eutectic. The size of the islands dynamically changes as accretion, dissolution and Ostwald ripening takes place. At this point the relative diffusion rates of the two materials X and Y becomes important. X-type adatoms of the material whose growth is desired can only saturate the droplet such that nucleation conditions are met provided they diffuse to the liquid at a greater rate than that of Y-type adatoms. Furthermore the high surface energy component segregates from the low surface energy component via Gibbs-Thomson pressure associated with growth from a high curvature surface (the liquidus island). With the saturation condition met, the composition of the liquidus alloy begins to change. This composition change can be followed on the XY alloy phase diagram in Figure 3.8. As the droplet becomes more saturated a critical nucleus forms within it. With continued heating growth of the nucleus can proceed and the single crystal nanoparticle forms. One advantage of SEDG is the ability to capture this crystal growth in real time gaining insight about nucleation theory as seen in the next section. In the final stages of crystal growth the size of the nanoparticles is determined by the amount of material deposited in the thin film. The upper limit of the binary film thickness is set by its stability. A very thick film will simply be to stable to rupture and undergo agglomeration. A unique feature of SEDG is the presence of a capping layer which surrounds the single crystal nanoparticle core which is similar in many ways to the metal catalysts that remain on top of nanowires grown via VLS methods. The SEDG capping layers are formed by the condensation of the liquidus eutectic droplet post annealing.

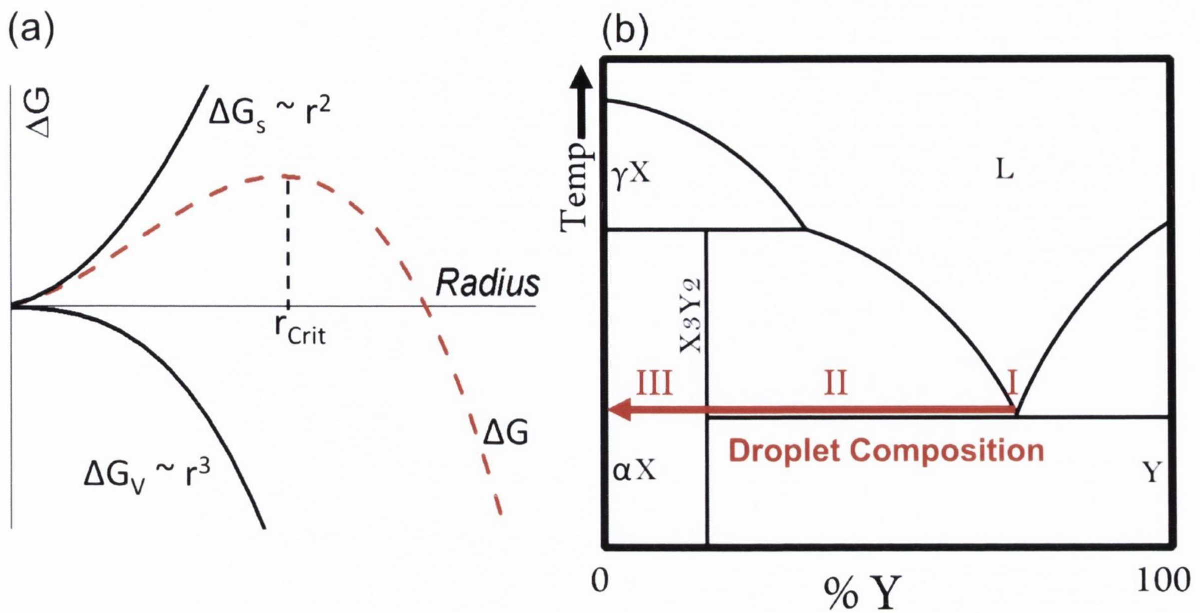


Figure 3.8 (a) Free energy change of a spherical nucleus as a function of its radius showing the contributions of each term in equation (8), ΔG_S and ΔG_V (solid lines), with a plot of the two terms together (dashed line) highlighting the presence of a nucleation barrier for nuclei with a subcritical size $r < r_{Crit}$. (b) XY binary alloy phase diagram depicting the change in droplet composition as X adatoms continue to saturate a liquidus droplet forming during annealing. At point I the composition is that of the eutectic, at point II the composition of the droplet is eutectic + X_3Y_2 and at point III only X_3Y_2 and single crystal αX remain.

3.6 Real Time Nucleation & Metastable Crystal Nucleus

There are several assumptions about the nature of critical nucleus in classical nucleation theory [41]. Most notably the shape of the particles formed are assumed to be spherical and that these nuclei are ordered in the same arrangement as the crystal phase that will eventually form. The growth process is also assumed to proceed in a stepwise manor which doesn't account for the possible combination of subcritical nuclei. Classical nucleation theory also fails to explain several nucleation phenomenon such as poor nucleation rates of crystals in undercooled liquids and gas phase nucleation in superheated liquids [42]. A two-step nucleation process was proposed in which the first step is the formation of aggregate clusters in solution followed by the nucleation of ordered crystalline solids within these clusters [43]. The formation of clusters or metastable nuclei is believed [44] to lower the free-energy barrier for the growth of the stable critical nucleus. A schematic representation of the two-step nucleation process is shown in Figure 3.9 (a). It describes a proposed alternate pathway for the formation of a critical sized nucleus via the combination of atoms in crystal shapes not representative of the final most stable nucleus. When the metastable nucleus approach r_{Crit} in size, it will transition into the final stable form of the growing nanoparticle.
Current methods used to investigate small cluster formation during nucleation include dynamic light scattering (DLS), UV-visible and X-ray spectroscopy. The direct observation of metastable states remains difficult owing to the transient nature and lifetime of metastable nuclei [45]. By heating the bilayer XY film on an SEM hotstage it is possible to monitor the growth of the nanocryrstals in real time with electron microscopy. As seen in Figure 3.9 (b) for the real time growth of Fe crystals via SEDG. The shape of the growing crystal changes rapidly from pyramidal to cubic through the course of the experiment - an observation that may support the two step nucleation process.

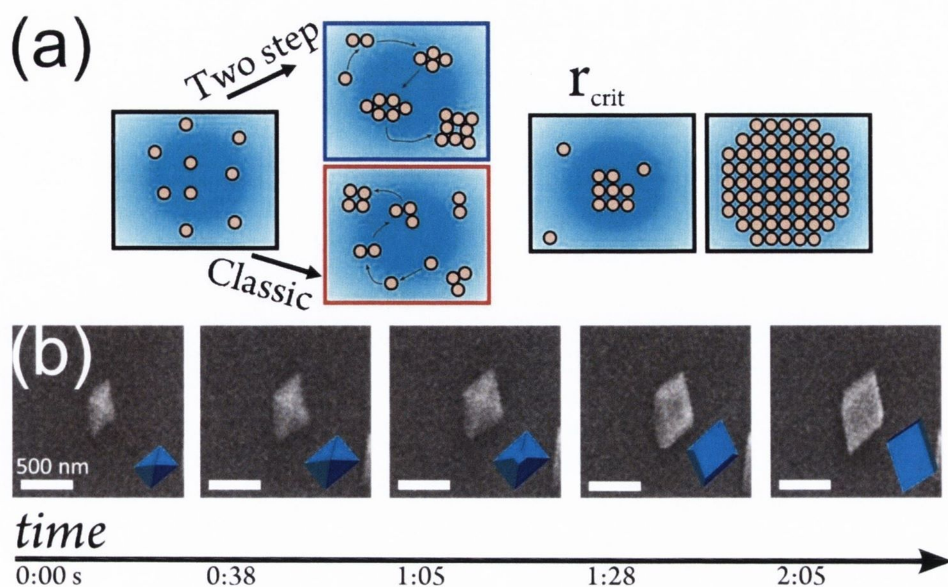


Figure 3.9 (a) A schematic describing each step in classical and the so called two step nucleation process. Classical nucleation is introduced as the piecewise addition of individual atoms to a growing nucleus whose shape is the same as the final stable nucleus. The two step nucleation process describes the piecewise addition of atoms to a growing nucleus that is meta-stable and transient. The role of the meta-stable nucleus is to facilitate growth up to a critical nucleus size where the metastable nucleus then transforms into its final most stable crystal shape for continued growth. (b) The growth of nanoparticles can be monitored in real time with SEDG using an SEM with a hotstage. The sequence of SEM images follows the evolution of an Fe crystal from its initial pyramidal crystal shape to that of a cubic crystal – the shape most stable for Fe crystals.

3.7 Summary and Outlook of SEDG

The SEDG method is a novel and inexpensive bottom up synthesis method for producing very large single crystal metal nanoparticles that can be prepositioned on a substrate. The method involves depositing two thin films of a binary alloy system and heating them above their eutectic temperature to form a liquidus alloy. The surface energies of the system are chosen to promote the liquidus eutectic breakup to allow saturation then nucleation to occur. The potential of SEDG may be unlocked when used in conjunction with top down fabrication techniques such as e-beam lithography or I-beam lithography to more accurately position growth of the nanoparticles. I-beam lithography has been shown to control dewetting of the liquidus film by either partially milling into the film prior to annealing creating defect sites or by milling through the film to act as pinning sites for the so call agglomeration wavefronts. The length of wavefronts can be calculated and therefore allow a milling pattern to be defined such that the dewetting of the film can be controlled for promoting nanoparticle growth. When heated on a hotstage in an SEM chamber the SEDG method offers a glimpse in real time at the growth kinetics of the nanoparticles which may reveal novel nucleation phenomena such as metastable nucleation states.

To date the SEDG method has been applied to over 3 separate systems to produce metal nanoparticle growth. It's possible that the method can be applied to a wealth of binary alloy systems to produce unique nanoparticles that cannot be realised easily through other growth methods. The binary alloy system allows significant reduced processing temperatures relative to the individual melting temperatures of the system. Adding a third alloy material to form a ternary alloy system could also be used to further depress processing temperatures. The main areas the SEDG method could be applied to include inexpensive catalysis formation, hierarchical advance materials and the production of very large single crystal metal nanoparticles relative to other synthesis methods.

3.8 SEDG Continuity

This chapter has described the individual phenomena with a significant bearing on the SEDG method in great detail. There remains great opportunity to study these phenomena in future work to resolve many scientific observations on nucleation and crystallisation. In terms of the research project continuity there remains practical in-house limitations that may inhibit or prevent future work with this method. It is worthwhile to highlight these limitations briefly for the purposes of future research projects. Indeed, the reason this thesis has two separate research topics is due to practical in house limitations which prevented continued work on the SEDG method along with renewing project funding.

The first practical limitation with this project is the cost of raw materials for deposition and ultimately growth. Ultrapure deposition materials are expensive and depending on the method of deposition can become prohibitively expensive to continue to use over time. The second practical limitation is access to deposition tools that can effectively deposit the desired material. To continue experimentation a robust deposition tool that can facilitate the deposition of many various materials without damaging it is required. One potential way to offset this in house limitation would be to have the material deposition performed in collaboration with another research group or institute that has such facilities.

3.9 References

1. Bhushan, B., *Springer Handbook of Nanotechnology*. Springer - Verlag.
2. Wagner, F.E., et al., *Before striking gold in gold-ruby glass.* Nature, 2000. **407**(6805): p. 691-692.
3. Faraday, M., *The Bakerian Lecture: Experimental Relations of Gold (and Other Metals) to Light.* Philosophical Transactions of the Royal Society of London, 1857. **147**: p. 145-181.
4. Mie, G., *Beiträge zur Optik trüber Medien, speziell kolloidaler Metallösungen.* Annalen der Physik, 1908. **330**(3): p. 377-445.
5. Xia, Y. and N.J. Halas, *Shape-Controlled Synthesis and Surface Plasmonic Properties of Metallic Nanostructures.* MRS Bulletin, 2005. **30**(05): p. 338-348.
6. Aiken Iii, J.D. and R.G. Finke, *A review of modern transition-metal nanoclusters: their synthesis, characterization, and applications in catalysis.* Journal of Molecular Catalysis A: Chemical, 1999. **145**(1–2): p. 1-44.
7. You, H., et al., *Synthesis of colloidal metal and metal alloy nanoparticles for electrochemical energy applications.* Chemical Society Reviews, 2013. **42**(7): p. 2880-2904.

8. Personick, M.L., et al., *Shape Control of Gold Nanoparticles by Silver Underpotential Deposition.* Nano Letters, 2011. **11**(8): p. 3394-3398.
9. Wagner, R.S. and W.C. Ellis, *Vapor-Liquid-Solid Mechanism of Single Crystal Growth.* Applied Physics Letters, 1964. **4**(5): p. 89.
10. Morales, A.M. and C.M. Lieber, *A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires.* Science, 1998. **279**(5348): p. 208-211.
11. Yu, D.P., et al., *Nanoscale silicon wires synthesized using simple physical evaporation.* Applied Physics Letters, 1998. **72**(26): p. 3458-3460.
12. Wang, Y., et al., *Catalytic Growth of Large-Scale Single-Crystal CdS Nanowires by Physical Evaporation and Their Photoluminescence.* Chemistry of Materials, 2002. **14**(4): p. 1773-1777.
13. López-López, M., et al., *Hillocks formation during the molecular beam epitaxial growth of ZnSe on GaAs substrates.* Journal of Crystal Growth, 1998. **193**(4): p. 528-534.
14. Shimada, T., et al., *Size, position and direction control on GaAs and InAs nanowhisker growth.* Superlattices and Microstructures, 1998. **24**(6): p. 453-458.
15. Hiruma, K., et al., *Growth and optical properties of nanometer-scale GaAs and InAs whiskers.* Journal of Applied Physics, 1995. **77**(2): p. 447-462.
16. Wu, X.C., et al., *Preparation and photoluminescence properties of crystalline GeO2 nanowires.* Chemical Physics Letters, 2001. **349**(3–4): p. 210-214.
17. Liu, X., et al., *Synthesis and electronic transport studies of CdO nanoneedles.* Applied Physics Letters, 2003. **82**(12): p. 1950-1952.
18. Young Kim, H., J. Park, and H. Yang, *Synthesis of silicon nitride nanowires directly from the silicon substrates.* Chemical Physics Letters, 2003. **372**(1–2): p. 269-274.
19. Ma, R. and Y. Bando, *Investigation on the Growth of Boron Carbide Nanowires.* Chemistry of Materials, 2002. **14**(10): p. 4403-4407.
20. Young Kim, H., J. Park, and H. Yang, *Direct synthesis of aligned silicon carbide nanowires from the silicon substrates.* Chemical Communications, 2003(2): p. 256-257.
21. (Ed.), R.S.W.A.P.L., *Whisker Technology,*. 1970, New York: Wiley-Interscience.
22. Hannon, J.B., et al., *The influence of the surface migration of gold on the growth of silicon nanowires.* Nature, 2006. **440**(7080): p. 69-71.
23. Jung, S.J., et al., *Surface energy driven agglomeration and growth of single crystal metal wires.* Nano Lett, 2011. **11**(3): p. 1294-9.
24. O'Regan, C., et al., *Engineering the Growth of Germanium Nanowires by Tuning the Supersaturation of Au/Ge Binary Alloy Catalysts.* Chemistry of Materials, 2013. **25**(15): p. 3096-3104.
25. Curtis, O.K., et al., *Single crystal iron nanocube synthesis via the surface energy driven growth method.* Nanotechnology, 2012. **23**(43): p. 435604.
26. Jung, S.J., et al., *Free-Standing, Single-Crystal Cu3Si Nanowires.* Crystal Growth & Design, 2012. **12**(6): p. 3076-3081.
27. Mills, K.C. and Y.C. Su, *Review of surface tension data for metallic elements and alloys: Part 1 – Pure metals.* International Materials Reviews, 2006. **51**(6): p. 329-351.
28. WW, M., *Flattening of a Nearly Plane Solid Surface Due to Capillarity.* Journal of Applied Physics, 1959. **30**(1): p. 77-83.
29. R. Nuryadi, Y.I., M. Tabe, *Formation and ordering of self-assembled Si islands by ultrahigh vacuum annealing of ultrathin bonded silicon-on-insulator structure.* Applied Surface Science, 2000. **160**.
30. Danielson, D.T., et al., *Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration.* Journal of Applied Physics, 2006. **100**(8): p. 083507.
31. Dai, B., L. Leal, and A. Redondo, *Disjoining pressure for nonuniform thin films.* Physical Review E, 2008. **78**(6).
32. Vrij, A., *Possible Mechanism for the Spontaneous Rupture of Thin, Free Liquid Films.* Discuss. Faraday Soc., 1966. **42**: p. 23-33.

33. Sheludko, A., *Thin Liquid Films.* Adv Colloid Interface Sci, 1967. **1**(4): p. 391-464.
34. Saramago, B., *Thin liquid wetting films.* Current Opinion in Colloid & Interface Science, 2010. **15**(5): p. 330-340.
35. Manev, E.D. and A.V. Nguyen, *Critical thickness of microscopic thin liquid films.* Adv Colloid Interface Sci, 2005. **114-115**: p. 133-46.
36. Morales, A.M.L., C. M. , *A laser ablation method for the synthesis of crystalline semiconductor nanowires* Science, 1998. **279**: p. 208-211.
37. F. Vandenbrouck, M.P.V., A.M. Cazabat, *Thin Nematic Films Metastability And Spinodal Dewetting.* Physical Review Letters, 1999. **82**(13).
38. Sangwal, K., *Additives and Crystallization Processes from Fundamentals to Application*. 2007: Wiley.
39. Sunagawa, I., *Crystals: Growth, Morphology and Perfection*. 2007.
40. Sun, Y., *Controlled synthesis of colloidal silver nanoparticles in organic solutions: empirical rules for nucleation engineering.* Chem Soc Rev, 2013. **42**(7): p. 2497-511.
41. Deniz Erdemir, A.Y.L., Allan S. Myerson, *Nucleation of crystals from solution classical and two step models.* Accounts of Chemical Research, 2009. **42**(5): p. 621-629.
42. Oxtoby, D.W., *Nucleation of First-Order Phase Transitions.* Accounts of Chemical Research, 1998. **31**(2): p. 91-97.
43. Filobelo, L.F., O. Galkin, and P.G. Vekilov, *Spinodal for the solution-to-crystal phase transformation.* J Chem Phys, 2005. **123**(1): p. 014904.
44. James F. Lutsko, G.N., *Theoretical Evidence for a Dense Fluid Precursor to Crystallization.* Physical Review Letters, 2006. **96**.
45. Finney, E.E. and R.G. Finke, *Nanocluster nucleation and growth kinetic and mechanistic studies: a review emphasizing transition-metal nanoclusters.* J Colloid Interface Sci, 2008. **317**(2): p. 351-74.

Chapter 4

Single Crystal Fe Nanocubes Synthesised via the SEDG Method

4.1 Introduction

Since the introduction of the hard disk drive in the 1956 by IBM the majority of research on magnetic materials focused on further developing the magnetic components of the drive. Increasing the areal density of the disk drive required successively developing magnetic media with smaller and smaller information clusters or 'bits' while increasing the sensitivity of the read head [1]. Today the magnetic bits are firmly in the nano-regime and can technically be thought of as bottom up synthesised nanoparticles [2]. Beyond magnetic recording devices magnetic nanoparticles have been developed for use in biomedicine, magnetic fluids, catalysis and environmental remediation [3, 4]. The enhanced surface area per particle make them attractive catalysts but there are two unique properties of magnetic nanoparticles that are of particular importance to their application. These so called finite size effects promote single magnetic domain formation within a nanoparticle imbuing it with very high coercivity or high resistance to an external magnetic field[5]. The particles coercivity is also influenced by the shape of the nanoparticle and its crystallinity. The second finite size effect is superparamagnetism, this effect allows the magnetic moment of the nanoparticle to flip under thermal energy changes and serves to increase the magnetic susceptibility - the degree of magnetisation, relative to bulk values of the nanoparticle material.

Magnetic nanomaterials include nanoparticles of Fe, Co, Ni with alloys and oxides such as FePt and Fe_3O_4 commonplace [6-8]. The reactivity of the metals makes it difficult to prevent oxidation of the nanoparticle. In many cases oxidation decreases the magnetic properties of the particle so steps are taken during synthesis to introduce a capping layer or the synthesis is designed to produce a magnetic alloy. Iron nanoparticles are well known to oxidize at atmosphere diminishing their properties over time. The resultant Fe_3O_4 oxide nanoparticle is

often used as an enhancing contrast agent during MRI scans, it can also be functionalized to selectively bond to damaged cells in the body which are then destroyed under force of an external magnetic field. Pure iron is a potent catalyst. Among other metals - it is well documented to readily enhance the Fischer-Tropsche synthesis of long chain hydrocarbons from small constituents[9]. With greater surface area Iron nanoparticles are ideal for scaling up this process, however due to oxidation and fouling they quickly lose their catalytic properties. Beyond catalysis iron is an important magnetic material that displays high saturation magnetisation and low magnetic anisotropy which are important for analogue circuit components such as transformers[10]. Irons low magnetic anisotropy (the relative magnetisation of different crystallographic directions) make it useful for electronic and information storage.

Iron nanoparticles are readily synthesized through colloidal means[10]. In a typical reaction – the precursor is an iron containing salt such as $FeCl_3$ are reduced in solution via arrested precipitation. Agglomeration is prevented via the introduction of a surfactant. Without special steps to prevent oxidation such as introducing a capping agent the iron nanoparticle s will oxidize in atmosphere or in a water solvent. Capping agents can be used to direct growth and crystallinity of the nanoparticle. Wire-like morphologies of iron can be obtained through laser induced deposition[11]. Iron deposited into anodised aluminium oxide (AAO) forms an amorphous wire which will be prone to oxidation. Single crystal self-assembled iron nanowires are formed by laser deposition of an iron containing perovskite target ($La_{1-x}Sr_xFeO_3$), the wires however remain embedded in a $LaSrFeO_4$ matrix and cannot be isolated individually[12]. Fan *et al.* reported the low temperature synthesis of Fe nanoparticles that resulted in the growth of 200 nm cubes [13].

The breadth of potential applications of the nanoparticle will thus be the deciding factor in the synthesis of the particle. Small size, high surface area, resistance to oxidation/fouling and crystal structure are important for catalytic applications. For electronics size and magnetisation properties are paramount. Therefore there is a need for highly crystalline magnetic nanoparticles that display the inherent finite size effects detailed earlier. They must also be resistant to oxidation and easily accessible/isolated such that they can incorporated into novel technologies. In this chapter the results of employing the SEDG method to synthesise single crystal iron nanoparticles between 50-600 nm in size are presented. These are the largest single crystal iron nanoparticle synthesised to date; heretofore the largest reported size was 200 nm [13])

4.2 Experimental Details

Fe-Nd bilayer samples were prepared on Si(100) wafer substrates (4 in. diameter, 280 µm ± 10 µm) with a 200 Å thick Si3N4 layer (NOVA electronic materials) . Typical sample sizes were approximately 1 cm^2 hand cleaved substrates. Polycrystalline layers of iron and neodymium were deposited using a magnetron sputter-coater (208 HR) employing a quartz crystal microbalance to monitor thickness. After deposition of the thin Fe film the sample was half covered so as to intentionally introduce a film edge in the middle of the substrate. This introduced film edge promoted dewetting in the bilayer film. Iron (Advent Research Materials) and neodymium (Testbourne) sputter targets were greater than 99.5 % and 99.9 % purity respectively. Fe is particularly difficult to sputter using a magnetron sputter-coater. This is a direct consequence of the magnetic properties of the Fe target disrupting the formation of the plasma 'racetrack' at the target interface. To offset this difficulty extremely thin foils of Fe targets were used ~ 0.25 mm thickness. Samples are initially prepared as polycrystalline thin films of iron and neodymium deposited on amorphous Si_3N_4 substrates via sputter deposition [14] [16]. This method is intentionally employed as it produces low quality film relative to other deposition methods. The purpose being that perfectly flat defect free films prepared by atomic layer deposition would be prohibitively stable against dewetting. Bilayer samples of various thickness (between 1-5 nm of each) were then annealed close to the eutectic temperature (700 °C Fe-Nd) for 4 hours under a 10:90 hydrogen-nitrogen atmosphere at a flow rate of 500 sccm and chamber pressure of 4.5 Torr before being allowed to cool to room temperature for analysis.

Qualitative information about the morphology of the resulting structures was obtained using SEM (Zeiss Ultra). The crystal structure and composition of the nanoparticles was obtained by TEM (FEI Titan) with EDX capability. To monitor the real time growth of the nanocubes samples of 4 nm Nd with 5 nm Fe were prepared but not annealed. A water-cooled hotstage attachment (Kammrath and Weiss Jumbo dTron 304) was set up within the chamber of the SEM (ZeissUltra) with a vacuum Pressure of $<10^{-5}$ mbar throughout. Sample heating was performed manually on the hot stage controller. Samples were typically heated up to 600 °C at a rate of ~ 20 °C/min then to 650 °C at a rate of ~3.5 °C/min. From 650 °C – to 685 °C ($T_{eutectic}$) heating was performed incrementally to prevent significant sample drift and allow for better quality imaging. The temperature was held constant the moment film rupture was observed

while imaging the edge boundary region. At the point of film rupture a droplet is identified and its evolution monitored as shown below. MFM measurements were carried out in collaboration with Nanoscan using a PPMS-AFM (Physical Property Measurement System). The PPMS-AFM system can has an operational range of 4-400 K and the option to apply fields of up to 16 T.

4.3 Fe Nanocubes Grown with SEDG by Design

4.3.1 Design Flow

In the previous chapter the relevant steps for the design and synthesis of novel nanoparticles was outlined as a generic approach to SEDG. In this chapter a focused approach is taken for the synthesis of Fe crystals using this novel method. The relevant parameters for the production of single crystal iron via the SEDG method were established. Fe is a magnetic transition metal with relatively high surface energy of 2.2 J/m^2 , it has a melting temperature of 1538 °C and is prone to oxidation both in solution and atmosphere. The surface energy of Fe is relatively large compared to other transition metals. For this reason it was seen as an ideal prospective material for nanoparticle growth using this new growth method. Having gained an understanding of the general properties of Fe and its surface energy the equilibrium crystal shape is determined. Generally Wulff construction should be used to discover the equilibrium crystal shape of a crystal but for this particular case it was sufficient to consult the literature for the equilibrium crystal shape of Fe [15, 16]. The most stable crystal surface of Fe is the <100> crystal plane, this is manifested in the simple cubic structure the equilibrium crystal shape adopts. In this case nanowires would not be expected to form following the SEDG production of Fe crystals as previously reported for SEDG grown Au and Cu_3Si nanowires [17, 18]. Despite their cubic shape they could still be useful as bit-patterned magnetic recording media or as small single crystal catalysts.

SEDG step 4 (see Chapter 3) involves choosing an alloy material for the primary material, which in this case Fe. Fe is most often alloyed with Nd and B to produce ultrastrong permanent magnets [19]. Both the Fe-B and the Fe-Nd binary alloy phase diagrams contain eutectic points with eutectic temperatures of 1195 °C and 685 °C respectively. Therefore, based on the lower

more accessible eutectic temperature, the relatively simple binary alloy phase diagram, the surface energy of Nd ~ 0.7 J/m^2 and the wealth of information about Nd and Fe alloys available in the literature - the Fe-Nd system was chosen for prospective growth.

To facilitate growth of Fe nanoparticles SiO_2 was initially chosen as a substrate during processing. It was assumed its low surface of 0.75 J/m^2 energy would enable dewetting of the liquidus alloy. However post annealing analysis revealed no agglomeration or any crystal formation on the SiO_2 substrate. SEM images of the surface of the substrate revealed a pitted and blurry-like texture indicative of etching. Subsequent research showed that transition metals such as Fe and Cu preferentially diffuse and etch through the SiO2 and react to form silicides. The use of Si_3N_4 substrates was then employed during processing to prevent etching. Si_3N_4 has a very low surface energy value of ~ 0.3 J/m^2 and is therefore conducive to promoting dewetting of the thin alloy film. Thin film deposition of each component was performed using a magnetron sputter coater which required an ultra-thin (0.25 mm) Fe foil in order to deposit Fe.

Efforts were also made to control the dewetting and agglomeration of the liquidus alloy film by introducing I-beam milled holes. These efforts were unsuccessful however and no evidence for circular diffusion wavefronts was found during post processing analysis. This may be explained by the relatively higher surface energies involved in comparison to the Au-Ge system. Fe much higher surface energy value likely results in a more viscous liquid alloy upon dewetting in comparison to the Au-Ge liquid alloy.

4.3.2 Fe Nanocube Growth

The various stages in the growth of Fe nanocubes produced via the SEDG method are shown schematically in Figure 4.1. Prior to annealing, film edges are intentionally incorporated into the bilayer film by covering half the substrate with a thin film of Fe already deposited as seen in Figure 4.1 (a). This facilitates the initial step in the growth process which is the formation of a liquidus FeNd alloy. The bilayer sample is annealed to 700 °C. This temperature is slightly above the FeNd eutectic temperature of 685 °C as shown in the Fe-Nd binary alloy phase diagram in Figure 4.1 (d) [18][20]. Above this temperature iron has sufficient energy to diffuse into the neodymium layer [19][21] facilitating the formation of the liquid alloy. No data exists

on the surface energy of the liquidus alloy of FeNd with eutectic composition. It was therefore assumed since Si_3N_4 has a lower surface energy (Si_3N_4 ~ 0.3 J/m2)[21][22] than either of the Fe (2.2 J/m^2) or Nd (0.7 J/m^2) film components this would provide a large driving force for de-wetting.

The liquidus alloy film formation is then proceeded by its rupture and break up into droplets or islands on the substrate seen in Figure 4.1 (b). Film breakup is an activated process which occurs preferentially at edges of the film that facilitates Fe and Nd intermixing and the creation of voids that expose the low surface energy substrate. The effect of heterogeneous nucleation, film thickness and interfacial energy determine the film stability on the substrate was revealed in chapter 3 [23-26]. Heterogeneous nucleation is important and the greatest density of cubes is always found at edge boundaries between the Nd and Fe layers illustrated in Figure 4.1 (b). The most prominent factor in determining film stability is the thickness of the liquidus alloy film. There is an upper limit on the amount of alloy material that can be deposited before the film becomes stable and thus fails to undergo the de-wetting process that is pivotal for SEDG. Droplets formed on the substrate following dewetting initially maintain the 78 atom % Nd eutectic composition of the film prior to break up. Continued heating sets up a dynamic system of dissolution and addition as Nd and Fe atoms diffuse and agglomerate into the droplets. The greater diffusion rate of Fe relative to Nd [19][21] causes the composition of the droplet to shift from the Nd rich side of the phase diagram into the $Fe_{17}Nd_5$ + L region (see Figure 4.1 (d)). At this point each droplet can be thought of as a pseudo-undercooled alloy melt containing between 10-78 atom % Nd. The increased diffusivity of Fe relative to that of Nd continues to increase the Fe composition within the droplet ultimately creating an Fe rich core-shell structure (Figure 4.1 (c)). The nucleation of Fe within the droplet is a consequence of the higher surface energy of Fe relative to Nd, which causes the higher surface energy component to segregate from the lower surface energy component, enriching the surface of the droplet with Nd [22][27] (Fe ~ 2.2 J/m^2,Nd ~ 0.7 J/m^2 at 700 °C) [23][28]. Continued heating promotes further growth of the nanocube within the droplet.

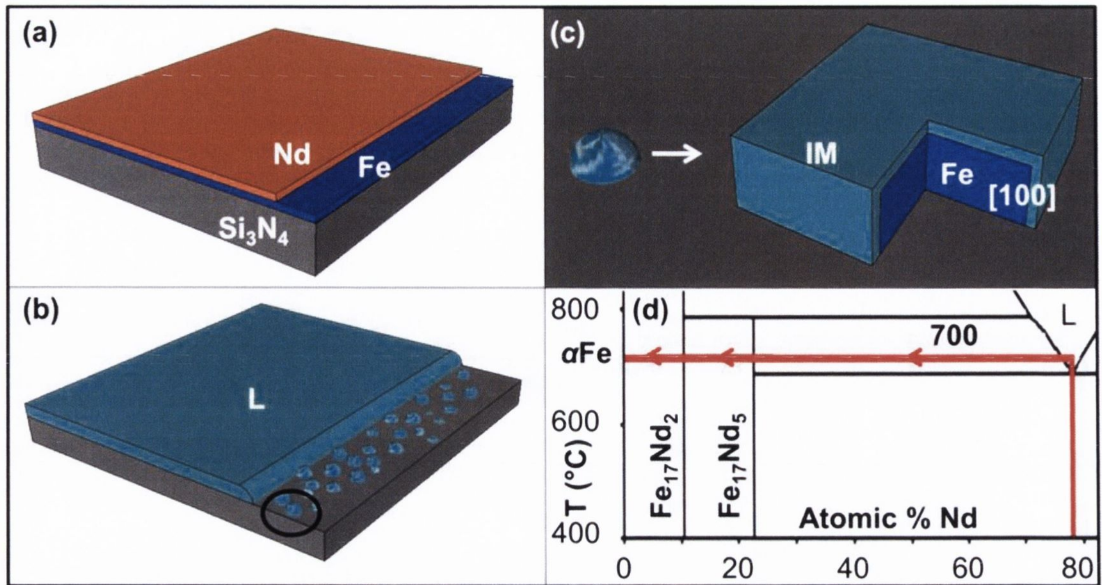


Figure 4.1 Schematic representation of the growth process. The growth mechanism of the nanocubes can be understood following the red line traced on a section of the Fe-Nd phase diagram (d) [20]. (a) Thin films of Fe and Nd are initially deposited on a Si_3N_4 substrate. (b) Bilayer samples are annealed at 700 °C, 15 °C greater than the $T_{eutectic} = 685$ °C of FeNd in order to promote liquidus alloy (L) formation with 78 atomic % Nd followed by film rupture and eutectic droplet formation (circled). This sets up a dynamic system of dissolution/addition of surface diffusing Fe and Nd atoms from the droplets. Due to the greater diffusion rate of Fe relative to Nd the eutectic composition of the droplets cannot be maintained pushing the composition of the droplet into the $Fe_{17}Nd_5$ + L section of the phase diagram. Continued Fe diffusion prevents a stable equilibrium from forming. (c) Maintaining the saturation conditions facilitates nucleation and formation of α–Fe phase crystal within the droplet. The cubic structure adopts the equilibrium crystal shape of Fe – a cube faceted by 6 [100] planes within the droplet. The alloy droplet encases the growing cube and forms a crystalline FeNd intermetallic (IM) phase. (d) Section of the Fe-Nd binary alloy phase diagram. The red line follows the enrichment path of the droplet with arrows indicating compositional changes that are occurring.

4.4 Real time Nanocube Growth

The nucleation and growth of the single crystal Fe nanocubes described in the previous section can be captured in real time using a specialised hot stage adapted for use with an SEM. This apparatus offers the ability to heat samples with the pre-deposited bilayer film to the required process temperature of 700 °C while using standard SEM to record the behaviour of the film. Bilayer films were heated 600 °C before approaching 700°C at a slower heating rate. Interestingly, during the slow approach to the standard annealing temperature of 700 °C used with the furnace, bilayer films were observed to undergo rupture, dewet and ultimately form Fe crystals at temperature of ~ 650 °C, 35 °C below the eutectic temperature of the binary alloy. Although sub-eutectic nanoparticle growth has been reported previously [29], it is the first time it has been observed for non-VLS growth methods.

The real time growth of an Fe nanocube is shown in Figure 4.2 below. Heated up to a sub-eutectic temperature ~ 670 °C prior to capture, the first image in the sequence follows the formation of a rectangular crystal faceted shape immediately after film rupture and dewetting. 30 seconds on from the initial image capture the crystal is seen to increase dramatically in size. After 120 seconds the crystal is visibly bigger still and its features have become more noticeably faceted.

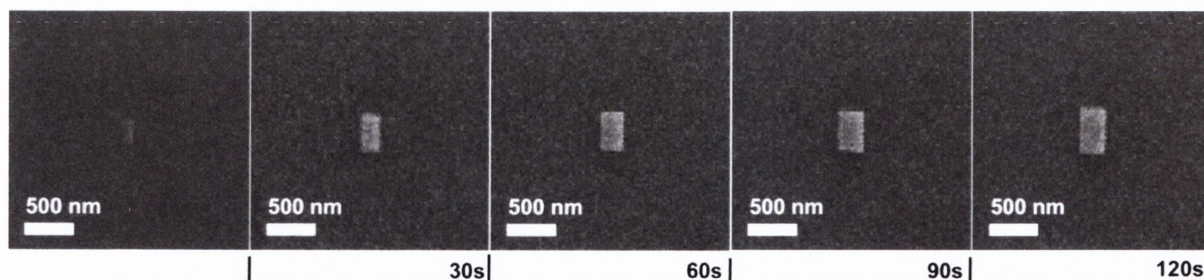


Figure 4.2 Real time growth of Fe nanocrystal using an SEM mounted hot stage to heat a predeposited bilayer sample of Fe and Nd. The sequence, taken immediately after film rupture follows the growth of a small rectangular crystal over the course of two minutes. During this time, it is observed to develop more noticeable facets and increase eight times in size.

4.5 Cube Morphology and Size

The incorporation of just 1 nm neodymium on a 1 nm thick iron film and subsequent annealing above the Fe-Nd eutectic temperature ($T_{eutectic}$ = 685 °C) at 700 °C resulted in the formation of small brightly contrasting shapes such as those shown in Figure 4.3 (a). Increasing the Fe composition in the bilayer to 3 nm, resulted in the formation of cube-like structures following the anneal such as those shown in Figure 4.3 (b). This cubic morphology is consistent with the equilibrium crystal shape of Fe. When a 5 nm thick Fe layer was deposited and annealed the growth of a small number of very large cube structures was observed (see Figure 4.3 (c)). Fe films of 10 nm thickness became increasingly stable against dewetting. This thickness represents the maximum thin film thickness at which cubic structures will form under these annealing conditions unless extra film edges or other heterogeneous nucleation sites are introduced via extra processing steps. Figure 4.3 (d) shows an angled view of one such structure; the cube is viewed at a 54° angle in a scanning electron microscope (SEM) and has a height of ~ 340 nm, which is comparable to its lateral dimensions.

The influence of the relative thickness of the Fe and Nd film layers on cube growth distribution was studied. The size distribution analysis only included nanoparticles with clearly defined cubic shapes, all other particles were omitted. Figure 4.4 (a) shows the dependence of the average cube size on the thickness of iron in the bilayer film. A 4 nm Nd layer was used throughout since this thickness of neodymium in the bilayer was found to promote cube formation with the smallest size dispersion in cubic structures formed for a set layer thickness of Fe. Also evident from the error bars in Figure 4.4 (a) is the increase in size disparity of the cubes for thicker bilayer films. Histograms showing the cube edge length and their frequency of occurrence following anneals of 1-5 nm Fe thick bilayer films are presented in Figure 4.4 (b). Counting was performed over a ~ 7.5 x 5.5 μm area of the substrate where cubes had formed. For clarity the binning parameters (cube edge length increments) are fixed at the same values for each Fe film thickness. Thin Fe films (1-2 nm thick) produce cubes with lower size disparity with the majority of cubes in the sub 100 nm range. The number density of cubes with dimensions greater than 200 nm increases as the Fe pre-anneal layer thickness is increased above 3 nm. Thus by controlling the thickness of Fe layer the average size of the cubes can be controlled.

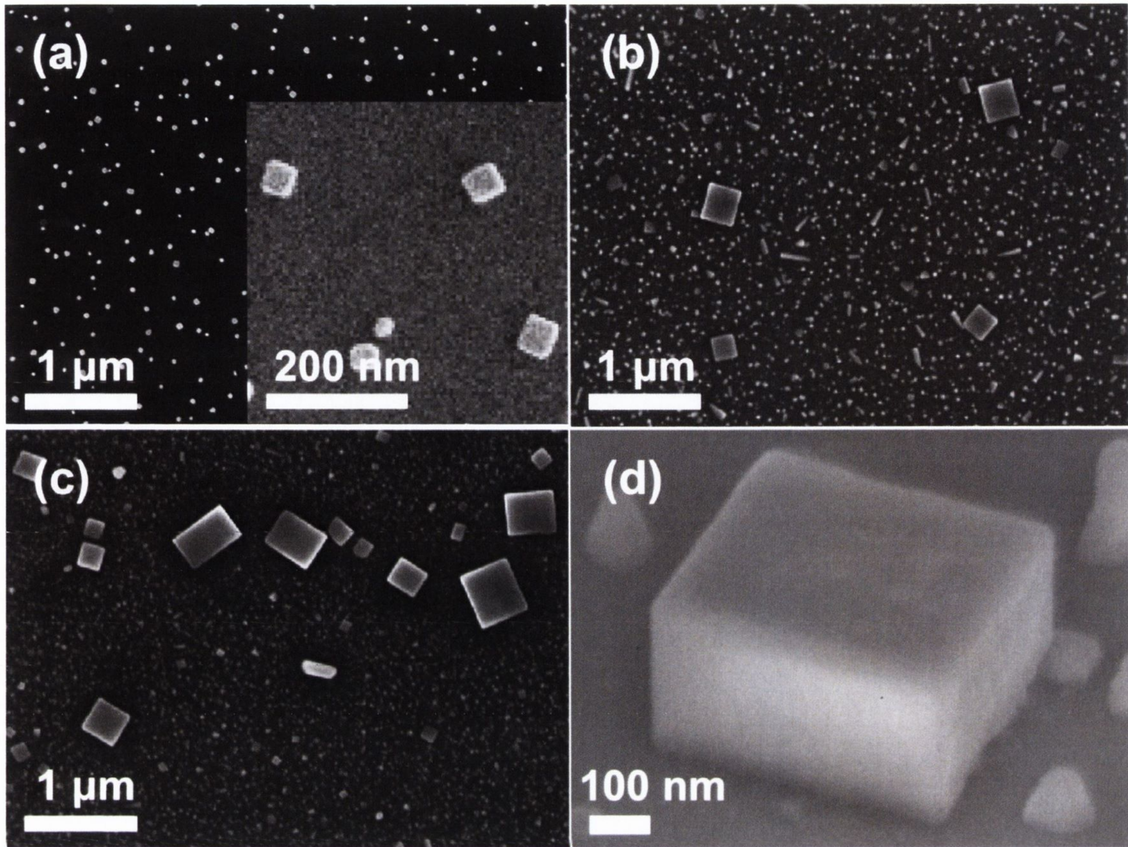


Figure 4.3 SEM images of particles formed on the Si_3N_4 substrate after annealing bilayer films of various thickness for two hours. (a) Cubic features formed after annealing films of 1nm Fe with 2 nm Nd, inset higher magnification image of the features formed. (b) Particles with clear square geometry form following annealing 3 nm thick films of iron with 4 nm Nd. (c) Particles with refined structure observed after annealing a 5 nm thick film of Fe with 4 nm Nd. (d) An image of a square particle grown from a 5 nm thick film of Fe with 4 nm Nd observed at an angle of 54° showing an elevation of ~340 nm from the substrate surface.

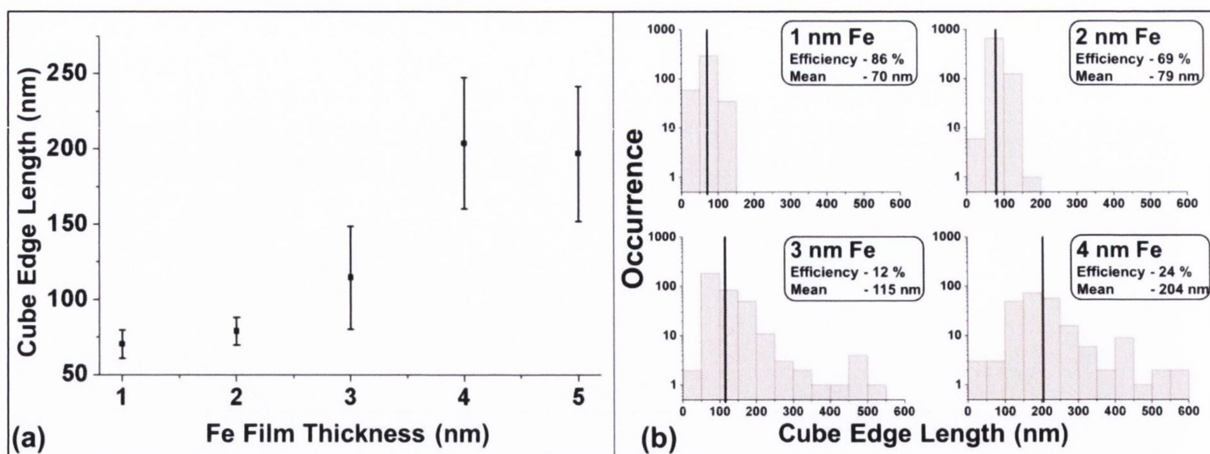


Figure 4.4 Average nanocube edge length and size distribution. (a) Pre-anneal Fe film thickness in the Fe-Nd bilayer ultimately dictates the mean size of the nanocubes formed after annealing. The standard deviation (y-uncertainty bars) in cube dimension increases greatly as the deposited thickness of Fe is increased. (b) Histograms depicting the greater number density and mean size (solid line) of cubes with larger dimensions produced for a set Fe film thickness (1 - 4 nm). The mean size of the cubes formed is shown to increase with initial Fe layer thickness. Not all iron in the film forms nanocubes upon annealing. For thicker films the efficiency of cubes formed relative to non cubic structures formed is lower compared to thin iron films. Counting was performed over an ~ 7.5 x 5.5 μm area on the substrate at edge boundaries between the Nd and Fe layers. An optimized thickness of a 4 nm Nd layer was typically used for a set thickness of Fe in the bilayer as it was found to consistently facilitate cube formation.

4.6 Physical Properties

To characterise the structure and composition of the nanocubes several cross-sectional lamella were prepared using focused ion beam (FIB) techniques for transmission electron microscopy (TEM) analysis. The nanocube which was used for TEM analysis is shown in Figure 4.5 (a). It was produced by annealing a bilayer sample with 4 nm Nd with 3 nm Fe. Figure 4.5 (b) presents a broad overview of the cross section structure of the Fe nanocube. The presence of tungsten is due to an intentionally introduced capping layer used to protect the cube from damage during the course of TEM lamella preparation. The Si_3N_4 substrate is shown below the cube. It was noted also during the analysis of the nanocube lamella that there appeared to be no crystal registry between the substrate and the growth direction of the nanocube. The cross section also reveals the presence of a thin capping layer ~ 20 nm thick encasing the entire cube. Furthermore the cube shows almost no truncation by the (110) plane at the corners of the cube. The presence of this capping layer around the growing Fe nucleus is a feature of the SEDG method [15][17]. This layer facilitates the saturation and nucleation of the single crystal component and arises from the nature of the growth mechanism which is discussed above.
Figure 4.5 (c) shows a TEM image of the lattice structure at the centre of the cube, circled in (b), viewed along the <100> zone axis. The lattice parameter corresponds to the body centred cubic (b.c.c) α-Fe structure and local area electron diffraction pattern in Figure 4.5 (d) reveals the single crystal nature of the cube. The inset in Figure 4.5 (d) shows the inverse FFT of the diffraction pattern and displays the Fe lattice spacing. Energy dispersive X-ray (EDX) spectra in Figure 4.5 (e) confirm the composition of the cube, revealing peaks characteristic of bulk Fe. The presence of a tungsten peak in the EDX is an artefact of the lamella preparation. A high magnification image of the iron core capping layer interface recorded at the square box location highlighted in Figure 4.5 (b) is shown Figure 4.5 (f). The image was obtained along the same zone axis as Figure 4.5 (c) and highlights the crystalline nature of the capping layer surrounding the cubic iron core.
It proved difficult to completely characterise the capping layer in the same detail as the core iron despite many FFTs and EDX spectra of the layer, some of which are presented in Figure 4.6. The capping layer was identified as that of an intermetallic (IM) phase alloy of the FeNd binary alloy phase diagram based on Figure 4.1 (d). Liquid droplets of eutectic composition form as the bilayer film is annealed. These droplets become saturated by iron due to its greater relative diffusion rate compared to Nd changing the composition of the droplet shifting it to

the Fe rich side of the binary alloy phase diagram shown in Figure 4.1 (d) – as prescribed for SEDG to occur. The change in composition of the droplet results in the segregation of the components, namely, the lower surface energy component (Nd) begins to enrich the surface of the droplet due to a Gibbs-Thompson effect. With continued Fe enrichment the conditions for crystallisation of the α-Fe phase within the droplet are met. However, during the α-Fe crystallisation process, alloy crystal phases of either $Fe_{17}Nd_5$ or $Fe_{17}Nd_2$ are likely to form as the composition of the droplet dynamically changes as described in the Fe-Nd phase diagram shown in red in Figure 4.1 (d). These intermetallic phase may condense on the surface of the growing αFe crystal giving rise to the quality of the crystalline character of the capping layer as seen in Figure 4.6 (e). The surface layer may also form during cooling at any point along the enrichment pathway in Figure 4.1 (d). The relative amount of Nd in both crystal alloy phases is relatively small - $Fe_{17}Nd_5$ + $Fe_{17}Nd_2$ (22 and 10 atomic % Nd respectively). This difference of Fe relative to Nd could account for the poor Nd detection rates in EDX analysis obtained on the ~ 20 nm thick capping layer. Furthermore the annealing temperature (700°C) is sufficiently close to the melting point of Nd (T_{melt} ~ 1000 °C) to enhance evaporation of Nd from the thin bilayer film.

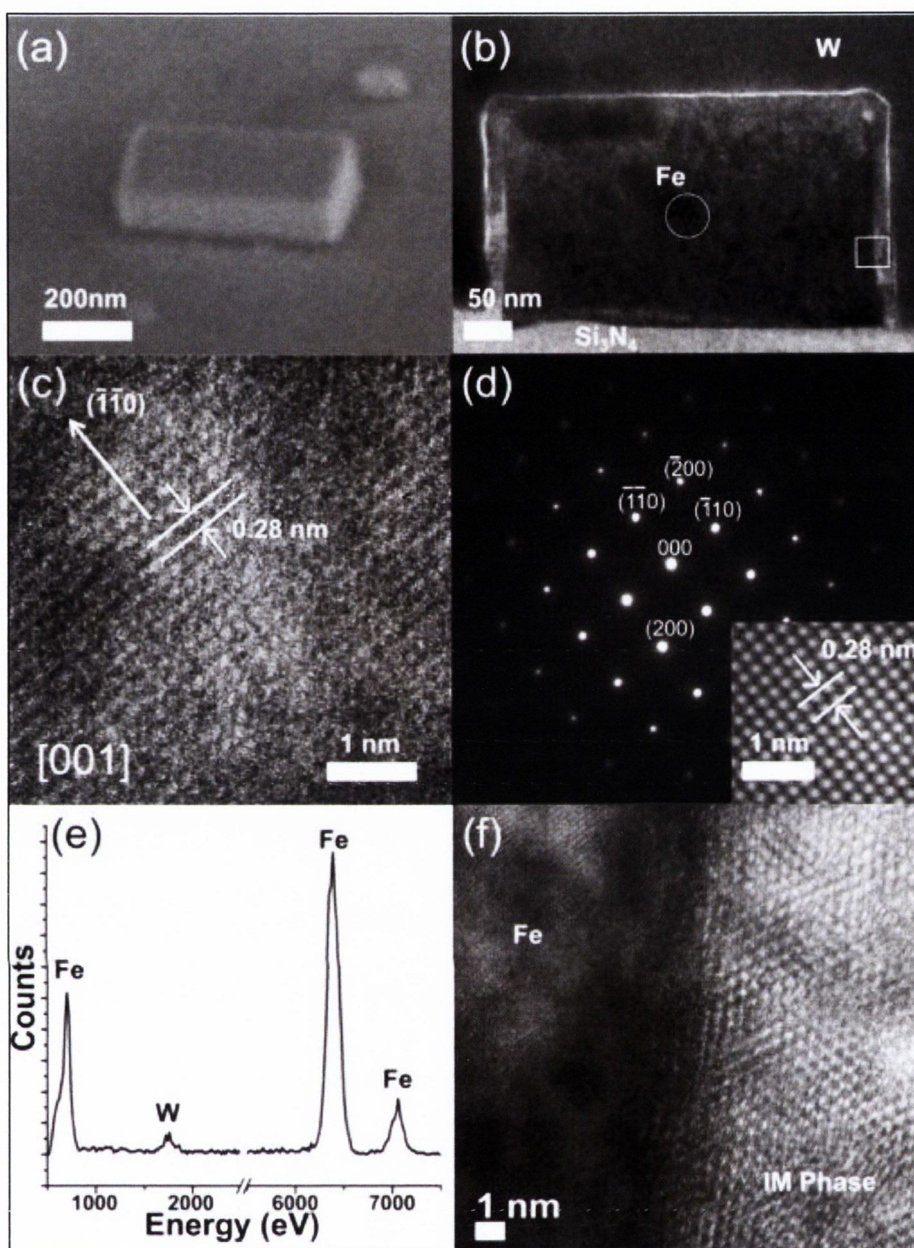


Figure 4.5 TEM characterisation of a characteristic nanocube. (a) SEM image of the nanocube prior to lamella preparation for TEM analysis, the nanocube was isolated post anneal of a 4 nm Nd, 3 nm Fe bilayer film. (b) TEM image of the nanocube cross section indicating the tungsten protective layer, Si_3N_4 substrate and also the presence of a capping layer around the iron crystal. (c) TEM image obtained at the centre of the cube (white circle in (b)), the lattice parameter of iron (0.28 nm) is confirmed along the [001] zone axis. (d) Selected area electron diffraction pattern from (c) reveals the bcc single crystal structure of the cube. Inset; an inverse FFT showing the structure has the same lattice parameter observed in (c). (e) EDX spectra of the core structure confirms the metallic iron character of the cube. The presence of a tungsten peak is due to the ion beam interactions (that are a consequence of lamella preparation) introducing some tungsten from the protective layer into the cube (f) TEM image of the iron core structure and the intermetallic (IM) capping layer encasing the cube (white square in (b)) viewed along [001] zone axis. The crystalline capping layer was a consistent thickness around the iron core structure.

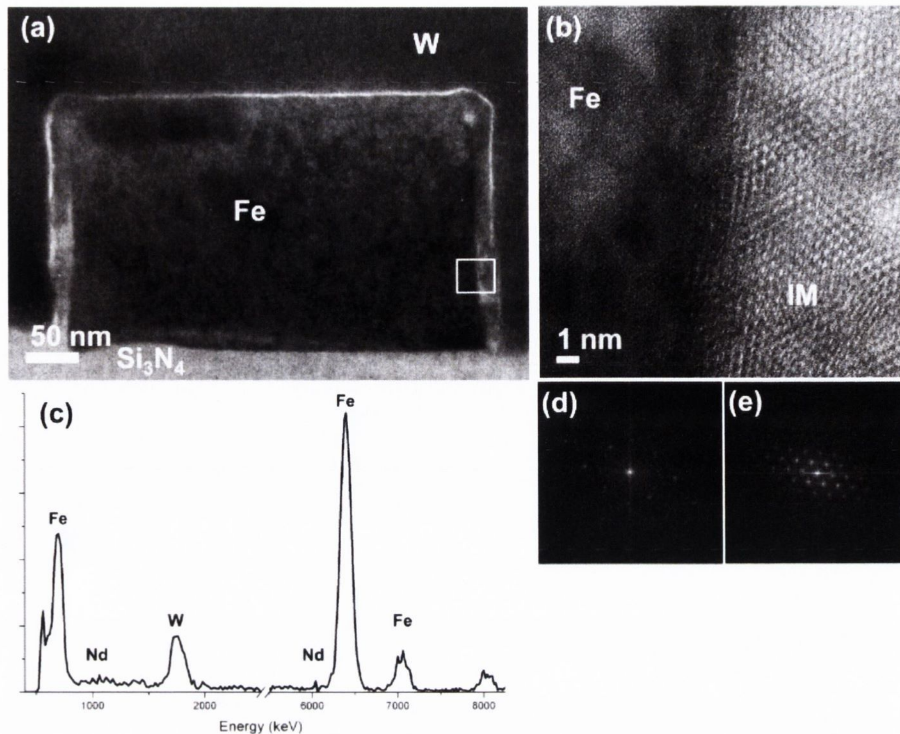


Figure 4.6 Preliminary characterisation of the iron cube capping layer. (a) Cross section of a nanocube. (b) HRTEM of the cube/capping layer interface, obtained from the area marked with a white square in (a) viewed along the [001]. (c) EDX analysis of the capping layer. Iron, tungsten and neodymium peaks were resolved. (d) FFT pattern obtained at the Fe cube. (e) FFT pattern obtained from the capping layer showing a periodic array suggesting the layer is crystalline.

The magnetic properties of the cubes were studied in collaboration with a team in Switzerland. The group performed a specific type of atomic force microscopy known as magnetic force microscopy (MFM) which principally maps the magnetic interaction of the AFM probe tip which is coated in a magnetic material, with the magnetic sample, in this case single crystal iron nanocubes. The single crystal nature of the nanocubes and their size is predicted cause the nanoparticle to exhibit so called finite size effects - either very high coercivity or exhibit superparamagnetism. Due to technical difficulties it was not possible to attempt dynamic magnetic experiments that would reveal these two effects in the cubes.

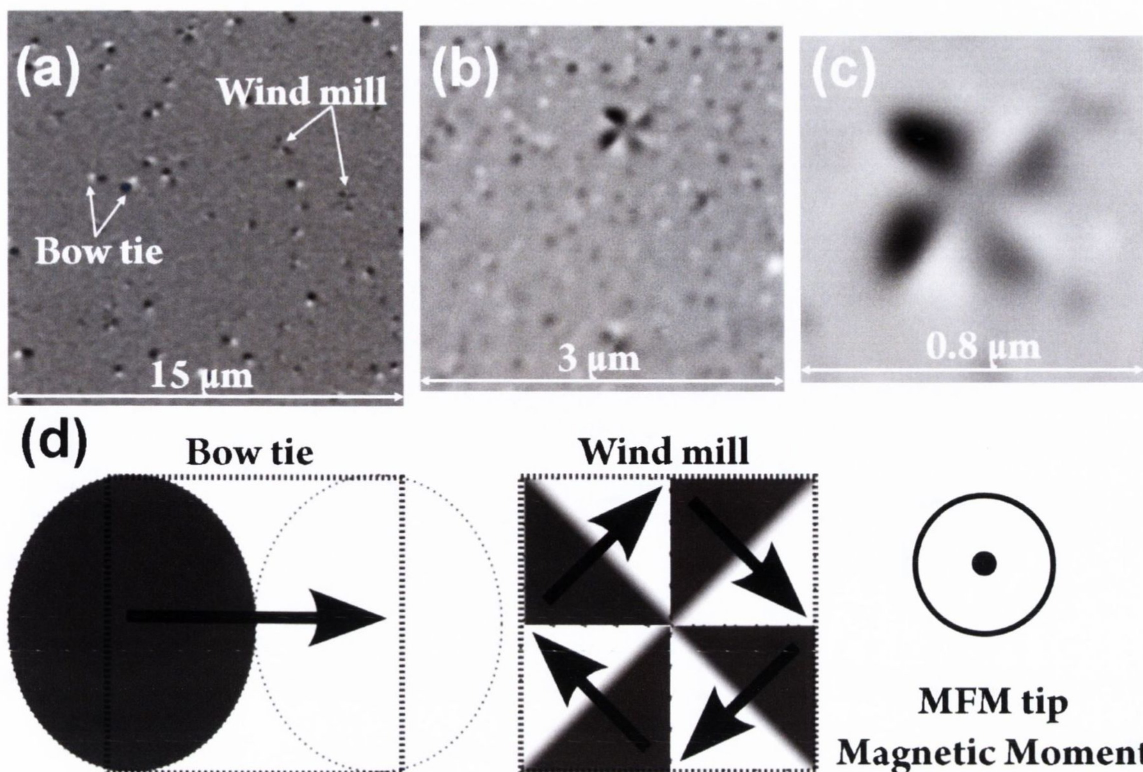


Figure 4.7 MFM images of samples with Fe nanocubes on the surface with a schematic of the magnetic domains revealed on the surface. (a) Bow tie and wind mill patterns are observed around the wide area scan of 15 μm^2. (b),(c) High resolution MFM scans on the windmill patterns reveal the complicated magnetic domain formation within a large nanocube. (d) The magnetic dipole bow tie and wind mill pattern are shown schematically. Dark areas are attractive for the MFM tip and white areas are repulsive to the tip which is magnetised into the direction of the sample.

High resolution MFM was possible however and revealed interesting magnetic features on the surface of the sample as shown in Figure 4.7. The sample is magnetised in the plane of the sample to introduce a magnetic moment to the particles prior to MFM. The tip is also magnetised in the direction of the tip long axis so as to interact with magnetic moments on the surface of the sample. The dark and white areas of the patterns represent attractive and repulsive tip/sample interactions respectively. Two distinctmagnetic features formed on surface following the magnetisation step, namely what appears to be a simple magnetic dipole or "bowtie" and a more complicated magnetic moment pattern or "wind mill" [30]. The two features formed are distinct and were present in unequal amounts on the substrate.

As the Fe nanocubes are single crystal there should be no individual grain boundary defined magnetic domains within them. Any domains formed within the single crystal represent a magnetostatic energy minimisation as the cubes become large enough to exit the finite size effects that were introduced at the beginning of the chapter namely the ability of a magnetic nanoparticle to contain only one magnetic domain. In the absence of the topographical line scan associated with the MFM trace it is difficult to infer the windmill patterns are produced in the larger sized cubes relative to the bowtie patterns.

4.7 Conclusions and Outlook

The SEDG technique has been successfully applied to the growth of single crystal Fe nanocubes using the Fe-Nd binary alloy system. Once the initial candidate material – Fe in this case, was chosen an alloying component was found following judicious choices prescribed by the SEDG process flow chart. Nd was nominated as the alloy component because of its low surface energy relative to Fe and the elementary binary alloy phase diagram the two elements form. FeNd magnets are well established magnetic materials which provided a large knowledge base in the literature. The use of Nd also introduced some redundancy into the process should pure Fe crystals fail to precipitate from the saturation process any resultant FeNd alloy would still be magnetic and therefore useful for applications.
Early experiments revealed heating the FeNd bilayer film to 700 °C on SiO_2 produced etching during processing. Thereafter inert etch/diffusion barrier Si_3N_4 substrates were used to deposit and process the bilayer films which proved successful. As expected the higher surface energy Fe component condensed within droplets to form single crystal Fe nanocubes on the substrate surface. The flow chart reveals cubic structures of Fe should result as this form is the equilibrium crystal shape of an <100> stabilised nanoparticle. The thickness of Fe in the bilayer was found to be the dominant factor determining the average cube dimensions, yielding cubes up to 0.6 μm in size – the largest single crystal Fe particles to date.
TEM and SAED revealed the single crystal nature of the cubic particles. The presence of an intermetallic phase surrounding the Fe core was also observed. The presence of a capping layer is not remarkable for SEDG and has been observed with other systems. However its high degree of order and crystallinity was a novelty in comparison to the amorphous capping layer reported previously by us [17]. The growth of a nanocube was witnessed in real time using an SEM mounted hot stage attachment. The growth of the nanoparticle took place on the order of

seconds and suggests a significantly shorter furnace heating scheme. Cube growth was also noted to take place at temperatures below that of the eutectic temperature of FeNd close to 650 °C which also suggests a revised heating scheme.

In terms of potential applications it was shown through using MFM that the array of nanocubes produced are indeed magnetic and that the presence of the intermetallic capping layer is not detrimental to core Fe magnetic properties. Indeed, this outer layer may prevent and/or inhibit oxidation and thus increase potential applications of these Fe nanocubes. For applications in magnetic memory storage or as bit patterned media the SEDG method will most likely have to be used in conjunction with a top down fabrication step such as e-beam lithography or mask indentation to accurately position cube growth.

4.8 References

1. *IBM 350 disk storage unit*. Available from: http://www-03.ibm.com/ibm/history/exhibits/storage/storage_350.html.
2. Shiroishi, Y., et al., *Future Options for HDD Storage.* Magnetics, IEEE Transactions on, 2009. **45**(10): p. 3816-3822.
3. Kolhatkar, A., et al., *Tuning the Magnetic Properties of Nanoparticles.* International Journal of Molecular Sciences, 2013. **14**(8): p. 15977-16009.
4. Beveridge, J.S., J.R. Stephens, and M.E. Williams, *The use of magnetic nanoparticles in analytical chemistry.* Annu Rev Anal Chem (Palo Alto Calif), 2011. **4**: p. 251-73.
5. Lu, A.H., E.L. Salabas, and F. Schuth, *Magnetic nanoparticles: synthesis, protection, functionalization, and application.* Angew Chem Int Ed Engl, 2007. **46**(8): p. 1222-44.
6. Reddy, L.H., et al., *Magnetic nanoparticles: design and characterization, toxicity and biocompatibility, pharmaceutical and biomedical applications.* Chem Rev, 2012. **112**(11): p. 5818-78.
7. Noh, J.-S., et al., *Hyperfine FePt patterned media for terabit data storage.* Current Applied Physics, 2011.
8. Sun, S., *Monodisperse FePt Nanoparticles and Ferromagnetic FePt Nanocrystal Superlattices.* Science, 2000. **287**(5460): p. 1989-1992.
9. Janbroers, S., et al., *A model study on the carburization process of iron-based Fischer–Tropsch catalysts using in situ TEM–EELS.* Applied Catalysis B: Environmental, 2011. **102**(3-4): p. 521-527.
10. Huber, D.L., *Synthesis, properties, and applications of iron nanoparticles.* Small, 2005. **1**(5): p. 482-501.
11. Borissov, D., S. Isik-Uppenkamp, and M. Rohwerder, *Fabrication of Iron Nanowire Arrays by Electrodeposition into Porous Alumina.* The Journal of Physical Chemistry C, 2009. **113**(8): p. 3133-3138.
12. Mohaddes-Ardabili, L., et al., *Self-assembled single-crystal ferromagnetic iron nanowires formed by decomposition.* Nat Mater, 2004. **3**(8): p. 533-8.
13. Fan, X.a., et al., *One-pot low temperature solution synthesis, magnetic and microwave electromagnetic properties of single-crystal iron submicron cubes.* Journal of Materials Chemistry, 2010. **20**(9): p. 1676.
14. Zhang, S.L., et al., *Silicon nitride films deposited from SiH2Cl2 • NH3 by low pressure chemical vapor deposition: kinetics, thermodynamics, composition and structure.* Thin Solid Films, 1992. **213**(2): p. 182-191.
15. Hong, S., *Surface energy anisotropy of iron surfaces by carbon adsorption.* Current Applied Physics, 2003. **3**(5): p. 457-460.
16. Wang, C.M., et al., *Morphology and oxide shell structure of iron nanoparticles grown by sputter-gas-aggregation.* Nanotechnology, 2007. **18**(25): p. 255603.
17. Jung, S.J., et al., *Surface energy driven agglomeration and growth of single crystal metal wires.* Nano Lett, 2011. **11**(3): p. 1294-9.
18. Jung, S.J., et al., *Free-Standing, Single-Crystal Cu3Si Nanowires.* Crystal Growth & Design, 2012. **12**(6): p. 3076-3081.
19. Ackerman, K.A. *High performance FeNdB Materials and annular geometries*. in *Electrical Insulation Conference and Electrical Manufacturing & Coil Winding Technology Conference, 2003. Proceedings*. 2003.
20. Okamoto, H., *Fe-Nd (Iron-Neodymium) Phase Diagram.* J. Phase Equilibria, 1997. **18**(3): p. 318.
21. Zhang, D., I.R. McColl, and J.V. Wood, *Diffusion reactions in the iron-neodymium binary alloy system.* Philosophical Magazine A, 1997. **75**(4): p. 959-974.

22. Kitayama, M., et al., *Modeling and simulation of grain growth in Si3N4. III. Tip shape evolution.* Acta Materialia, 2000. **48**(18–19): p. 4635-4640.
23. Vrij, A., *Possible Mechanism for the Spontaneous Rupture of Thin, Free Liquid Films.* Discuss. Faraday Soc., 1966. **42**: p. 23-33.
24. Anthony M. Anderson, L.N.B., *Foam Mechanis spontaneous rupture of thinning liquid films with plateau border.* Journal of Fluid mechanics, 2010. **658**: p. 63-88.
25. Sheludko, A., *Thin Liquid Films.* Adv Colloid Interface Sci, 1967. **1**(4): p. 391-464.
26. Danielson, D.T., et al., *Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration.* Journal of Applied Physics, 2006. **100**(8): p. 083507.
27. Sa, I., et al., *Thermodynamic analysis for the size-dependence of nanowire composition grown by a vapor–liquid–solid method.* Calphad, 2008. **32**(4): p. 669-674.
28. Mills, K.C. and Y.C. Su, *Review of surface tension data for metallic elements and alloys: Part 1 – Pure metals.* International Materials Reviews, 2006. **51**(6): p. 329-351.
29. Adhikari, H., et al., *Metastability of Au–Ge Liquid Nanocatalysts: Ge Vapor–Liquid–Solid Nanowire Growth Far below the Bulk Eutectic Temperature.* ACS Nano, 2007. **1**(5): p. 415-422.
30. Diebel, C.E., et al., *Magnetite defines a vertebrate magnetoreceptor.* Nature, 2000. **406**(6793): p. 299-302.

Chapter 5

Single TiO_2 Nanowires as a Unipolar Memristor Device

5.1 Introduction

Modern semiconductor memories are ubiquitous in today's society. The continued development of technologies such as random access memory (RAM) and erasable programmable read only memory (EPROM) have enabled hand held electronic devices to flourish. Used together, these technologies form the basis of mobile memory which leverages the speed of RAM with the long term memory retention of EPROM for better battery endurance [1]. RAM devices operate with great speed relative to EPROM. Typically RAM write/erase steps are on the order of nanoseconds with an endurance of 10^{16} cycles [1, 2]. These properties make them attractive for rapid cache computing, but any information stored within the device is lost once it is powered off. This type of memory is called volatile memory, and is useful for platforms where there is a continuous power supply such as desktop computers. EPROM technology is a type of non-volatile memory (NVM). Information is retained after the power is removed but it has drawbacks in comparison to volatile memory. These include a limited number of read/write cycles (~10^5 cycles) and much slower write/erase times on the order of milliseconds [2]. Therefore NVM is primarily used for facile data storage and transfer in USB Flash memory keys. Currently in mobile technology, a combination of both volatile and NVM are used to provide speed as well as long term memory [1]. However there is a need for a novel non-volatile memory device with endurance and write/erase speeds comparable to RAM, to limit power consumption in mobile devices.

5.1.1 Random Access Memories

Static RAM (SRAM) and dynamic RAM (DRAM) represent the current state of the art in volatile memory and both have undergone significant scaling down in size over successive device generations Figure 5.1 [1]. However, as the current generation approaches sub 20 nm feature size it becomes ever more difficult to improve circuit density and operation. These factors influence the cost of memory technologies and influence the choice of memory technology for device integration. Given a minimum feature size F, SRAM has a large footprint in comparison to similar technologies, with a minimum cell size of $140F^2$ consisting of 6 transistors. The 6 transistor set-up is key to its low power operation and cannot be altered significantly to reduce size [4]. This factor keeps the price of SRAM comparatively high relative to other technologies that have smaller footprints. Another popular RAM called dynamic RAM or DRAM is relatively smaller and therefore cheaper to produce with a cell size of $6F^2$. Its greatest drawback is poor energy efficiency during operation which directly affects battery life. The cell is composed of a single transistor and capacitor. The capacitor is used to hold information encoded onto it but it must be periodically topped up to retain this memory. This operation lends to unsustainable power consumption in mobile platforms. Therefore, having noted the limitations of SRAM and DRAM, it is obvious neither technology will suit mobile platforms sufficiently well for future generations of devices.

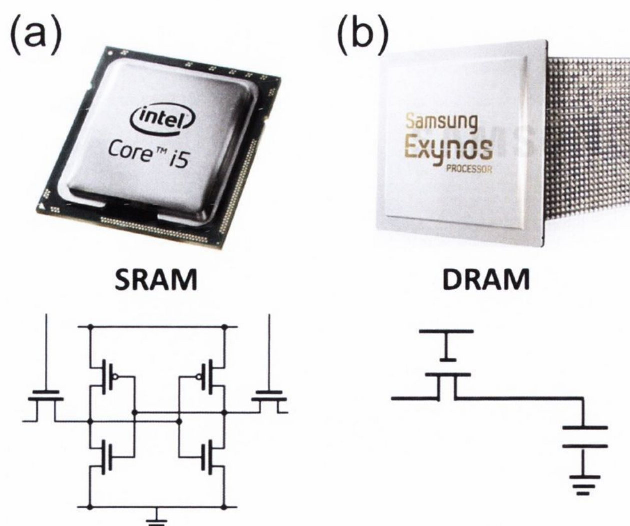


Figure 5.1 (a) Static RAM is extremely fast but has a large footprint with the low power consuming 6 transistor configuration. The large footprint makes it expensive and is primarily used in CPU cores like the Intel i5. (b) Dynamic RAM is a cheaper, slower and more power demanding RAM. Although popular in contemporary mobile platform technologies due to its price, its large power consumption is unsustainable through scaling generations.

There has been an increased interest in developing novel memory types that could satisfy the two main requirements of mobile platform devices namely small scalability/low price and low power consumption/efficiency. Many emerging semiconductor RAM technologies with these requirements are based on NVM operation. Their individual operation is based on many diverse physical mechanisms to retain encoded information states including magnetoresistance change, phase change, polarization change and resistance change phenomena [1]. The device properties speed and size of each are listed in Table 5.1. In this chapter the focus will remain on introducing the resistance changing phenomena or more commonly, resistive switching. A discussion of the operation principles of each memory type phenomena is beyond the scope of this chapter, reviews by Waser *et al* and Jeong *et al* cover each memory phenomena comprehensively [2, 5].

5.1.2 Resistance Switching RAM

Resistance switching memory – ReRAM or RRAM is a specific type of RAM technology that operates on the principle of an externally applied voltage or current inducing a change in conductivity of the active material within the device [5]. The change in conductivity of the active material is correlated with a dynamic resistance change measured across the device. Examples of TiO_2 based resistance switching devices are shown in Figure 5.2. The typical resistance level changes are orders of magnitude in difference. In the high level resistance state or 'off' state, the active medium has a prohibitively large resistance that prevents significant levels of current passing through the device. This off state will remain until a sufficiently large or persistent external stimulus alters the physical properties of the active medium. Typically the voltage/current stimulus induces a chemical change in the matrix of the active medium by either creating defects, moving mobile ions or altering crystal structure. The stimulus required to elicit this change is often called the forming step [5].

After the forming step has been performed, the device displays notably more current, associated with a large change in resistance or a switch from the off to the on state. The on and off states of the resistance switch material are used to correlate with computational binary 1 and 0 states for information processing and storage. The resistance level in the material and therefore the binary information remains as long as the chemical change brought on by the forming step persists.

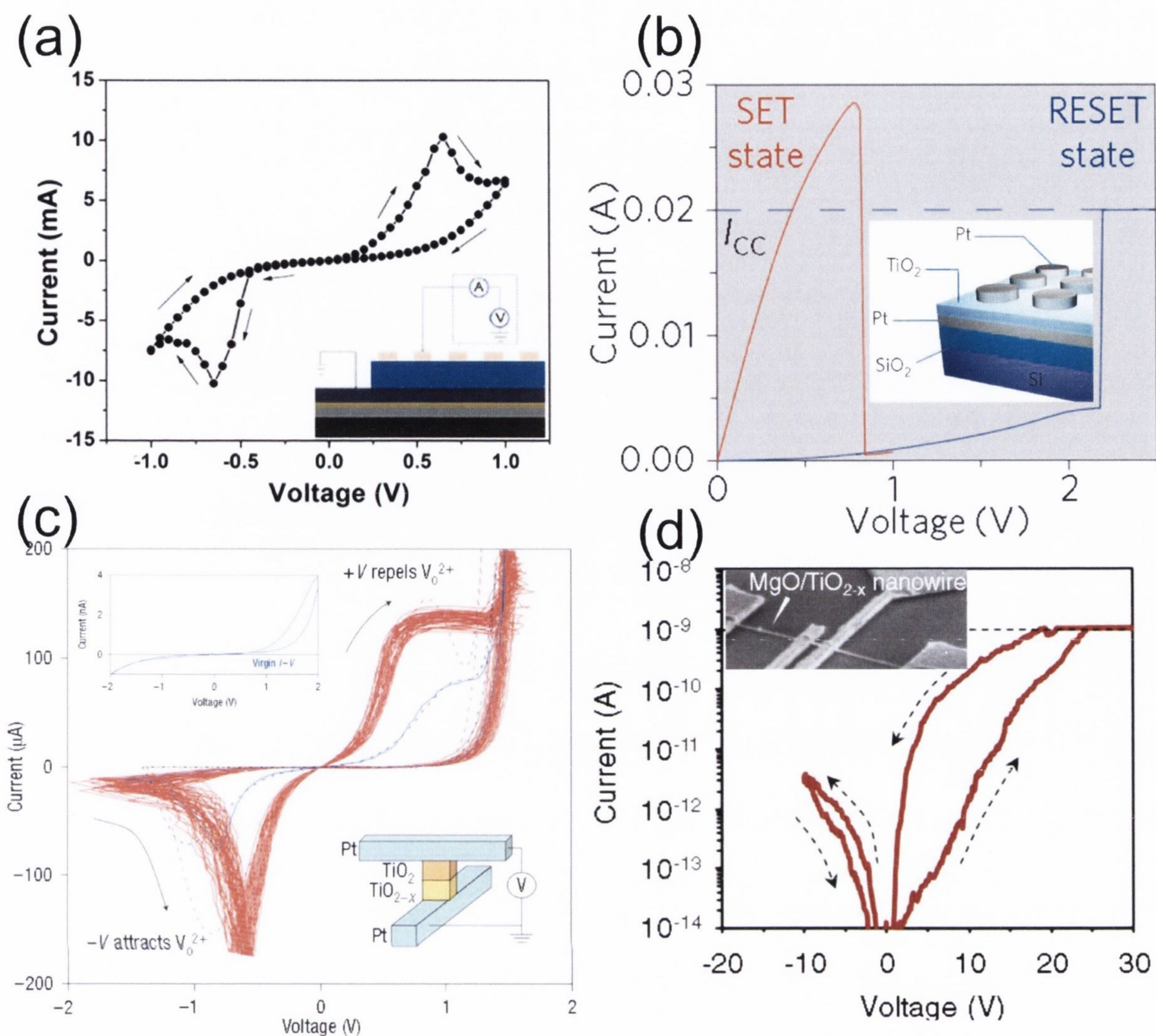


Figure 5.2 Resistance switching devices in literature based on TiO_2. (a) A device with a 20 nm thin film of TiO_2 contacted with TiN and Pt electrodes [6]. This device displays interesting negative differential resistance behaviour. (b) A 40 nm thick film of TiO_2 sandwiched between two Pt electrodes completes this device [7]. The device was used to observed the conductive filaments caused during switching events in the TiO_2. (c) A thin bilayer film device with 50 nm of TiO_2 with a 15 nm process induced oxygen deficient TiO_{2-x} layer [8]. (d) A device composed of a single MgO nanowire coated with a 5 nm thick TiO_2 shell layer [9].

The actual forming mechanism that induces the resistance change in the active material is still poorly understood [10]. There are many proposed mechanisms to explain the resistance switching action under applied stimulus and they may vary by material [2, 5, 10, 11]. These mechanisms are supported by evidence for individual resistance switching systems. Only some aspects of each individual resistance switching system can be applied to the broader range of switching material [11]. The two most popular and well developed mechanisms for describing resistance switching are the filamentary growth/rupture process and the interfacial doped process, shown schematically in Figure 5.3.

Table 5.1. The operational parameters of conventional volatile and non-volatile semiconductor memories are presented in this table along with those of novel developing non-volatile memories [1]. SRAM is the fastest type of RAM memory available at the moment. It is primarily used in CPU cores due to its speed but its large footprint means the device remains relatively expensive. DRAM is used as a cheaper alternative with compromise of speed and power efficiency. It is used in mobile platforms such as mobile phones but power efficiency is becoming an increasingly difficult issue as the technology scales smaller. Flash memory is an incumbent well recognised memory technology, primarily used for personal data storage and transfer. PRAM operates on the principle of a dynamic phase change in the active material of the device for large stable resistance switching. The devices first appeared in the 1960s [3] but has yet to be developed into a viable memory due to large power requirements to prompt the phase transition. FRAM and MRAM are magnetic based memories. Data is stored as magnetic moments or permittivity change as opposed to electrical signal. Ferroelectric RAM operates similar to that of DRAM with a magnetic material holding a magnetic polarisation. Problems remain in the deposition of the magnetic material in a reproducible and scalable manner. Magnetic RAM is akin to a transistor, two magnetic plates are separated by an insulating layer. The polarity of one of the plates is dynamically altered in order to change the permittivity of the insulating layer between them to store memory. This process requires relatively high current however. RRAM memory is based on resistance switching between high and low resistance states. Its main advantage is considered its small footprint, but the forming step required to activate these devices can damage the cell due to the sudden power dissipation.

	Volatile Memory		**Non-Volatile Memory**		**Developing Non-Volatile Memory**			
Type	**SRAM**	**DRAM**	**NOR-FLASH**	**NAND-FLASH**	**PRAM**	**FRAM**	**MRAM**	**RRAM**
Application	CPU Cache	RAM	USB Data Storage	USB Data Storage	Memory	Memory	Memory	Memory
Advantage	Very high Speed	Inexpensive	Storage	Speed	Mature Technology	Cycle Lifetime	Cycle Lifetime	Small Size
Disadvantage	Cost	High Power	Low Retention Time	Low Retention Time	High Power	Difficult Integration	High Current	Forming
Min. Size	$140F^2$	$6F^2$	$10F^2$	$5F^2$	$5F^2$	$22F^2$	$20F^2$	$4F^2$
Max Cycles	10^{16}	10^{16}	10^5	10^5	10^8	10^{14}	10^{16}	10^{10}
Write time	0.3 ns	10 ns	1 ms	1 ms	20 ns	10 ns	10ns	5 ns
Erase time	0.3 ns	10 ns	10 ms	0.1ms	50 ns	10 ns	10 ns	5 ns

The first mechanism occurs during the course of forming the device. A conductive filament (CF) is formed in the matrix between the two contacts. This filament has a low resistance relative to rest of the matrix material presenting a low energy pathway for conduction. To switch the device off again requires a stimulus that will rupture this filament. Successive on/off switching cycles bridges and breaks the conduction path. In the case of conductive filament switching, holding a bias across the active material promotes redox reactions within the matrix lattice at the electrode [11]. Charged mobile ions are created initially at the interface and act as dopants. Internal imperfections in the matrix such as contact roughness may cause internal electrical fields to be non-uniform throughout the matrix [12]. This is believed to impact the position of the first dopants created, and their ability to grow into filaments. The CF growth may proceed via a winner takes all process whereby the largest CF will continue to grow via higher electric fields in its vicinity in a process analogous to neuron strengthening in mammalian brains [13]. When the CF is ruptured it is believed to remain largely intact save a few crucial bridging atoms. These bridging atoms are reduced and oxidized as the CF is broken and remade locally as the device is switched off and on respectively .

The second proposed mechanism is an interfacial type conduction path. Initially intrinsic dopants are introduced into the matrix by the same route as CF formation – redox reactions at the electrode or via Joule heating [14]. In contrast to CF however no site at the interface preferentially promotes local redox reactions needed to produce a filament. Instead the electrode interface is homogeneously doped to a depth w [15]. The width of this region can be controlled externally as the dopants drift under voltage stimulus in a direction defined by the polarity of the applied bias. The doped region has lower resistance compared to the pristine region. Overall the resistance of the device is lowered due to creation of this doped region at the interface. There is no broad agreement about the type of electronic conduction enhanced by the local build-up of ionic dopants at the interface. Variable range hopping, electronic tunnelling, and thermionic emission mechanisms are most likely to increase device conductance within the device at the doped interface and the broader parts of the device (non doped regions and contacts) [4]. Resistive switching in the case of interfacial conduction change is manifested by a large dopant region width spanning the majority of the device [15]. The device switches on as the doped region dominates the resistance of the overall device. To switch the device off once more the dopant region width must be made smaller under the action of a bias. This also has the effect of destroying some of the dopants by the reverse redox reaction that created them at the interface [16].

The doped and non-doped regions of the device can be considered as two resistors in series with the total device resistance defined as the sum of the two. The non-doped region will have a single value resistance and the doped region will have a variable resistance dependent on the dopant concentration (which is a function of total history of applied voltage). The doped region will therefore have a history dependant resistance or memory resistance (memristor). This may be used to define a continuum of resistance states within the device opposed to just low resistance 'ON' states (LRS) and high resistance 'OFF' states (HRS) observed in CF resistive switching.

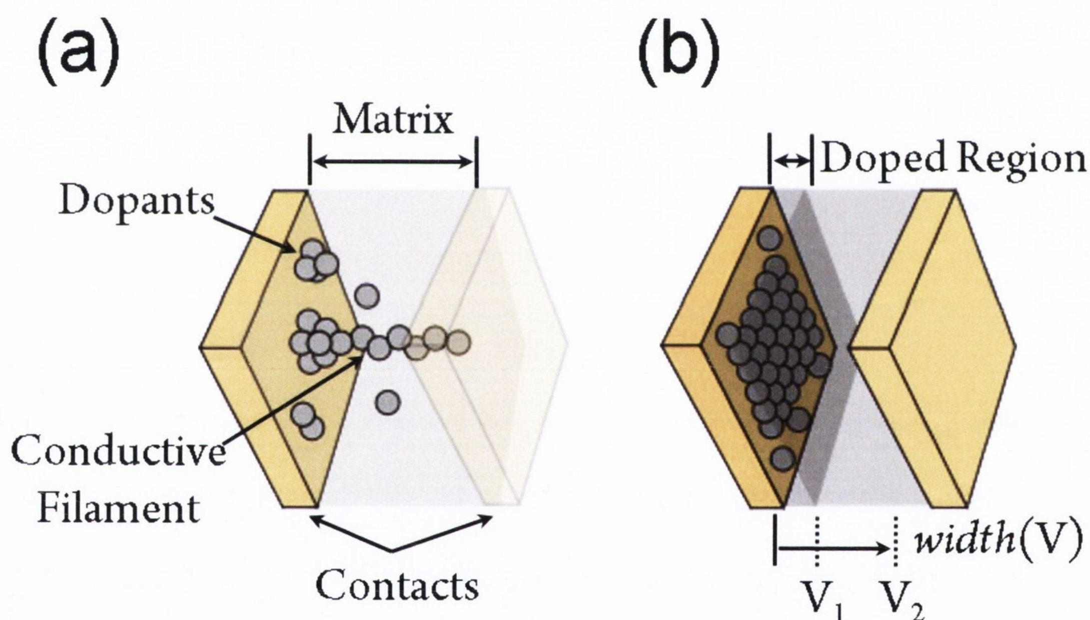


Figure 5.3 A schematic describing both conductive filament and interfacial switching mechanisms. (a) During electroforming, dopants are electrochemically introduced into the matrix material spanning the distance between the two electrodes. Non-homogenous distribution of the electric field within the matrix may lead to a preferential site where a strong filament grows at the expense of others. Once the filament spans the matrix the device is said to be formed. At this point the device is in the on or low resistance state and resistive switching can proceed via cycles of breaking and rebridging the filament. (b) Dopants created during electroforming are homogenously distributed around the interface of the anode contact metal. These dopants form an interface region with a set width w after electroforming. The width of this region can be changed dynamically as more dopants are introduced at the interface and the dopants already present drift under an applied voltage bias.

5.1.3 Memristors

To date many of the reported RRAM devices hailed as memristors display bistable resistance switching with little difference in the conduction value of the ON state, i.e. no continuum resistance. These devices are typically planar consisting of a thin TiO_2 layer (50 nm thick) sandwiched between two metal contacts. This technology is currently being developed for market applications by several companies, with Hewlett Packard intending to ship memristor devices by 2017 [17]. While these devices are attractive in terms of their non-volatile memory retention, they ignore the potentially greatest aspect of RRAM technology – multilevel functionality. In this study different device configurations that may facilitate these novel functionalities will be presented. A memristor is a specific subset of RRAM technology that displays memory and learning properties. The physical operation is based on the movement of charged ionic dopant species in the lattice under applied stimulus [15]. This allows the end user to define the position of the ionic dopants and therefore the resistance level of the memristor as a function of applied stimulus. To describe this behaviour an interfacially doped memristor is considered, which can be considered as two resistors in series as shown in Figure 5.4. The second resistor represents the bulk resistance of the device set by the pristine material while the first resistor has a resistance value based on the width of the doped region and the total number of dopants in that region. Both factors that define the resistance of the doped region are a function of the history of voltage stimulus applied to it. Ohm's law does not adequately describe the behaviour of such a history dependent resistor. In principle, a memristive device can operate along a continuum of resistance states between the traditional HRS and LHS found in conventional resistive switching devices, with the evolution of the resistance state controlled by the flow of charge or voltage flux through the device. In practice, the level of performance has yet to match that described in memristor simulations [18, 19]. However, if reliability can be improved, memristors have the potential to enable novel multilevel or multibit coding paradigms, storing more information per unit memory cell and maintaining this information without consuming power.

Leon Chua, a pioneer in the field of memristors, first predicted their existence in the 1970s [20]. Chua developed equations to capture the history dependence of a memristor [21], which are introduced as expressions describing the time integrals of current and voltage to produce both charge and flux equations.

$$q(t) \triangleq \int_{-\infty}^{t} i(\tau)d\tau \tag{5.1}$$

$$\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)d\tau \tag{5.2}$$

Equation (5.1) captures the time dependence of the value of charge q passed through a conductor and is described as the time integral of the amount of current i that has flowed in a conductor during a given time period τ. Equation (5.2) is not as intuitive as the charge equation. Chua arrives at equation (5.2) based on the mathematical generalisation of flux resulting from a field which in this case is the voltage through a conductor [21]. Its physical interpretation is limited as there is no standard electrostatic definition that relates an electric field or voltage to a time varying flux [20]. Its closest physical analogue is Faraday's law which states "the induced electromotive force (voltage) in any closed circuit is equal to the negative of the time rate of change of the magnetic flux through the circuit" or $V = -{}^{d\Phi_B}/_{dt}$ [22]. Nonetheless equation (5.2) is assumed to describe a flux φ of voltage v through a memristor.

Equations (5.1) and (5.2) are useful for deriving the constitutive relations or basic equations that describes the behaviour of a memristor-like device. If the constitutive relations can be expressed in terms of charge q or flux v the memristor device is termed charge-controlled or flux-controlled respectively.

$$\varphi = \hat{\varphi}(q) \tag{5.3}$$

$$q = \hat{q}(\varphi) \tag{5.4}$$

Equation (5.3) describes a charge controlled memristor and equation (5.4) describes a flux controlled memristor. Equation (5.4) is now differentiated with respect to time.

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = G(\varphi)v \tag{5.5}$$

$$\frac{d\hat{q}(\varphi)}{d\varphi} = G(\varphi) \tag{5.6}$$

Where $G(\varphi)$ is the memductance (memory-conductance) at φ with units of Siemens (S, Ω^{-1}). Equation (5.5) is analogous to Ohms law with a flux dependent term. The flux dependent term incorporates the complete history of flux applied to the device which is captured by the time integral in equation (5.2). Deriving a constitutive equation that captures the behaviour of a memristor is quite involved due to the complex current switching response, namely $i(t)$ is difficult to model in response to a standard $v(t)$. Attempts at simulation and derivation of the nanowire devices presented in this chapter will be discussed in a later section.

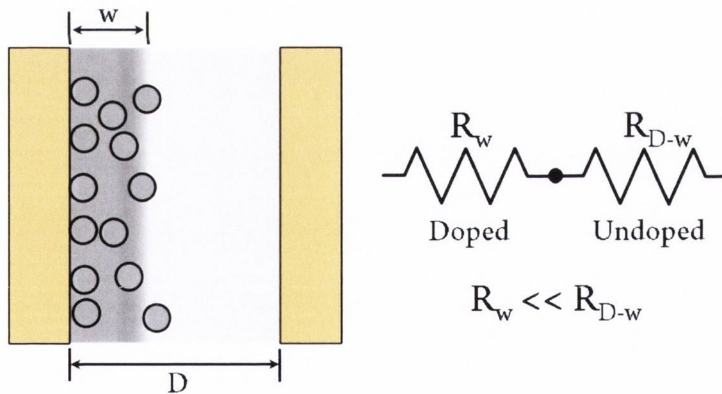


Figure 5.4 Schematic describing two resistors in series model for an interfacial memristor. The two region within the device are described by an individual resistor. The undoped region reflects the resistance value of the pristine matrix material or the off value resistance. The region containing the dopants has a much lower resistance value relative to the undoped region. As the memristor is stressed electrically, the width of the doped region increases or decreases depending on the polarity of the bias. Under this action the device dynamically changes resistance in response to applied bias.

5.2 Device Fabrication

5.2.1 Sample Preparation

Single nanowire devices are fabricated following a three step process of UV lithography that involves defining contact pads, nanowire spray deposition and electron beam lithography (EBL) to define metal contacts to the wires. Devices were fabricated on silicon substrates with 200 nm oxide thickness. UV lithography was used to produce 150 μm2 Ti/Au metal contact pads with metal thickness of 5/30 nm respectively. Commercially available TiO_2 wires from EMFUTUR, with diameter 50 nm length 5-10 μm (TiO_2-E), and Novarial Materials, with diameter 100 nm length 1-10 μm (TiO_2-D), were used separately to produce nanowire devices. Both wire batches were comprised of uniform single crystal anatase phase wires as shown in Figure 5.5. TiO_2-D wires arrived as a wet white powder already dispersed in water in a 1:10 ratio. Approximately 0.02 g was added to 10 ml DI water to produce a TiO_2-D dispersion for hand spraying. These dispersions were not stable however despite many sonication attempts white material remained at the bottom of the dispersion container. TiO_2-E wires arrived as dry white powder. To disperse them approximately 0.002 g of powder was added to 10 ml DI and hand shaken until all large powder clumps were broken up and dispersed (~30-60 mins), followed by 1 minute sonication at 37 kHz 100% power and 1 minute 80 kHz 100%. TiO_2-E dispersions remained stable for longer compared to TiO_2-D dispersions. TiO_2-D wires appear to still have some material left over from the synthesis remaining in wet white power shipped product. Although they also displayed similar electrical behaviour to that shown in the rest of this chapter they were less frequently. TiO_2-E wires appeared cleaner with less additional unknown material present on the substrate after spraying compared to TiO_2-D solutions.

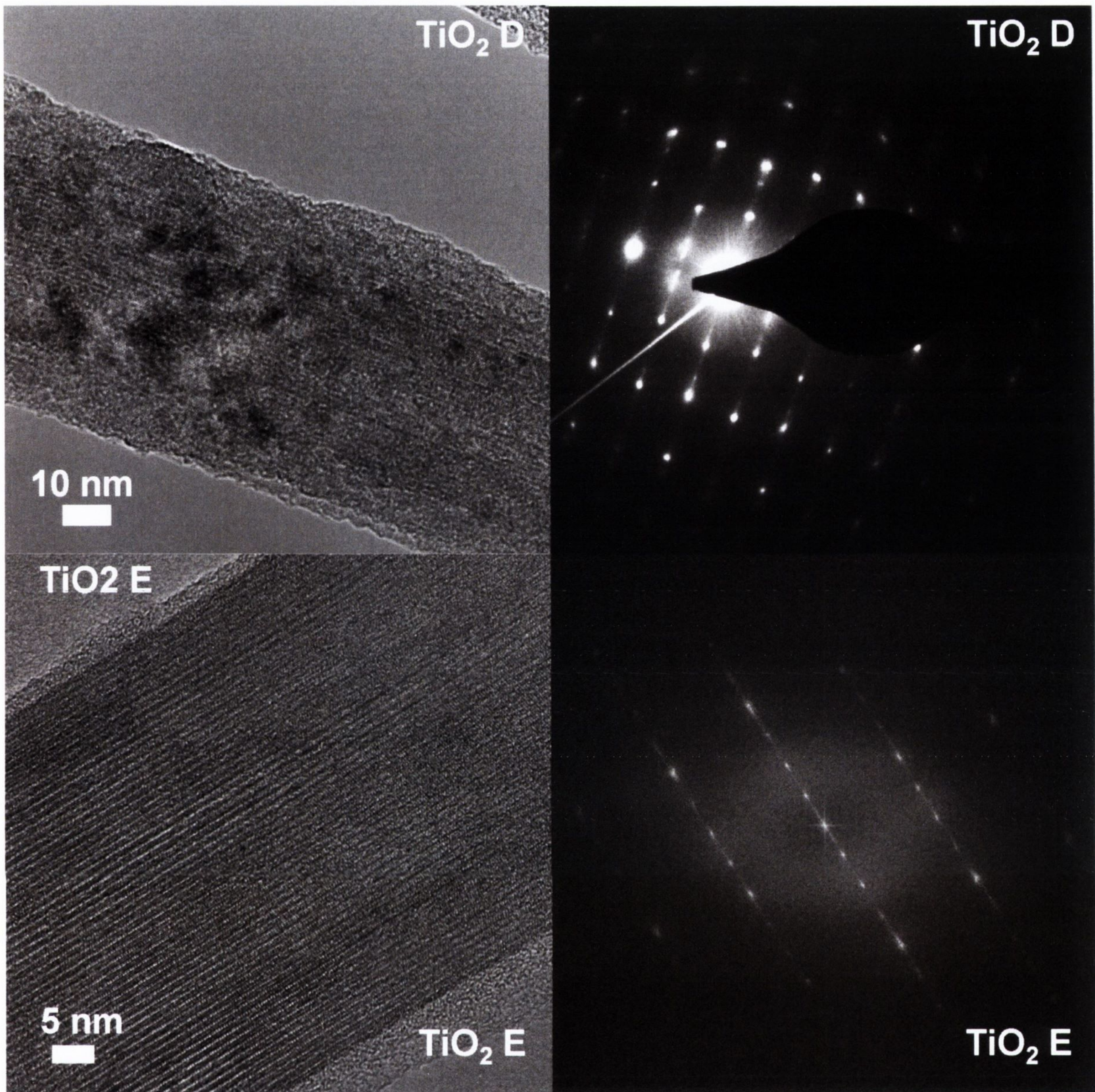


Figure 5.5 TEM, SAED and FFT images performed on two separate batches of TiO_2 nanowires obtained from different suppliers. The crystalline nature of each batch of wires was first observed under HR-TEM and confirmed using diffraction and FFTs.

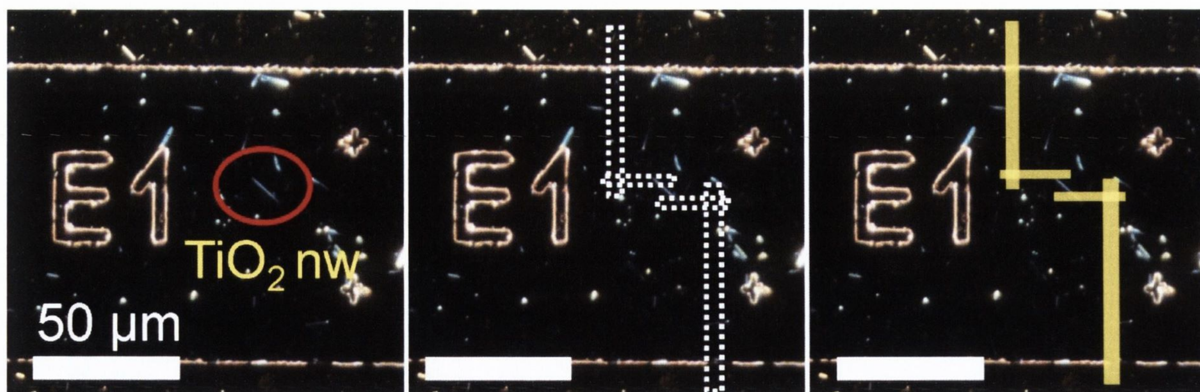


Figure 5.6 Hand sprayed TiO_2 nanowires are photographed under an optical microscope at x50 magnification. Once a suitable isolated nanowire is found, the image is then used to establish scale and coordinates to define contact leads up to the wire. Post-EBL the photoresist is developed and the sample is metallised with 80+ nm of Au for electrical measurements.

5.2.2 Hand Spray and Contacting

The hand spraying and electrical contacting procedure is shown in Figure 5.6. Hand spraying was performed using approximately 0.5 – 1 ml TiO_2 dispersions at 3.8 bar back pressure. Samples were sprayed in increments until a sufficient amount of long wires were present between the prefabricated large contact pad electrodes. After spraying was completed, images of long isolated TiO_2 wires were photographed in optical microscope under x50 magnification. These images were then used to define EBL write masks needed to electrically contact the single wire. Au metal contacts 80 nm thick were deposited in order to complete the device.

5.2.3 Electrical Characterisation

Electrical measurements were performed on the single nanowire devices using a 2-point probe setup with a Keithley 4200-SCS parameter analyzer. Electroforming steps were carried out by applying 10 V with a 1 nA compliance for approximately 1000 seconds. Typical triangle wave voltage sweeps were performed at a sweep rate of 0.23 V/s with a magnitude of 10V. Frequency dependence was investigated by varying the sweep delay between points that comprise a 20 point triangle wave voltage pulse. Very low frequency AC impedance measurements were carried out as prescribed by the VLF C-V application note and involved the application of a 350 mV AC modulation at 10 Hz.[23]

5.3 Results

5.3.1 Basic Electrical Behaviour

Each device consisted of a single crystal TiO_2–E nanowire and two Au contacts, as shown schematically in Figure 5.7 (a). As the inset shows, the distance between the two electrodes was close to 2 μm and was the average channel distance for these devices. This distance was chosen to maintain a high EBL throughput. In contrast to many thin film TiO_2 devices our nanowire devices use symmetric metal contacts without a process-induced oxygen deficient interface between the TiO_2 and metal contact [8, 24]. Therefore when testing each sample initially, one ground electrode was arbitrarily defined and remained grounded throughout its lifetime. In the virgin pristine state the device is a poor conductor. To probe the initial state of the virgin device, a +10 V sweep is applied at a rate of 0.23 V/s (total time ~130 s) while the current levels are monitored. Current typically ranges from 10–1000 pA for individual devices in the initial sweep. The black curve in Figure 5.7 (b) shows a typical current trace for a virgin device. The current rises above the noise threshold level at around +7 V during the initial voltage sweep, and there is clear hysteresis in the current trace as the bias is swept to +10V and then back to 0V. The direction of the hysteresis loop is indicated by the arrows in Figure 5.7 (b).

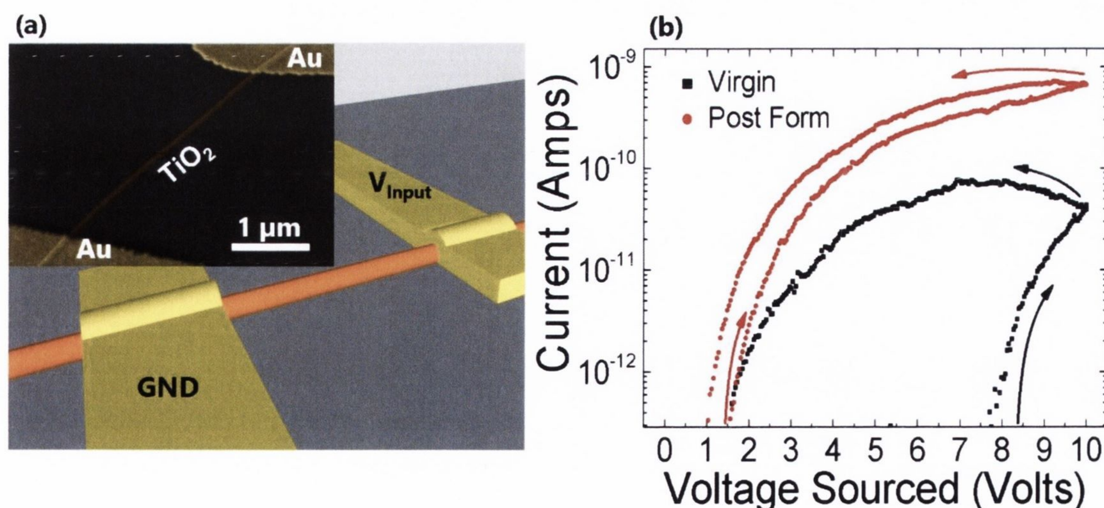


Figure 5.7 (a) A schematic of a typical nanowire device showing a single TiO_2 nanowire spanning two Au metal contact pads. Inset is an electron microscope image of a typical TiO_2 nanowire junction device. (b) The current response of a virgin single TiO_2 nanowire device to a 10 V voltage sweep both before and after carrying out a +10 V forming step on the wire. The device is shown to be more conductive after the forming step has been carried out.

The current levels within the nanowire device can be significantly increased by undergoing an electroforming step similar to those used for planar thin film TiO_2 devices.[7, 16, 24] This involves the application of a steady state voltage (typically +10V) for a sustained time period (typically 1000 s) while the current is monitored with a set compliance limit of 1 nA. The red curve in Figure 5.7 (b) shows the difference in current levels for the same device before and after the forming step. The maximum current is increased and the turn-on voltage is reduced to +1.5V, comparable to the turn-off voltage for the device in its virgin state. This electroforming step changes the properties of the wire in the vicinity of the positively biased electrode (see below) and increases the overall conductance of the device. Similar behavior is observed for a device under negative bias conditions, except that the modification of the wire occurs at the electrode that is grounded, see Figure 5.8 below.

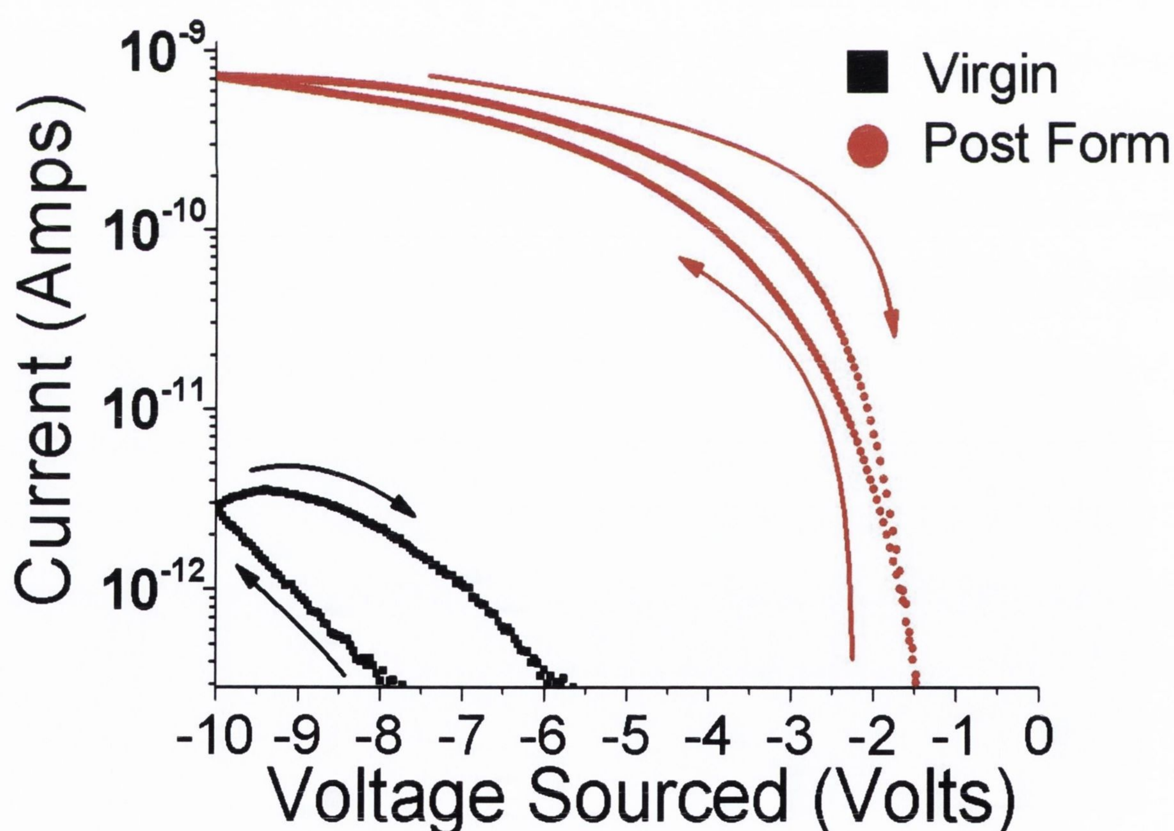


Figure 5.8 The polarity of an applied voltage bias does not have a significant effect on the initial device behavior tested in the virgin state. Initially the turn on voltage at -8 V and turns off again at -6 V. After forming the device at -10 V both the turn on and turn off voltage collapse to -1.5 V, similar device behavior at positive bias.

5.3.2 Effect of Electrode Metals

The effect of the electrode material on the behavior of the device was also investigated by employing Ti and Pd metal electrodes instead of Au during fabrication. The initial voltage sweeps and forming steps were the same as before, carried out in ambient. The electronic characteristics were not the same however. Firstly, there is a large difference in the yield of "active" nanowire devices per chip depending on the contact metal used. Typically for Au contacted nanowires the yield of active devices - devices that show hysteresis and respond to electroforming - was about 28%. Up to 25 nanowires are contacted on an individual chip per EBL session. A summary of device properties for different contact electrode material is shown in Table 5.2. Notably Ti metal contacts produced the highest yield of active devices per chip ~ 75%. This may be due to the material similarity of Ti and TiO_2 enabling favorable adhesion to the wire and therefore good electronic contact formation. However, Ti contacted devices continued to degrade as the total voltage flux through the device increased, and became worse the more they were tested. SEM images shown in Figure 5.9 reveal a clue not only to the electrical degradation of the device but also to the chemistry taking place at the TiO_2 contact metal interface. Pronounced 'bubbling' is observed at the device anode or positively biased electrode, consistently for all Ti contacted nanowire devices held at positive bias for a long time period. The physical origin of the observed bubbling will be revisited in the memristor mechanism section.

Bubbling was not observed for devices contacted with either Au or Pd metals. Indeed both are well known inert metals commonly used to prevent excess oxidation or minimize consumption when acting as a catalyst. The yield of active devices for Pd contacted devices was considerably lower than that of Ti or Au contacts, 15% . This is ascribed to the poor adhesion of Pd metal. As a deposition material for contact electrodes and other applications it is rarely deposited without a dedicated adhesion layer to improve its adhesion to the substrate. Overall Au offers the best return on yield per device by offering good adhesion and chemical inertness. In an effort to maximize yield 1 nm Ti was deposited prior to Au deposition. This was thought to combine the good adhesion with high yeild reflected in the Ti electrodes the inert nature of Au. The results were poor, only matching the device yield of ~25% for Au only contacted devices and performing worse electronically. These devices displayed less hysteresis or response to electroforming steps. Thus pure Au metal contacts were used for all remaining device fabrication.

Table 5.2 Statistics gathered during fabrication and testing of nanowire devices contacted with various metals. N is the total number of viable devices after fabrication. Initially active devices refers to the total amount of devices that displayed hysteresis during the virgin voltage sweep. Ti metal contacted devices posting the greatest yield. Post forming is the amount of initially active devices that remained active after the 10 V forming step was applied. Ti metal contacted devices that were initially active performed poorly following forming. Current measured from these devices was observed to decrease with time as the forming process progressed.

Metal	Au	Ti	Pd	Ti/Au
N	18	12	7	12
Initially Active	28%	75%	15%	25%
Post forming	28%	50%	15%	25%
Device Yield	28%	50%	15%	25%

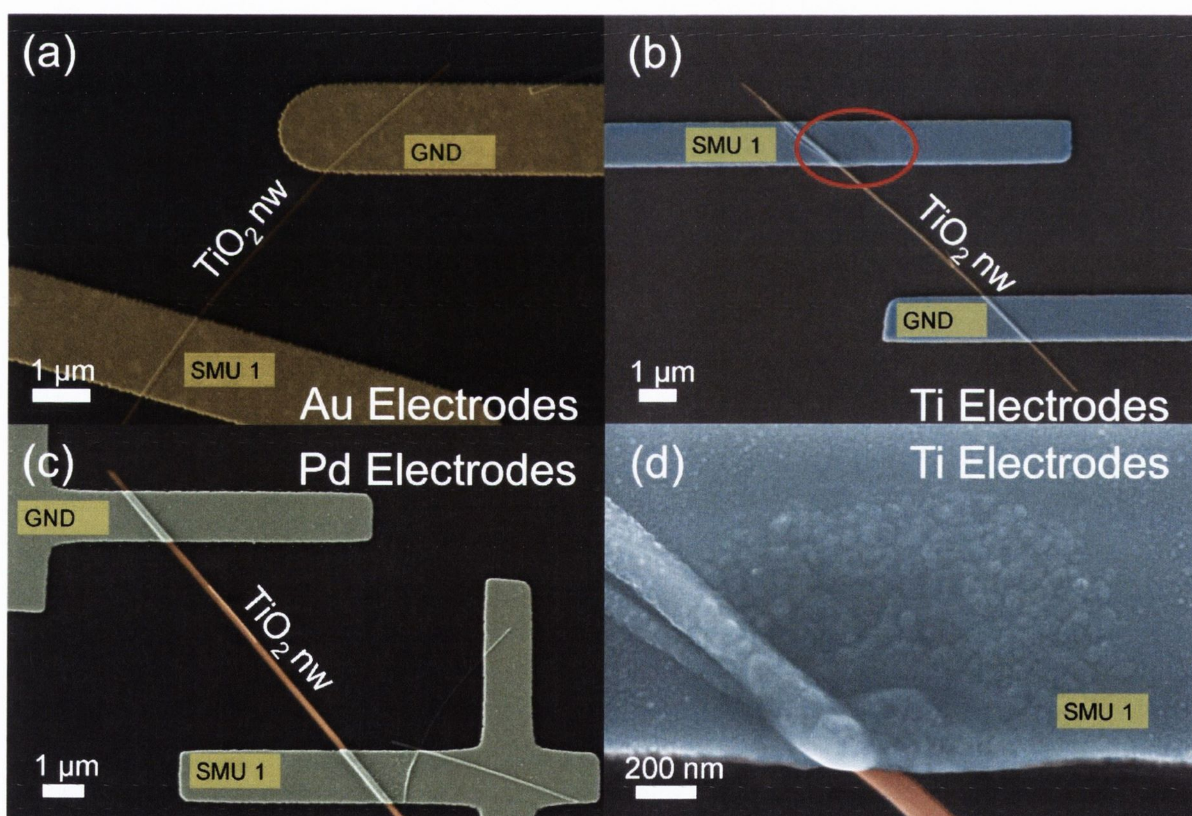


Figure 5.9 SEM images of various nanowire devices contacted with different metal electrodes. (a) Au contacted nanowire. (b) Ti contacted nanowire with bubbling feature circled in red at the anode (SMU 1). (c) Pd contacted nanowire. (d) A high magnification image of the bubbling feature circled in red in (b) reveals the modified texture in the metal contact around the wire.

5.3.3 Dynamic Current Response

Current levels within the device can be developed further by successive electroforming steps at higher set compliance values or through continuous and repeated application of voltage sweeps. Continuous voltage sweeps reveal the dynamic behavior of the nanowire device and also provide insight into the physical mechanism of operation. Figure 5.10 (a) shows the evolving current response to a series of 8 voltage sweeps. The conductance of the device increases incrementally with each applied sweep, up to a maximum conductance value. By the 8th sweep, the current levels no longer increases with additional voltage sweeps, and the device response collapses into a stable repeating hysteresis loop. The turn-on and off voltages also collapse onto a single value, +1.5 V in this case. Under this condition, the device remains in a stable or 'saturation state' (SS). All devices display this dynamic behavior in response to repeated voltage sweeps. The SS condition provides a useful reference state for the device, to which the device can always be returned. This is important for a dynamic memristor-like device which, by its nature, is susceptible to changing state in response to the voltage, current, and sweep rate conditions it is exposed to. The SS represents a stable reproducible state in an otherwise dynamic and continuously evolving device operation space.

Changing the frequency of the applied voltage sweep also greatly affects the electrical properties of the device, as seen in Figure 5.10 (b). In each instance the device was brought to the SS associated with that frequency. The different traces in Figure 5.10 (b) have been offset for clarity. The maximum sweep rate is 5 Hz, which is slow but reflects the > 2 μm size of the device. Altering the frequency of the applied voltage sweep affects two aspects of the device current-voltage response. Firstly the maximum current becomes diminished for faster voltage sweeps while secondly, the breath of the hysteresis loops become notably collapsed at higher frequencies. Both behaviors are characteristic properties of memristors as described by Chua and Williams *et al*, despite the fact that our device does not have the conventional two-electrode sandwich memristor geometry.[15, 21]

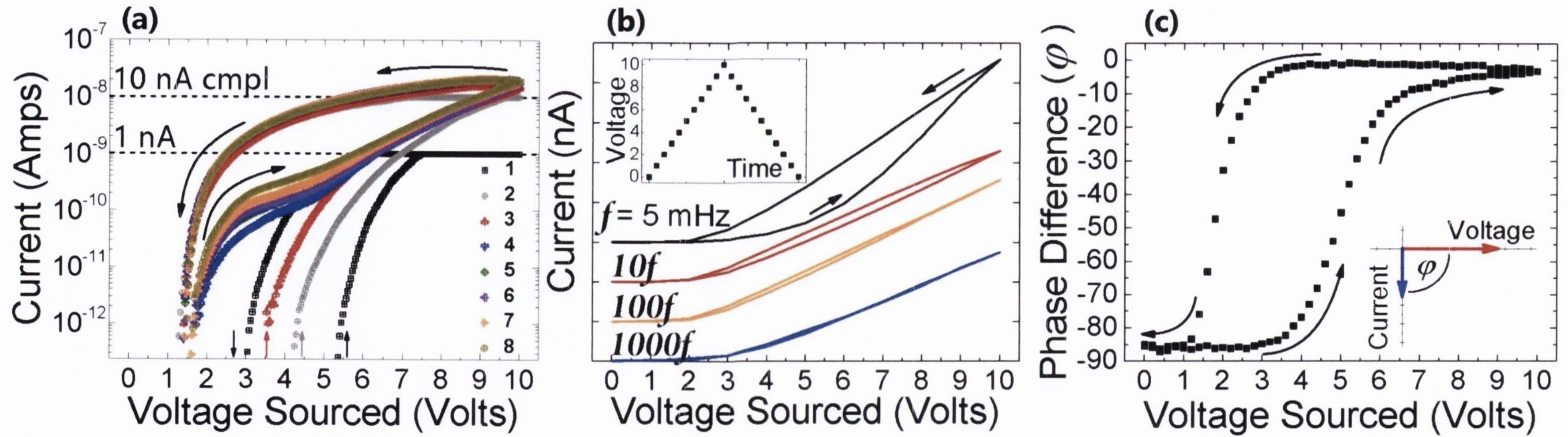


Figure 5.10 Many properties of a memristor depend heavily on the electrical stimulus and the device history. In (a) the evolution of the current response of the nanowire device to the same voltage pulse is shown for a sequence of 8 pulses performed directly after each other. The first and second voltage sweeps hit 1 nA and 10 nA compliances respectively; each subsequent sweep increases the maximum current within the device until a pseudo-steady-state saturation point is reached whereby the current is no longer changing. This saturation point was used as a point of reference for further experiments. (b) As the frequency of the applied voltage sweep increases, the current at saturation for each individual sweep frequency decreases. Hysteresis in the current loop is also observed to decrease with increased sweep frequency. (c) Performing a 10 V DC sweep with a small signal 10 Hz 0.35 V AC component at each point allows the change in device behavior be observed as the sweep progresses. For capacitive circuits the current is -90° out of phase with the driving voltage, a dynamic shift is observed changing from a purely capacitive device to a purely resistive device during the voltage sweep.

Figure 5.10 (c) shows the phase angle between the drive voltage and current recorded during the measurement of the SS in Figure 5.10 (a). A phase angle of -90 degrees is consistent with a capacitive response that dominates the initial low voltage behavior of the device, however at larger voltages the response is resistive indicating the establishment of improved electrical conduction between wire and the metal contact. This behavior is consistent with the presence of a blocking capacitor at the device interface that becomes increasingly transparent at high applied voltages.

5.3.4 Multi-level Memory Device

Figure 5.11 (a) shows the response of a device specifically prepared to be in the SS at positive bias to a bipolar voltage sweep. As expected, the device initially displays the SS response during first positive voltage sweep (red curve labelled 1 in Figure 5.11 (a)), similar to the response seen in Figure 5.10 (a). On the other hand, no significant level of current is observed during the negative voltage sweep (2), indicative of diode-like behavior. The second positive voltage sweep (3) reveals a current response albeit at a lower level than that observed in the first sweep. Our device is therefore essentially a unipolar memristor, and thus the application of a negative voltage pulse can be used to systematically step back or reduce the conductance at positive biases. Note however that the application of a sustained negative voltage eventually quenches the device conductance in the positive voltage direction, resulting in the growth of the same device characteristic seen in Figure 5.10, except at negative voltages with the electroforming phenomenon at the grounded electrode (see Figure 5.8).
This ability to reset or step back the conductance in the forward channel by applying a reverse bias pulse is not available in conventional memristors and enables improved control of device operation and enhanced performance. Thus a -7.5V pulse can be applied to reset the device, following which the device response to a subsequent series of positive set pulses is examined. Figure 5.11 (b) shows the combined effect of a -7.5 V reset followed by five +7.5 V set pulses for a device that was originally in its SS defined by a 18 nA saturation current at +7.5 V. The pulse is 2.5 sec in duration. Each positive voltage pulse increments the device conductance by a specific amount while the device can be quantitatively reset using a negative pulse. The resulting six-level memory device in Figure 5.11 (b) has high current fidelity and precisely controlled levels compared to previous multilevel memory devices.[25, 26] The observed on-off ratio is excellent, as expected for high-purity TiO_2.[27] Figure 5.11 (c) shows the time

evolution of the six-level memory device from the beginning of the pulsing sequence. Note that the device response evolves during the initial cycles, but beyond 60 pulse applications it saturates into six well defined conductance levels, from which the data in Figure 5.11 (b) were recorded. This initial behavior is consistent with that seen earlier in Figure 5.10 (a) and typical of memristor devices in general,[15] which exhibit a temporal response to any voltage stimulus. Critically, the relative separation between the memory levels remains unchanged even during the initial period.

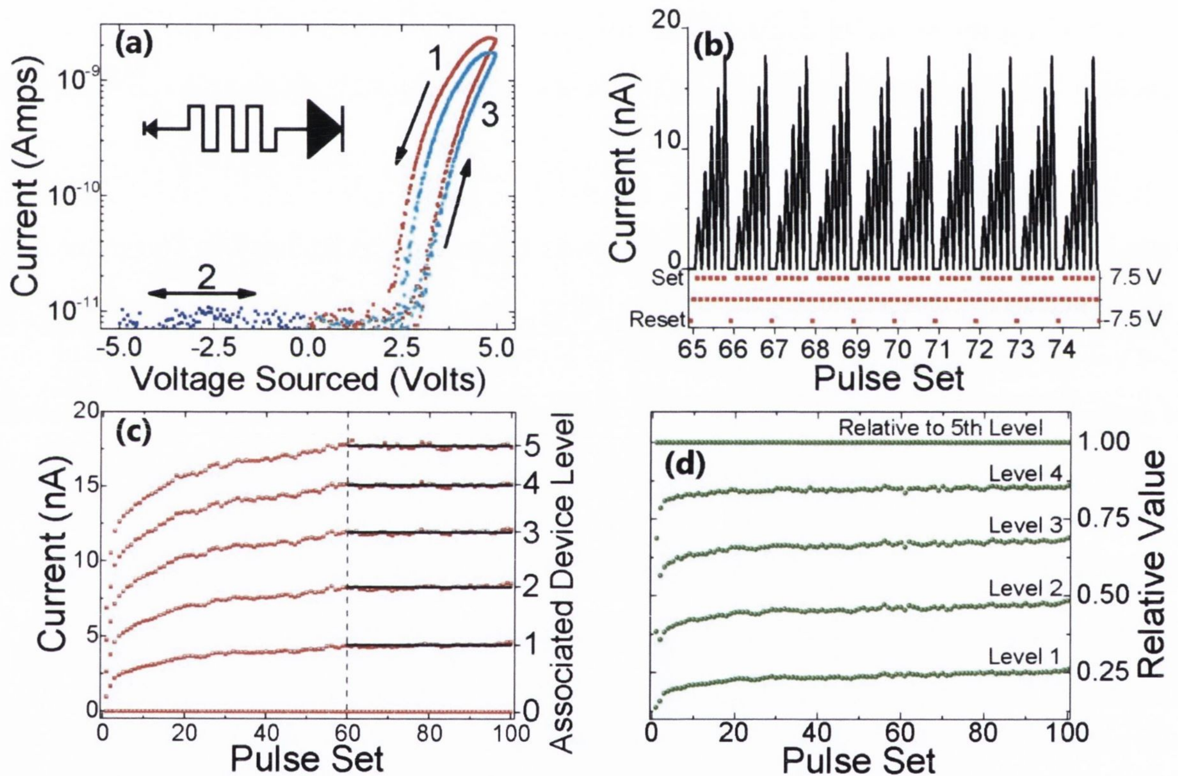


Figure 5.11 The diode-like behavior of the nanowire junction device is revealed in (a). Current rectification occurs at reverse bias, the degree of which is heavily dependent on the history of applied voltage stimulus. The sequence of voltage stimulus is (1) +5 V forward sweep, (2) -5 V reverse sweep, (3) +5 V forward sweep. Initially saturated at sweep 1, sweep 2 partially erases the saturation state. Sweep 3 is in a less conductive state following sweep 2. (b) It is possible to define arbitrary conductance levels in the device via successive pulse applications as shown for a segment involving 5 set voltage pulses (+7.5V). Applying a -7.5V pulse resets the device removing its previous memory: a unique feature of these nanowire junctions. (c) Evolution of the device behavior in (b) during the application of over 100 pulses applied to a nanowire junction. The device conductance levels approach steady state after ~60 pulses and remain within 3% mean value for each memory level. (d) Even during the initial period up to 60 pulse sets of (c), the ratio between the levels remains unchanged relative to the 5th conductance level of each set.

This is underscored in Figure 5.11 (d) which shows the magnitude of the current at each level as a fraction of the highest current level. Despite the initial induction period, the relative magnitudes are essentially constant throughout. Once steady state has been achieved the conductance values associated with each memory level are defined to better than 3%. By changing the pulse combination or by tuning the pulse height and width before the reset pulse, it is possible to change the number of memory levels that span the maximum current level the device can support.

Figure 5.12 shows the case of a four-level memory device. The status of the memory levels is read by the application of a sub-threshold voltage pulse large enough to produce a measurable current, but not capable of modifying the conductance. Threshold behavior is a characteristic memristor property and in our case the optimum read pulses are between +3 V and +6 V [18] as seen in Figure 5.12 (b). The read voltage is the most difficult parameter to optimize. The read voltage in Figure 5.12 (b) is close to the 7.5 Volt set voltage shown in (a). While initially the read voltage does not perturb the device conductance, following the reset it is obvious as the device evolves 6 Volts is sufficient to increase conductance. Relatively high set voltages of 15 V are used in this instance to show pronounced conductivity changes between set steps. Although the results are far from ideal, the data shown in Figure 5.12 (b) proves in principle at least how a functioning device may operate with 4 level memory states.

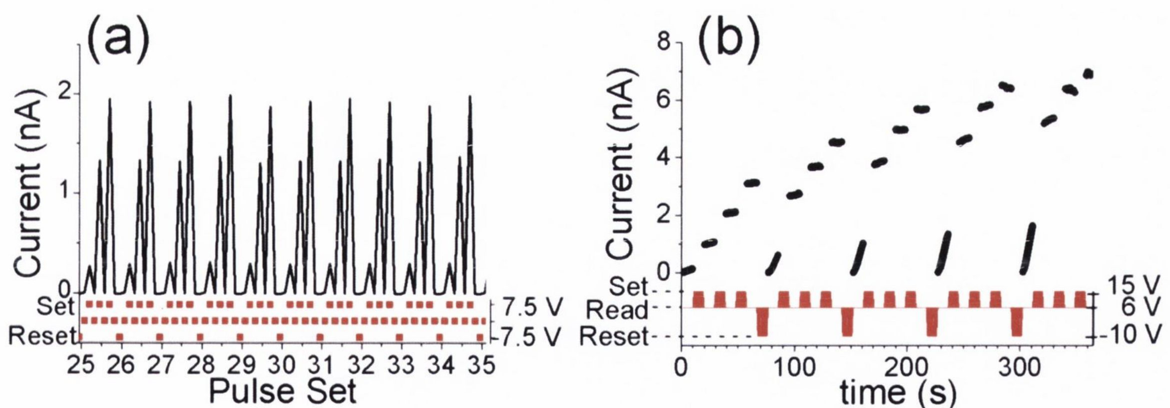


Figure 5.12 A device that displays four level memory in response to a -7.5 V reset pulse followed by three forward 7.5 V set pulses is shown in (a). (b) A 6 V read voltage is used to sample the conductance state of the device between 15 V set pulses and -10 V reset pulses (only read currents shown). 15 V pulses are used to increment the conductance of the device and the -10 V pulses are used to dial back the conductance. These preliminary results are promising but will clearly require further development for multbit coded information storage.

5.4 Memristance Mechanism

The mechanism of resistive switching and memristance in TiO_2-based device is widely debated in the literature.[5] It is possible at this point to hypothesise on the operation of our device in the context of what has been reported. Initially the band alignment across the device structure shown in Figure 5.7 (a) is considered. The Au contact leads have a work function of 5.1 eV and form Schottky barrier contacts with the wide bandgap TiO_2 nanowire. Since the nanowire is single crystal with a high degree of perfection, few carriers are available to screen the Schottky barrier, so that the presence of the latter likely dominates the measured conductance of the virgin wire. This situation is described schematically in Figure 5.13 (a) where band bending reflects the Schottky barrier height and width. Under electroforming conditions described here, oxygen vacancies are known to readily form at the TiO_2 interface with the positively biased Au metal contact.[7, 9, 16, 24, 28] These anodic conditions result in the oxidation of the lattice oxygen $O_O^{\times}$ to form positively charged oxygen vacancies $V_O^{\bullet\bullet}$ by the following reaction:[29]

$$O_O^{\times} \rightleftarrows V_O^{\bullet\bullet} + 2e' + \tfrac{1}{2}O_{2\,(g)} \qquad (5.7)$$

It is well established that oxygen vacancies act as n-type dopants with shallow donor states below the conduction band of bulk TiO_2.[30] This has the effect of shifting the Fermi energy closer to the bottom of the TiO_2 conduction band, as shown in Figure 5.13 (b), thereby increasing the number of free electrons in the band. The oxygen vacancies generated by reaction (5.7) may form a charged double-layer with the negative sheet of charge on the Au electrode established during Schottky barrier formation.[29] This double layer is a capacitor and may be the origin of the capacitive behavior seen in the impedance data in Figure 5.10 (c). The additional carriers created by this reaction will reduce the Schottky barrier height and width and increase the rate of tunneling into the contact. If a sufficiently large population of vacancy dopants are created and extend beyond the interface, an impurity band could form that facilitates conduction by a variable range hopping mechanism.[31]

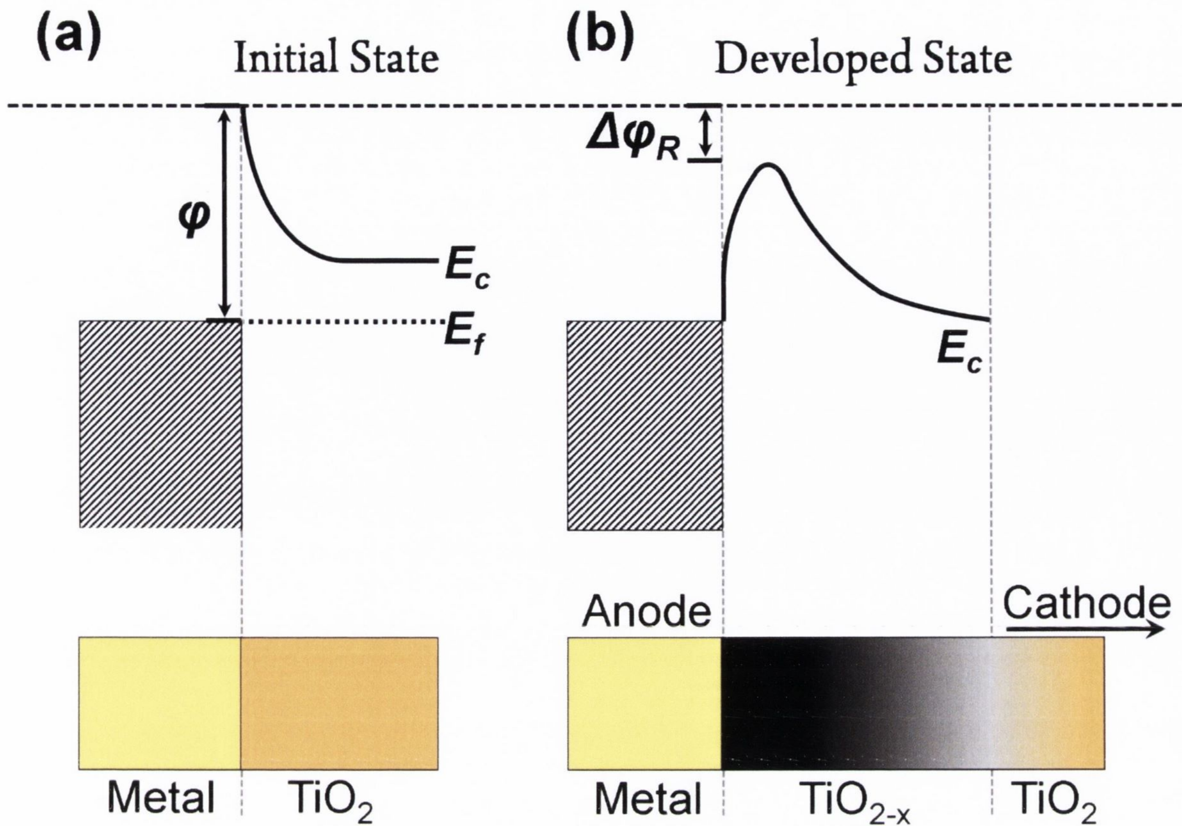


Figure 5.13 (a) Band alignment at the contact region of a virgin device, φ is the Schottky barrier height. (b) The Schottky barrier between the TiO_2 wire and the Au electrode has a reduced height and width following the production of a population of oxygen vacancies which act as n-type dopants promoting electrons to the conduction band, $\Delta\varphi_R$ is the reduction in Schottky barrier height. This ultimately increases charge injection and the conductance of the device. Furthermore, this population of dopants is manipulated during device operation, giving rise to the dynamic device behaviour reported in the text.

An important aspect of the device operation is that positively-charged oxygen vacancies created at the anode are mobile. While mobility is necessary to establish the charge double layer described above, any penetration of an applied electric field through the double layer will naturally cause the oxygen vacancies to drift away towards the cathode. Based on this it may be suggested that the SS condition described in Figure 5.10 (a) reflects a balance between the rate of vacancy generation at the anode and the rate of vacancy drift towards the cathode. Crucially, the application of a short negative (reset) voltage pulse has the effect of injecting electrons from the Au electrode into the wire, annihilating oxygen vacancies in the near contact region via the reverse of reaction (1). This creates a depletion region next to the Au electrode and effectively resets the device, consistent with the data in Figure 5.11. Subsequent set pulses

sequentially restore the oxygen vacancy population. This unique reset ability provides an important handle in controlling the multilevel memory operation.

The liberation of lattice oxygen from planar TiO_2 devices is reported in many cases to degrade Pt and Au metal contact [7, 24]. The fact that has not been observed for our Au contacted nanowire devices may be due to the novel geometry of our nanowire devices which have intimate contact between the TiO_2 wire, the electrode and the atmosphere. In contrast to planar thin film devices in a stacked orientation, the transverse orientation may allow our devices to 'breath' by allowing the oxygen gas to escape the interface without adversely affecting the metal adhesion to the wire. However as shown in Figure 5.9 (d) the use of Ti electrodes reveals visible signs of degradation or bubbling after forming. The bubbling is ascribed to the oxidation and oxygen capture by the Ti electrodes from the TiO_2 wire underneath it. For the purpose of device operation it is therefore necessary to have an inert metal electrode that facilities the formation of oxygen vacancies, prevents ionic exchange reactions and does not become reduced as a result of the oxygen liberation.

Having introduced the physical mechanism, it is worth attempting to produce a constitutive relation that describes the overall device behavior. For a flux (voltage) controlled memristor, i.e. a memristor which has voltage stimulus applied to it while the current output is monitored, the constitutive relation must be a function of voltage (equation (5.4)). Data that describes the device dynamic current characteristics is shown in Figure 5.10. The observation that V_{on} reduces to a single value at steady state suggests the both the energy bands and the depletion layer population are no longer changing at interface. If the population of vacancies at the interface is steady it's possible to assume the corresponding built in potential of the depletion layer has a single value. The equation that describes current transport in a Schottky barrier by thermionic emission can therefore be used, given below as [4]:

$$J = AT^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{5.8}$$

$$A = \frac{4\pi q m^{\star} k^2}{h^3} \tag{5.9}$$

Current density J, is a function of the effective Richardson constant A (A/cm^2-K^2), T temperature, q the charge of an electron, Boltzmann's constant k, voltage V and the Schottky barrier height ϕ_b. For the purpose of simulation equation (5.8) is simplified and expressed it in

terms of current i by dividing J by the Richardson constant. The resulting equation is expressed as:

$$i(t) = T^2 \exp\left(\frac{-\phi_b(\varphi)}{kT}\right)\left[\exp\left(\frac{V(t)}{kT}\right) - 1\right] \tag{5.10}$$

This equation has the form of equation (5.5) with the conductance given by:

$$\frac{d\hat{q}(\varphi)}{d\varphi} = \exp\left(\frac{-\phi_b(\varphi)}{kT}\right) = G(\varphi) \tag{5.11}$$

The $\phi_b(\varphi)$ term captures the dynamic nature of the device conductance as the height of the Schottky barrier fluctuates. It will be a function of voltage history through the device times a generation rate (α) of oxygen vacancies in the device in response to the voltage stimulus. It may be expressed as,

$$\phi_b(\varphi) = \phi_I - \phi_S(\varphi(t)) \tag{5.12}$$

With $\phi_S = \varphi(t) = \alpha \times \int_0^t v(t)\, d\tau$ (5.13)

Where ϕ_I is the initial barrier height for carrier injection from the semiconductor into the metal, ϕ_S describes how this barrier height changes as more vacancies are created at the contact interface. The voltage integral over all time captures the total voltage applied to the device. This flux value will be related to the prevailing number of vacancy defects created in that time under bias. The constitutive relation could be refined by taking into account how the population of vacancy defects alters the barrier height and setting a saturation limit on the total population of defects to reflect the measured current saturation at a given voltage. The constitutive relation may offer some predictive capacity for these nanowire devices. This would be useful in determining the optimum voltage pulse sequence for a device to realise various multilevel memory states.

5.5 Conclusions and Future work

Pseudo-unipolar memristors are fabricated by contacting single TiO_2 nanowires. Wire resistance can be reduced to ~ 10^{-8} ohms from pristine values of ~10^{-11} through electroforming or exhaustive voltage sweeps. Current levels behave dynamically in response to voltage sweeps, evolving and increasing current levels when the same voltage pulse is applied. Current and hysteresis levels both decrease as the speed of the voltage sweep increases. The presence of a saturated device state provides a reference in what would otherwise be a continually changing device. A model that fits the observed device characteristics is introduced, based on engineering a population of mobile ionic dopants, oxygen vacancies in the wire introduced through voltage stimulus.

The population of vacancies can drift within the wire under applied bias offering a degree of control over their position in the wire. Acting as n-type dopants, the vacancies decrease wire resistance by increasing the conduction band electron population, enhancing band bending at the metal interface, and reducing the Schottky-barrier height. These factors all increase thermionic emission into the metal. Typical device characteristics are described in terms of vacancy position at the metal interface. Reproducible multilevel resistance states can be coded in the device with programed voltage pulses, demonstrating single nw devices as viable memory elements for applications in novel nonvolatile memory cells. These device also serve as a relatively simple platform for investigating memristance phenomena.

The single nw device reported here has parallels with conventional planar Au/TiO_2/Au memristors, except that by comparison the thickness of the TiO_2 layer in this device is very large, which effectively separates the behavior of the device into the two electrode regions which can be treated independently. In contrast, a conventional planar memristor typically has an oxide layer that ranges in thickness from 20-50 nm, and both electrodes are involved in the creation and/or subsequent reaction of mobile charge dopants responsible for device operation. Issues such as dopant discharge at the counter electrode are common.[18] An obvious attraction of the device geometry in Figure 5.7 (a) is the possibility of gating. Whilst this is not important in the present case—the channel length is 2 μm and the overall conductance of the device is controlled by the behavior at the contacts—gating should become increasingly effective as the channel length is reduced, allowing modulation of the tails in the barriers that extend into the channel from the electrode regions on either side.

Much of the future work will focus on developing new device layouts that would be more conducive to circuit integration and improved device simulation. As a simple two terminal device spanning microns in distance, its electronic properties are very interesting. Two immediate aspects of the device can be changed to facilitate integration: shortening the pitch and increasing the number of metal contacts on the wire. Shortening the pitch would naturally increase the current levels within the device while increasing the number of individual metal contacts on the wire would allow for many intrawire devices.

5.6 References

1. *International Technology Roadmap for Semiconductors 2013 Edition*. Available from: http://www.itrs.net/Links/2013ITRS/Summary2013.htm.
2. Jeong, D.S., et al., *Emerging memories: resistive switching mechanisms and current status.* Rep. Prog. Phys., 2012. **75**(7): p. 076502.
3. Ovshinsky, S.R., *Reversible Electrical Switching Phenomena in Disordered Structures.* Physical Review Letters, 1968. **21**(20): p. 1450-1453.
4. Sze, S.M. and K.K. Ng, *Physics of Semiconductor Devices*. 2006: Wiley.
5. Waser, R., et al., *Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges.* Adv. Mater. , 2009. **21**(25-26): p. 2632-2663.
6. Du, Y., et al., *Symmetrical Negative Differential Resistance Behavior of a Resistive Switching Device.* ACS Nano, 2012. **6**(3): p. 2517-2523.
7. Kwon, D.H., et al., *Atomic structure of conducting nanofilaments in TiO2 resistive switching memory.* Nat Nanotechnol, 2010. **5**(2): p. 148-153.
8. Yang, J.J., et al., *Memristive switching mechanism for metal/oxide/metal nanodevices.* Nat Nanotechnol, 2008. **3**(7): p. 429-33.
9. Kazuki, N., et al., *Switching Properties of Titanium Dioxide Nanowire Memristor.* Jpn. J. Appl. Phys., 2012. **51**(11S): p. 11PE09.
10. Sawa, A., *Resistive switching in transition metal oxides.* Mater. Today, 2008. **11**(6): p. 28-36.
11. Rainer Waser, M.A., *Nanoionics-based resistive switching memories.* Natuure Materials, 2007. **6**.
12. Dearnaley, G., A.M. Stoneham, and D.V. Morgan, *Electrical phenomena in amorphous oxide films.* Reports on Progress in Physics, 1970. **33**(3): p. 1129.
13. Dayan, P. and L.F. Abbott, *Theoretical Neuroscience: Computational And Mathematical Modeling of Neural Systems*. 2005: Massachusetts Institute of Technology Press.
14. Strachan, J.P., et al., *Direct identification of the conducting channels in a functioning memristive device.* Adv Mater, 2010. **22**(32): p. 3573-7.
15. Strukov, D.B., et al., *The missing memristor found.* Nature, 2008. **453**(7191): p. 80-83.
16. Jeong, D.S., et al., *Characteristic electroforming behavior in Pt/TiO2/Pt resistive switching cells depending on atmosphere.* J. Appl. Phys., 2008. **104**(12): p. 123716.
17. Vance, A., *With 'The Machine,' HP May Have Invented a New Kind of Computer*, in *Bloomberg Businessweek*. 2014.
18. Yang, J.J., D.B. Strukov, and D.R. Stewart, *Memristive devices for computing.* Nat. Nanotechnol., 2013. **8**(1): p. 13-24.
19. Pershin, Y.V. and M. Di Ventra, *Memory effects in complex materials and nanoscale systems.* Adv. Phys., 2011. **60**(2): p. 145-227.
20. Chua, L.O., *Memristor-The missing circuit element.* Circuit Theory, IEEE Transactions on, 1971. **18**(5): p. 507-519.
21. Chua, L., *Resistance switching memories are memristors.* Appl. Phys. A 2011. **102**(4): p. 765-783.
22. Grant, I.S. and W.R. Phillips, *Electromagnetism*. 2013: Wiley.
23. Keithley, *Performing Very Low Frequency Capactiacne-Voltage Measurements on High Impedance Devices Using the Model 4200-SCS Semiconductor Characterization System.* Application Note Series 2013(3140).
24. Joshua Yang, J., et al., *The mechanism of electroforming of metal oxide memristive switches.* Nanotechnology, 2009. **20**(21): p. 215201.
25. Choi, S.J., et al., *In situ observation of voltage-induced multilevel resistive switching in solid electrolyte memory.* Adv. Mater., 2011. **23**(29): p. 3272-3277.

26. Iulia, S., et al., *Origin of the OFF state variability in ReRAM cells.* Journal of Physics D: Applied Physics, 2014. **47**(14): p. 145102.
27. Hu, C., et al., *Highly Controllable and Stable Quantized Conductance and Resistive Switching Mechanism in Single-Crystal TiO2 Resistive Memory on Silicon.* Nano Lett., 2014.
28. Diebold, U., *The surface science of titanium dioxide.* Surf. Sci. Rep., 2003. **48**(5–8): p. 53-229.
29. Jeong, D.S., H. Schroeder, and R. Waser, *Mechanism for bipolar switching in a TiO2 resistive switching cell.* Phys. Rev. B, 2009. **79**(19): p. 195317.
30. Janotti, A., et al., *Hybrid functional studies of the oxygen vacancy in TiO2.* Phys. Rev. B, 2010. **81**(8).
31. Fogler, M.M., S. Teber, and B.I. Shklovskii, *Variable-range hopping in quasi-one-dimensional electron crystals.* Phys. Rev. B, 2004. **69**(3): p. 035413.

Chapter 6

Neural Learning and Memory Behaviour at a Single Nanojunction in Response to Heterogeneous Stimuli

6.1 Introduction

The human brain's ability to process multiple complex stimuli into useful information is unrivalled. Despite its modest size of 1200 cm^3 it can perform upwards of 10^{16} operations per second. More importantly, the brain's power requirement to execute these operations is around 20 W. Although modern technology incorporated into supercomputers is approaching similar levels of performance they are physically massive ~ 1500 m^3 and require up to 3 MW of power to reach comparable brain function [1]. Table 6.1 outlines some of the main differences between silicon based devices and biological systems. In terms of speed, accuracy and reproducibility integrated circuits perform better than any biological system. But the advantages of biological systems stem from their adaptability, interconnectivity, parallelism and self-healing nature. These attributes, coupled with the emergent self-awareness biological systems display make them prolific computation systems.

The brain is an organ that is part of a larger system (the body) that supports and enable its function (the mind). Beyond the organs providing nourishment to the brain in the form of oxygen and blood, there is a series of sensory organs that make the brain aware of its surroundings. These sensory organs respond to external stimuli such as light, smell, sound, taste and touch which make up the traditional senses. The more complex senses that make up the vestibular system are the senses of balance, movement and spatial orientation. The central

nervous system is optimised to convert all sensory stimuli into an electrical signal which is transmitted to the brain for interpretation.

There has been much work on developing digital semiconductor devices that perform the same function as the various sensory organs [2]. The retina [3, 4], the cochlea [5], the nose [6, 7] and touch [8, 9] have been partially reproduced with semiconductor based hardware to emulate each sense. From a device point of view the sensory organs may be classified as analog circuits which by definition have a continuous variable signal. The sensory organs operate as devices that detect a stimulus and transmit it to the brain for interpretation. This specific operation can be reproduced with greater accuracy and sensitivity using digital circuits for each sensory organ. However there remains one specific function digital circuits cannot easily reproduce to the same degree as the brain, and that is cognition and interpretation.

Table 6.1 A comparison between the inherent attributes biological systems and silicon based devices display.

Biological Systems	Silicon Based Devices
Emergent Properties	Speed/Precision
Self-healing	Reproducible
Adaptable	Programmable
Analog & Digital Platform	Digital Platform
Massive Interconnectivity	Integratable

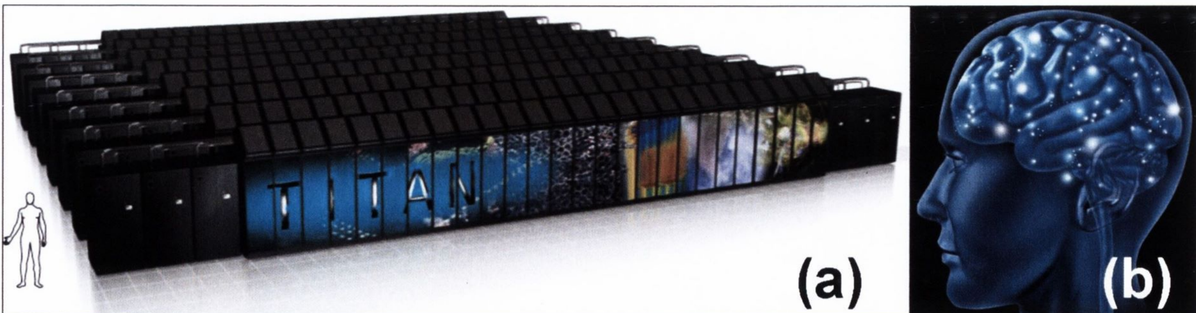


Figure 6.1 Giant supercomputers are required to match the operation of a human brain. (a) The Titan supercomputer pictured with a human for scale occupies 400m^2 and consumes 8.2 MW [10]. (b) The human brain has many superior characteristics relative to a supercomputer, not least the power efficiency per operation [11].

The specific cells in the brain responsible for memory, learning, cognition and interpretation are called neurons. There are up to 100 billion neurons in the brain and together they form a vast interconnected neural network with 100 trillion connections called synapses [12]. An individual neuron cell is shown in Figure 6.2. The activation, 'spiking' or 'firing' of a neuron requires firstly an incoming stimulus with a large enough amplitude to elicit a response from the neuron. The neuron operates on an all-or-nothing principle meaning sub threshold stimuli will not fire the neuron. Once fired however, the neuron will propagate the electrical signal along its length. A more intense stimulus only increases the frequency of neuron firing.

Synaptic connections between individual neurons may be electrically or chemically triggered. For the latter case a strong stimulus will cause a large amount of chemical signals (neurotransmitters) to be released quickly from the synapse. Once a sufficient amount of neurotransmitters are collected by the receptors of the adjacent synapse, the condition is met for producing axon transmission or stimulus propagation. The propagated stimulus will reach synapses at the end of the 'fired' neuron and, provided the electrical signal (action potential) is great enough, repeat the process in the next adjacent neuron. A 'fired' neuron elicits a secondary response which reinforces the strength of the neuron. This ultimately lowers the 'firing' threshold of the neuron and increases the amplitude of the action potential it produces. This process constitutes learning.

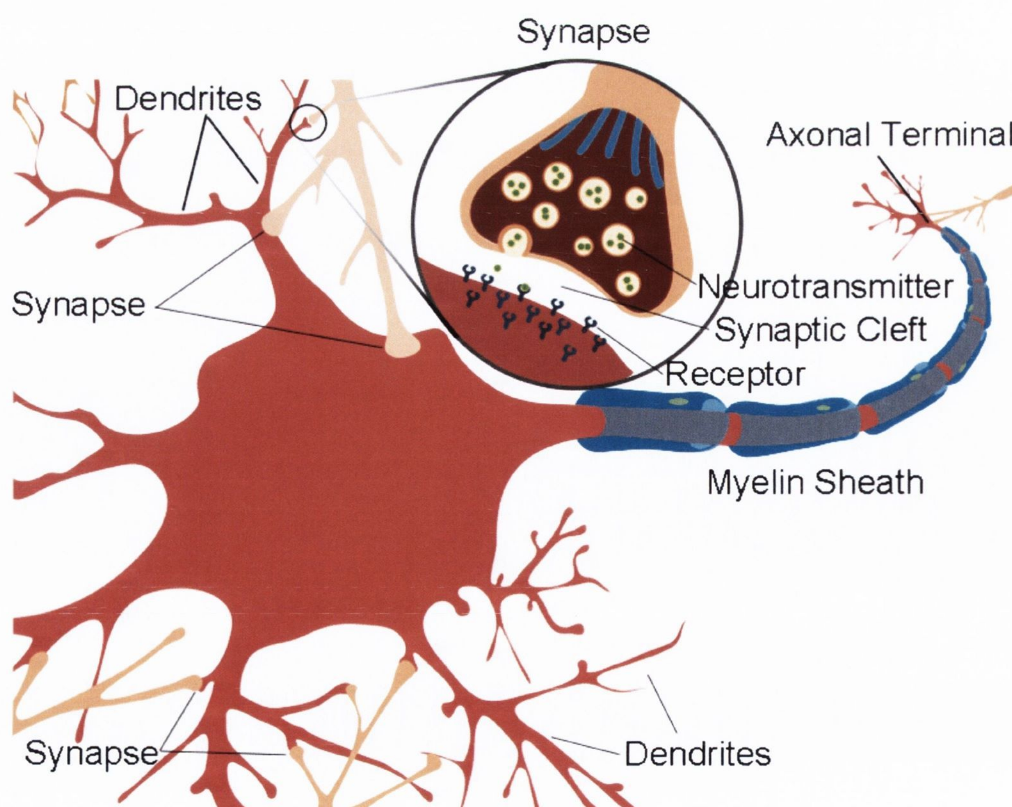


Figure 6.2 A schematic of the components constituting a single neuron [13].

Thus how a neuron operates in response to a stimulus has been described briefly. As an analogue circuit roughly 20um^2 in size, it operates as a non volatile memory cell with read/write cycles of μs and erase cycles of hours. When considered individually, the function of a neuron can be reproduced and executed faster with digital circuits such as SRAM and DRAM described in the previous chapter. However as alluded to before, the massive parallelism and connectivity are the greatest strengths of the brain's neural network. This gives rise to specific emergent properties unique to a neural network that enable it to outperform standard memory circuits.

Associative memory is the ability to learn, remember and recognise the relationship between unrelated heterogeneous stimuli. It is the ability to correlate one stimulus and response with another separate stimulus to produce the same response of the initial stimulus applying only the second stimulus. An example of associative memory is the gradual association of a sound of a bell with the sight of food to produce salivation in a dog [14]. Exposing the dog to these two stimuli simultaneously produces salivation as an action or output. Over time the sound of

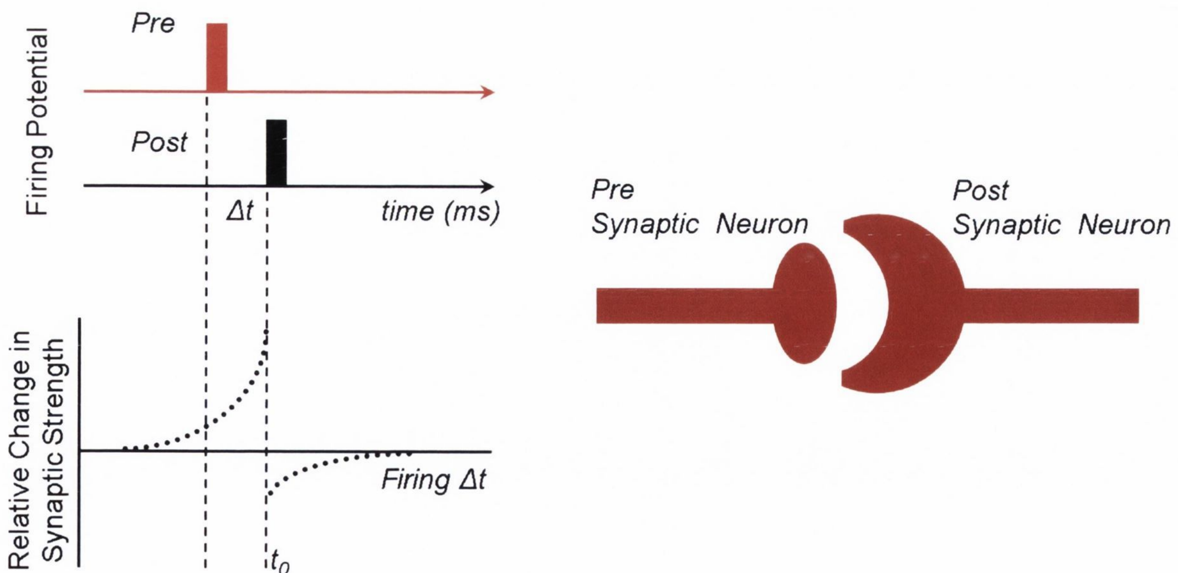


Figure 6.3 An illustration of Hebbian STDP. There is a small time window (0-20 ms) in which the presynaptic neuron must fire relative to the postsynaptic neuron (t_0) in order to cause LTP or strengthening of the synapse between the two.

a bell alone can produce the same output without the sight of food. This is a fundamental operation the brain executes everyday allowing us to function and thrive in our environment. The physical principle is based on the concept of Hebbian learning and spike timing dependent plasticity (STDP) both illustrated in Figure 6.3.

Hebbian learning is the observation that when one cell (i) contributes to the firing of the adjacent cell (ii) the strength of the synapse from (i) to (ii) is increased. The concept was first introduced in 1949 and laid the foundation on which modern STDP is based [15]. There is clear correlation between the strength of a neural synapse and the relative timing of pre and post synaptic spikes [16]. Changing the synaptic plasticity, the ability of synapses to strengthen or weaken over time, requires synchronous spikes to produce long term potentiation (LTP), or depression (LTD). For LTP to be realised a presynaptic spike must precede post synaptic spikes within a timing window of 0-20 ms. For the purposes of timing the post synaptic spike is considered t_0. Should the two spikes fire relative to each other within this timeframe the strength of the synaptic connection between them increases. Correspondingly the synaptic strength between the neurons can be decreased when the post synaptic spike precedes the presynaptic spike by 0-100 ms. Together the LTP and LTD processes are proposed as the biological foundation of memory and learning.

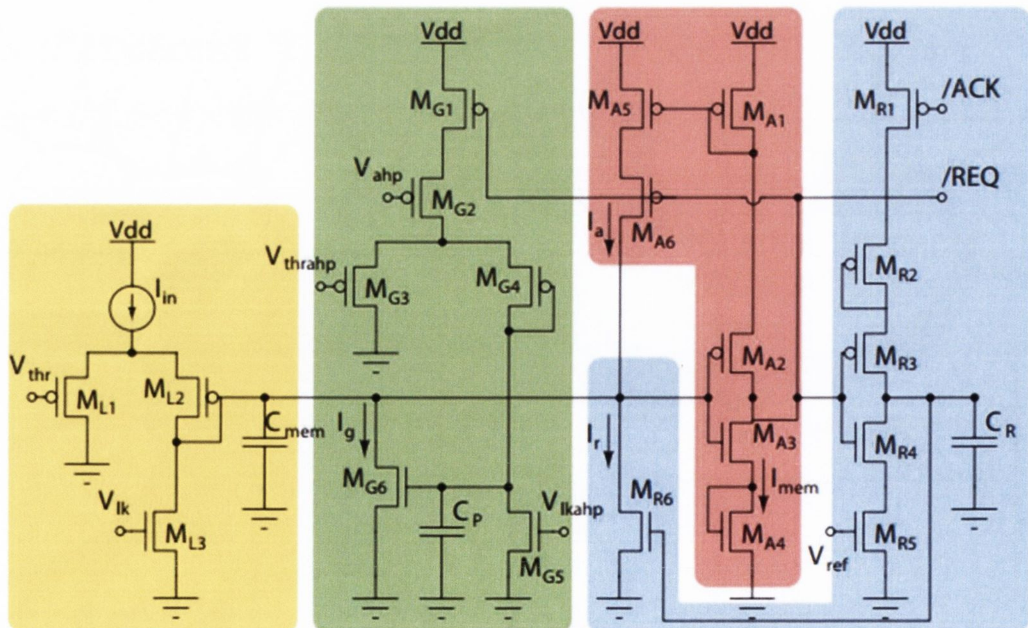


Figure 6.4. A schematic diagram of a digital based integrated circuit designed to emulate the function of single neuron [17]. Each coloured section has an individual function which combine to produce a neuron like behaviour.

These physical processes are difficult to emulate with standard digital circuitry and require many integrated components. An example of a digital circuit specifically designed to perform the same functions of a *single* neuron is shown schematically in Figure 6.4 [17]. Stringing these components together to form a neural-like system will be larger and ultimately require more power in comparison to the brain's neural network. Although digital components have undergone tremendous scaling in size over the last 40 years the issue is not purely about size but about maintaining the low power and parallelism of neural networks.

There have been many efforts to emulate the computation power of a brain using established digital circuitry. To date the main research efforts have used various combinations of digital circuits that when combined together will operate in a similar manner to that of a human brain [18]. Recent efforts have successfully mimicked the cognitive ability of half a cat brain employing a 1.4 MW supercomputer modelling simplified point neurons 700 times slower than real time [19]. The two key issues in realising a semiconductor based brain are implementing a programming code using individual digital circuits to produce learning, so-called neuromorphic or adaptive programming. The second is a lack of semiconductor components or so called 'neuromorphic hardware' that behave sufficiently like that of the base elements of the brain. Together they represent the grand challenges of realising human level intelligence with computers. Adaptive programming has become more sophisticated over the years with some notable advances,[20] producing brain-like function through a combination of semiconductor elements. However the combination of each individual element produces not only a larger size than that of the biological element it mimics, the neuron, but it also requires much greater levels of power. There is therefore a need to produce a circuit element that accurately mimics neuron operation while maintain low power consumption. One such device, the memristor, is capable of producing these effects.

In 1971 Leon Chua predicted the existence of a circuit element with intrinsic history dependence – the fourth element in addition to the resistor, capacitor and inductor [21]. This element, known as the memristor, should display evolutionary, dynamic device behaviour and rudimentary learning capabilities. More importantly, it can be shown mathematically that this element cannot be made up of any linear combination of the other fundamental circuit elements. Experimentally, the memristor was not realised until 2008 when William et al reported the first two terminal memristor [22]. Since then many examples of memristors have been observed [23]. Crucially, they represent a novel semiconductor technology and neuromorphic hardware platform that can in principle be used to emulate neuron function with low power and high speed. In the previous chapter, memristors were introduced as simple multi-level memory

elements from a non-volatile memory perspective. In this chapter, the focus will be on the neuromorphic computing power a memristive like component may enable.

In this chapter a novel phenomenon will be introduced that has yet to be realised in other materials or systems, even biologically. By coupling individual and distinct stimuli associative memory has been successfully demonstrating in TiO_2 nanowire devices. This novel behaviour is demonstrated and its importance discussed. As mentioned before, the sensory organs transform stimuli into electrical signals the brain can interpret to display associative memory. Non-biological systems display this behaviour for homogenous voltage or optical stimuli to produce associative memory. In this chapter, heterogeneous stimuli coupling to produce an associative memory effect will be presented for the first time. The significance of this coupling lies in the ability of a single synapse to process and translate different physical stimuli, which is not possible even in biological systems where specific sensory neurons process signals from the different senses. When fully realised, heterogeneous stimulus coupling devices will enable the replication of neural cognition at small scale and low power consumption.

6.2 Experimental

TiO_2 nanowire devices were fabricated as described previously using UV lithography, spray deposition and e-beam lithography. For blanket nonspecific UV exposures, a 100 W Mercury arc UV lamp with 350-500 nm filter option was used to form the device before being placed back into the probe station for further electrical measurements. The optical set up used for UV stimulus in real time is pictured in Figure 6.5 it details all of the individual components that comprise the optical and voltage stimulus test equipment. The Keithley 4200-SCS parameter analyser is used to source voltage and measure current in real time while the optical set up is used to modulate the incident laser light onto the single nanowire and to measure the electrical response in real time. The laser used was a collimated laser diode module (Thor Labs), 405 nm wavelength, 4.5 mW output power, elliptical beam spot shape. The laser was focused to 470-490 nm FWHM spot size using a Mitutoyo 50x microscope objective. A physical shutter was used to ensure coincident voltage and optical stimulus was applied to the wire device with a resolution of 0.5 seconds rise/fall time.

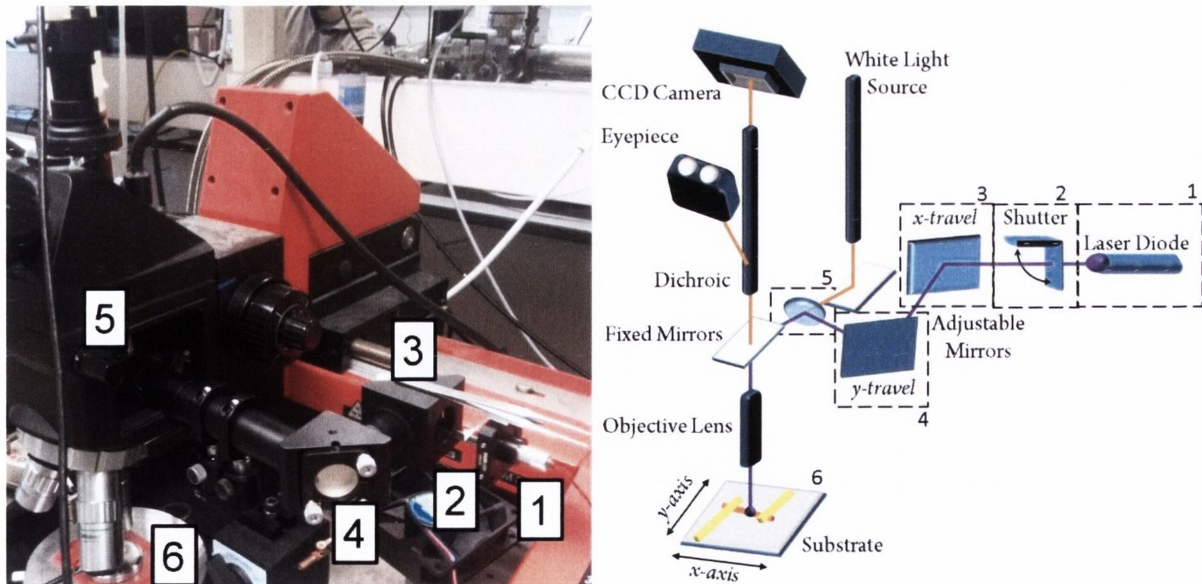


Figure 6.5 Electrical probe station with laser mounted setup for dynamic UV laser experiments. Each component is numbered to correspond to the schematic diagram on the right.

6.3 Results and Discussion

6.3.1 Interaction of TiO_2 with Static UV Light for Assisted Forming

Light impinging on a semiconductor is absorbed mainly through interband electronic transitions and some free electron contributions [24]. The efficiency of light absorption is determined by the crystal structure of the semiconductor material, namely if the crystallographic symmetry allows direct or indirect transitions across the band gap. Direct bandgap materials are more efficient in terms of light absorption. Indirect bandgap materials require additional momentum or energy from a phonon to absorb photons, which is therefore less efficient. There is growing confidence in the literature that TiO_2 Anatase and Rutile phases are both indirect bandgap materials [25-27]. The interaction of TiO_2 with light is well documented and studied owing to its popularity as a solar cell electrode material. Its primary role in solar cells is to increase cell efficiency by preventing photogenerated electron-hole pair recombination [28].

TiO_2 is considered a wide band gap semiconductor with a band gap energy of 3.0 eV (Rutile) or 3.2 eV (Anatase). These energies correspond to 413 nm and 387 nm wavelength of light respectively and are in the UV range of the electromagnetic spectrum. At these wavelengths, the opacity from the atmosphere approaches 100%, so TiO_2 is used in conjunction with dyes that are sensitive to visible light to harvest energy, as visible light transmits better through the atmosphere [29].

More generally, light impinging on a semiconductor with energy that is above the band gap will form electron hole pairs which are known as excitons. The electron hole pair may be weakly bound (essentially free) to each other by electrostatic interaction or strongly bound together. They can move about the material for a finite time before recombination. In solar cells, electrons in the conduction band of the electrode material (e.g. TiO_2) must be injected into the circuit at a faster rate than the recombination rate in order to sustain a photocurrent. Beyond generating current, the separation of electron hole pairs can induce chemical changes in the material. The free electrons or holes may interact with a lattice atom to take place in a chemical reaction. One such reaction is described below for TiO_2 [30-32]:

$$TiO_2 + hv \rightarrow e' + h^{\bullet} \tag{6.1}$$

$$h^{\bullet} + \frac{1}{2}O_O^{2-} \leftrightarrow \frac{1}{4}O_{2\,(g)} + V_O^{\bullet\bullet} \qquad (6.2)$$

Equation (6.1) describes the photogeneration of electron hole pairs in TiO_2 through the interaction with photons of energy *hv*. Equation (6.2) describes the subsequent interaction of the photo-generated holes with lattice oxygen to produce oxygen gas and oxygen vacancies at the TiO_2 surface. In Chapter 5 the role of oxygen vacancies in TiO_2 was discussed. To reiterate, oxygen vacancies present in TiO_2 can be considered n-type dopants that introduce shallow trap states into the forbidden energy gap of TiO_2. Overall they increase conduction within TiO_2. Reactions (6.1) and (6.2) together prescribe an alternate route for introducing oxygen vacancies into TiO_2. This route does not require a voltage bias at either electrode. This is in contrast to how vacancies were introduced in Chapter 5 where the description of how the conductivity of TiO_2 is heavily dependent on the amount of oxygen vacancies and their distribution in the material. To demonstrate the ability to dope TiO_2 with optically generated oxygen vacancies single TiO_2 nanowire devices were fabricated with gold contacts in a similar fashion to that described in the previous chapter.

An initial -10 Volt sweep is used to check the status of the single wire device before exposing the *whole chip* to UV light for 15 minutes using the 100 W UV source with a calculated intensity at the sample of $4*10^4$ J/m^2. The exposure took place outside of the electrical testing set up and the current was not monitored in real time. The device is tested again using the same -10 Volt sweep as before. The results are shown in Figure 6.6 (a) The initial current response is traced out in black with the post UV exposed current traced out in red. The device remains off initially with no measurable change in current from the base noise level of the set up. After UV exposure for 15 mins the device displays a dramatic increase in conductivity in response to a voltage sweep. The increase is roughly four orders of magnitude from base detection level $\sim 10^{-12}$ to $\sim 10^{-8}$ Amps. Overall the time required to fully form the nanowire device has been reduced to 15 minutes, which is significantly less time than the hours required to fully form the device with voltage alone.

Thus UV light as a facile route to form and develop the nanowire device to 10's of nA conductance has been demonstrated. The blanket exposure of the ~ 1 cm^2 chip under UV not only exposes the entire wire device but also every other wire on the chip. This contrasts with purely voltage forming whereby only the anode interface is saturated with oxygen vacancies. Therefore it is reasonable to assume this homogeneous distribution of oxygen vacancies along

the length of the wire. The completely doped wire gives rise to the four fold increase in conduction compared to a two-three fold increase in conduction following a voltage bias step. Building on these UV device forming experiments, a UV diode laser set up mounted on the electronic probe station (as shown in Figure 6.5) was prepared for real time dynamical measurements of the UV interaction with our nanowire devices. The laser power reaching the nanowire device was measured at ~ 10 μW, which is quite low relative to the previous UV light source. Increasing the laser power delivered to the wire would introduce significant heating in the sample as the spot size is focused down onto the wire. The set up afforded the ability to use both UV and voltage stimuli on an individual device and to monitor its current response in real time. In the first instance both stimuli are used to test how quickly the saturated state can be obtained (note this device was already formed previously). To remove device history a voltage V_{His} = -10 Volt is held across the device for 60 seconds prior to application of $V_{initial}$ = +10 Volt. The initial trace is plotted out in black on Figure 6.6 (b). $V_{initial}$ is held until the device reaches steady state saturation current ~ 16 nA for this particular device. After this V_{His} is applied again before the application of simultaneous 10 Volt and UV laser stimulus ($V + L$). The resulting current trace plotted in red approaches saturation current faster (~125 s) than that of only voltage stimulus alone. Finally V_{His} was applied once more before the last V_{Post} = +10 voltage only stimulus was applied. Interestingly the current trace shown in green approaches device saturation quicker (50 s) than $V_{initial}$ (t_{sat} = 375 s, $V_{initial}$) revealing a persistent memory effect (t_{sat} = 250 s - V+L, t_{sat} = 325 s - V_{Post}).

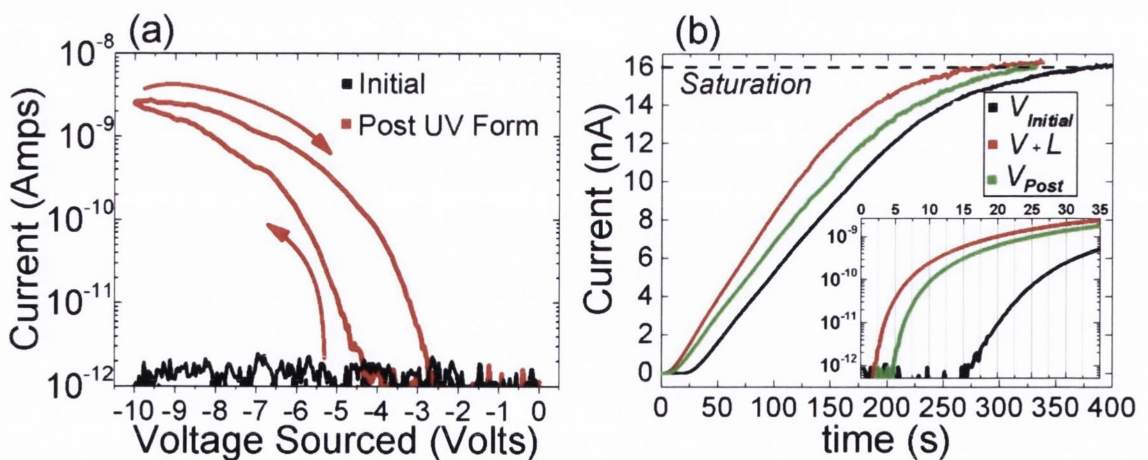


Figure 6.6 (a) An initial -10 Volt sweep is applied to a virgin nanowire device producing no change in current. Device conductance increases four fold after the chip the device is illuminated under a UV lamp for 15 minutes. (b) Appling both voltage and UV stimulus helps develop device saturation quicker than voltage stimulus alone. Inset: Log current scale to show clearly the difference in onset for each stimulus sequence.

This sequence of experiments reveals that combining both optical and voltage stimuli produces faster saturation sequences. Physically this is the result of combining two oxygen vacancy forming mechanisms to saturate the interface of the device with oxygen vacancies. A more subtle result involving the sequence of experiments shown in Figure 6.6 (b) is the retention or ability of the final V_{Post} bias to approach saturation more quickly bias after UV exposure. This suggests a long term memory effect has resulted from combining the two forming stimuli despite the application of V_{His} between the pulses in between. The nset of Figure 6.6 (b) shows the time of the onset current for each experiment in this sequence. $V_{initial}$ current onset begins after 15 s, while $V + L$ and V_{Post} onset occurs at 2.5 and 5 s respectively.

6.3.2 Dynamic Interaction of Optical Stimulus with Voltage Stimulus

In this section the dynamic effects of pulsing UV light while holding a voltage bias across the nanowire device are investigated. Typically for memory type devices it is necessary to move between memory states quickly. For SRAM and Flash memory devices this is achieved by applying rapid voltage pulses of the necessary polarity to change the memory state of the device. These pulses are typically ns – us range for RAM memory devices. The nanowire devices in this and the previous chapter typically respond to voltage pulses on the order of ms for a saturated device but require longer pulse widths (> 1 sec) to move between conductance levels. This time delay is a function of the size and hence the RC time constant of the device, but may also include contributions from the formation and diffusion kinetics of the oxygen vacancies at the anode under voltage bias. Therefore when moving between conductance states these reaction rates will ultimately become rate limiting.

As shown in Figure 6.6 the critical rate processes that control the speed of the device are improved through a UV pulse stimulus. The rapid response of the nanowire devices to UV stimulus is shown in Figure 6.7 (a). In this figure a +10 Volt bias is applied to the wire throughout the experiment. Once the device is saturated, UV laser pulses are then applied. The light pulse sequence is chosen to reveal a Morse code signal of TiO_2 so as to rule out random noise. As the figure shows, the current in the device jumps ~ 1 nA under light stimulus which accurately reproduces the word "TiO_2" in Morse code (–,••,–––,••–––) in the current trace of Figure 6.7 (a).

In this setup, the TiO_2 wire is already saturated with oxygen vacancies through voltage stimulus in contrast to the previous forming section. The UV light stimulus in this instance is merely

generating an additional photocurrent within the material is due to an increase in the number of carriers in the conduction band. Band to band transitions are considered intrinsic transitions. Extrinsic transitions occur when transitions from forbidden-gap energy levels (trap/defect states) generate carriers. Assuming intrinsic only transitions some useful parameters can be extracted from the pulse sequence, such as the external quantum efficiency:

$$\eta = \frac{I_{ph}}{q}\left(\frac{hv}{P_o}\right) \tag{6.3}$$

Where

$$\frac{hv}{P_o} = \Phi \tag{6.4}$$

I_{ph} is the additional photocurrent generated under illumination, q is the elementary charge of an electron and P_o is the power absorbed by the wire. Φ is the photon flux. The responsivity is another parameter of merit and is given by:

$$\mathcal{R} = \frac{I_{ph}}{P_o} = \frac{\eta q}{hv} \tag{6.5}$$

Using the values of I_{ph} = 1 nA, hv (405 λ) = 4.9^{-19} J, $P_o = 10^{-6}$ W obtained for a single TiO_2 nanowire;

$\eta = 3*10^{-4}$ carriers produced per incident photon

$\mathcal{R} = 1.00*10^{-4}$ Amps/W

$\Phi = 2*10^{+13}$ photons/second

To gain some appreciation of these numbers it is necessary to compare them to similar TiO_2 devices. The closest published device consists of a film of TiO_2 nanorods (in contrast to our single wire) contacted with Au and FTO electrodes has a reported responsivity of 134.8 Amps/W at 350 nm light [33]. Using values quoted in the report, an external quantum efficiency of 10.2 can be derived and a photon flux of $1.52*10^{14}$ photons/second. Morphological and size differences between the two devices make direct comparison difficult.

These differences may explain the large discrepancy in efficiency and responsivity between the two. Primarily, the spot size of the diode laser is 800,000 nm^2, meaning focus and positioning are extremely important. This is compounded by the small size of the wire (50-100 nm in diameter) meaning all the power in the spot is not reaching the wire, in contrast with the film of nanorods quoted above. The current in our devices is also ~ 1 nA photocurrent due to its large size 2 μm electrode separation (cf. 0.5 mA I_{ph} [33]). Optimisation of the set up and devices will continue as part of future work as spot size and position can be addressed easily.

In a subsequent experiment, the device was brought to saturation at 10 Volts and stepped down the applied voltage in one volt increments while dynamically pulsing light for 10 s during each step. The results are shown in Figure 6.7 (b) with each laser pulse marked in purple with the voltage level outlined in red and the measured current given in black. As expected an apparent instantaneous jump in current was detected for each UV stimulus. After the light stimulus is removed the current levels within the device remain at higher levels than before the voltage pulse was applied, as seen inset of Figure 6.7 (b).

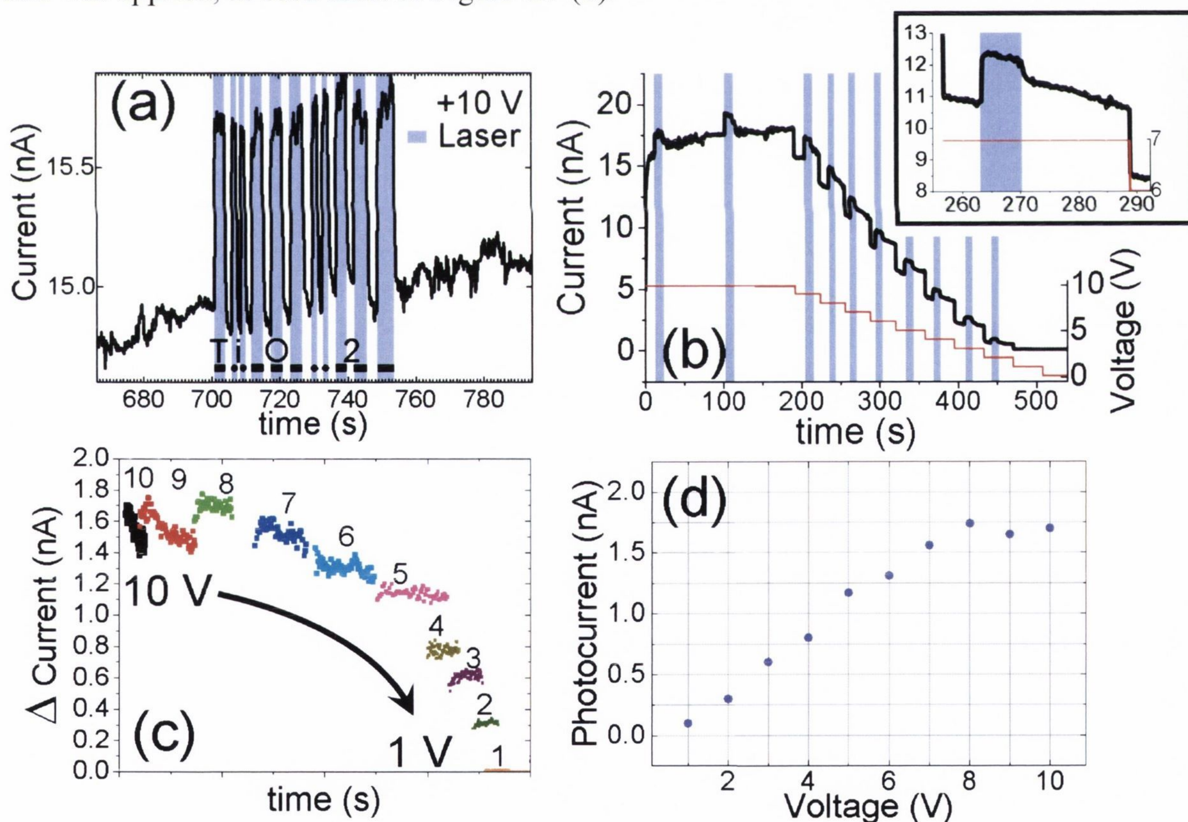


Figure 6.7 Non steady state device characteristics with UV stimulus. (a) While appling 10 volt bias, UV stimulus is pulsed onto the device in a pattern to reproduce the word "TiO_2" in Morse code (-,••,---,••---). (b) 10 volts is applied to the device for 190 s before the voltage is decreased in 1 volt increments to 0. UV stimulus is applied to the device at each voltage value during the course of this voltage pattern. (c) The extra current gained at each voltage (photocurrent) decreases in magnitude from 8 to 0 volts. (d) Photocurrent increases linearly with a slope of 0.25 nA/V to 8 volts where the photocurrent flattens out.

This trend continues across the whole voltage range. Subtracting the voltage-only current at each voltage step reveals the change in current or photocurrent the light stimulus elicits at each voltage and is shown in Figure 6.7 (c). Each voltage step is offset for clarity but there is an obvious trend of decreasing photocurrent after the 8 volt step. The additional photocurrent produced at each voltage is better visualised in Figure 6.7 (d). There appears to be a linear increase with a slope of ~ 0.25 nA/V in photogenerated current up to 8 volts. The photocurrent response then exhibits a plateau region after 8 V where the current no longer increases. The increase in photocurrent is due to both a decrease in carrier transit time and an increase in carrier drift velocity v_d, which are both related linearly to voltage and electric field:

$$t_{rn} = L^2 / \mu_e V \tag{6.6}$$

$$v_d = \mu_e \mathcal{E} \tag{6.7}$$

where t_{rn} is the carrier transit time, L is the electrode separation, μ_e is electron mobility and $\mathcal{E}$ is the electric field ($V = \mathcal{E} L$). The linear increase in photocurrent in response to greater applied fields is expected due to the linear relationship between carrier mobility and field. The flat plateau region of peak photocurrent generated as a function of voltage that appears above 8 V seen in Figure 6.7 (d) deviates from this linear relationship. The plateau is consistent with saturation of drift velocity of the carriers under high fields [24]. The phenomenon is frequently observed in semiconductor devices with short channels and high internal electric fields [34]. In this work large internal electric fields could build up in the depletion region as device becomes saturated with oxygen vacancies. In turn this may cause the carrier mobility to deviate from the expected linear relationship of applied field producing a saturation in the value of the drift velocity at high applied bias voltage.

In an effort to improve our analysis dynamic light pulsing experiments with the nanowire device in the saturated condition at each holding voltage was performed. This experiment attempted to introduce excess carriers through light stimulus alone to a system in a pseudo-steady state displaying no current change in response to a fixed voltage stimulus. To ensure the devices were in steady state, the device was held at each voltage for a period of time (previously determined to be sufficient to saturate the device) before introducing the laser light. Only when the device was close to steady state was the UV stimulus introduced for two 20 second pulses. The results are shown in Figure 6.8 (a). Each plot is normalised to only show

the excess photogenerated current ie I_{ph}-I_{dark}, with I_{dark} defining the device current with no illumination. The photocurrent is significantly more stable with time over the course of the UV pulse width than prior. Implying a stable population of carriers is present in the device. Figure 6.8 (b) recaptures the linear increase (slope 0.37 nA/V) in photocurrent to a maximum saturated value at high applied bias seen before in Figure 6.7 (d) (slope 0.25 nA/V).

Under pseudo steady state conditions with greater time resolution it's possible to observe the photocurrent response time and persistence time of the generated photocurrent in the device. The photocurrent persistence times are plotted in Figure 6.8 (c) at each voltage. The peak heights are normalised for clarity. The photogenerated carriers persist the longest at lower voltage bias ~ 20 s at 2 volts with current persistence ~ 2 s at 10 volts. The persistence current is directly related to carrier lifetime and drift velocity as well as the recombination rate G_e.

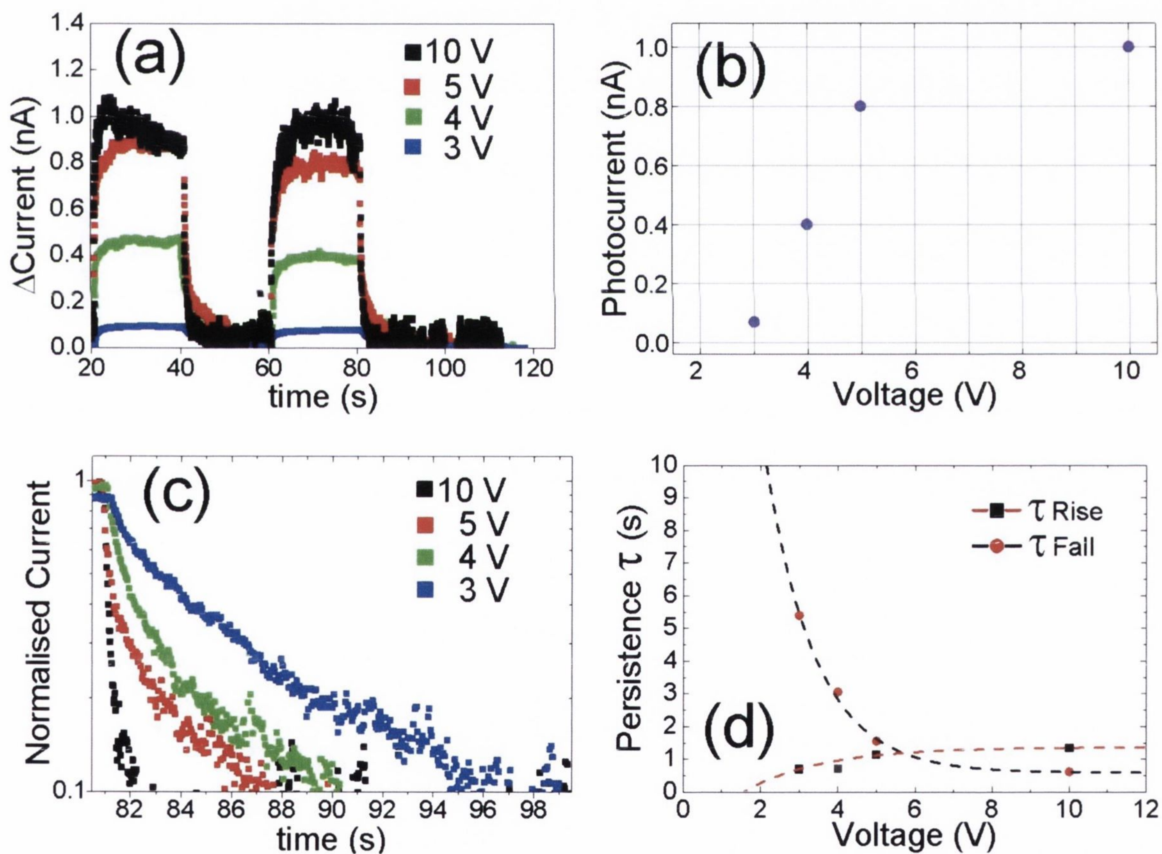


Figure 6.8 Pseudo steady state device characteristics with UV stimulus. The nanowire device is brought to saturation at each voltage before two 20 s UV pulses are applied to the device. (a) The photocurrent is given at each voltage where evidence of exponential growth and decay of the photocurrent is observed. (b) Photocurrent plotted as a function of applied voltage, again a linear increase (slope 0.37 nA/V) followed by a plateau is observed. (c) The decrease in photocurrent is normalised to one peak to compare the time it takes for the photocurrent to dissapate. (d) Fitting each decay to an expontial decay function similar to that in equation (9) Each time constant τ (persistence) as a funciton of voltage is extracted and plotted. Dotted lines are single exponential fits for τ_{Fall} and τ_{Rise}.

$$G_e = \frac{n}{\tau} \tag{6.8}$$

Where n is excess carrier density corresponding to the photogenerated current and is related to carrier lifetime (after the light is turned off) by the following:

$$n(t) = n(0)\exp\left(\frac{-t}{\tau}\right) \tag{6.9}$$

$n(0)$ is the initial number of carriers. In Figure 6.8 (d) at each voltage bias a single exponential decay function is fitted to each photocurrent decay [35]. From the fit its possible to extract and plot the carrier lifetime τ_{Fall} as a function of the change in voltage. Similar fits are performed to establish the time it takes the photocurrent to reach its maximum value and extract the rise time τ_{Rise}. The plot reveals the asymmetry between the lifetimes of τ_{Fall} and τ_{Rise}. The rise time is faster than the fall time particularly at low voltages.

The asymmetry may be explained in part by the UV stimulus generating extra oxygen vacancies during the pulse, but overall the photocurrent persistence time will be longer than the rise time due to intrinsic and extrinsic photoexcitation of carriers in the TiO_2. Oxygen vacancies introduce more trap states below the conduction band of the TiO_2 [36]. UV light will evacuate occupied trap states quickly, but when the light is removed any excess carriers caught in these trap states may persist there for longer before relaxing back to the valence band. The rise and fall times presented here are similar to those for 2D materials such as MoS_2 and graphene [37, 38] while they are orders of magnitude shorter than amorphous oxides [39]. These carrier dynamics can also be heavily influenced by the surrounding atmosphere [40, 41]. Future work will involve investigating the change in persistent photocurrent as the device atmosphere is altered and the defect composition in the material is varied.

6.3.3 Correlated Voltage and Light Pulse Stimuli

The results presented in this chapter and the previous chapter together describe the nanowire device characteristics in response to voltage and UV stimulus. Some long term persistence effects and history dependence in the wire which are indicative of stimulus dependent evolutionary behaviour have been demonstrated. As shown earlier, correlated voltage and UV stimuli brings the device to saturation current faster than voltage stimulus alone. Then, when a voltage only stimulus is applied to the device after the correlated UV/voltage stimuli, it approaches saturation current faster than the first initial voltage only stimulus. The device appears to remember the correlated UV/voltage stimuli, which implies a longer term material modification or change in the wire. To capture this action and try produce device learning a set of pulse sequences that contained both voltage and UV stimuli that fired independently and synchronously was designed.

The optimum pulse sequence for device response and learning was discovered to be comprised of individual pulses of each stimulus separately before applying a subsequent pulse of simultaneous stimuli. Figure 6.9 presents the results of one such experiment. The device is pulsed with only voltage stimulus initially with no appreciable increase in current. The first type of stimulus involved a pulse train consisting of 1 volt step pulse on a 2 volt holding bias. The low voltage amplitude was chosen such that it would not affect a conductance change in the wire. As established in Chapter 5, the conductivity of the device can be altered used high amplitude (7.5 V) voltage pluses. Thus to rule out voltage induced memory and capture only the correlated stimuli behaviour these low amplitude voltages were required.

The UV stimulus pulse train consisted of laser pulses on top of a 2 Volt bias held on the device. As established earlier, the photocurrent created is a function of voltage (Figure 6.7 (d)). Under illumination with zero bias, no current is detected in the device. A 2 volt holding bias was the optimized value as it produced a small measurable signal (0.5 pA) and tied into the voltage only pulse train. The final pulse train is composed of both the voltage only and UV only pulse trains but was sequenced such that both stimuli are coincident on the nanowire device during repeated time intervals. Whenever the two stimuli are coincident there is a marked (x20) increase in current. Moreover, the response of the device grows over time demonstrating a learning behaviour.

The coincident dual stimuli pulse train elicits a current response from the device greater than the response from the sum of the two individual pulses (as seen for the voltage and UV only

stimulus pulse trains). Physically, the action of a stepping from two volts to three volts produces a small set of excess carriers (in addition to those generated under 2 volts) with a density of n_V via the introduction of oxygen vacancy n-type dopants. Similarly, under UV stimulus an excess carrier density of n_{UV} is created by charge separation and oxygen vacancy creation (cf equations (6.1) and (6.2)).

The excess carriers created when the coincident voltage and UV pulse stimuli hit the device (n_{CO}) are not equal to the sum of the carriers created by the separate stimulus alone. There is a significant difference in device behaviour when both pulses are applied simultaneously to the device. The observed behaviour is not simply the sum of each stimuli when applied separately to the device. Thus the action of stepping from 2 V to 3 V when the device is exposed to light generates more current through the device relative to the sum of each applied separately.

There are no similar reports of this type of behaviour in the literature. This phenomenon is not well understood, but it's possible to propose a mechanism that could explain such an increased device response. To begin to rationalise this behaviour the nature of the device band structure is first considered. In the previous chapter the dynamic nature of the Schottky barrier interface region as more oxygen vacancies were introduced to the wire was established. These oxygen vacancies are mobile dopants with a +2 charge in the lattice that define the depletion region of the nanowire at the metal interface. A diode depletion region is defined as the region containing ionised dopants – dopant atoms that have lost a charge carrier to the conduction or valence band. These ionised dopants give the depletion region an associated built-in voltage which will vary as the voltage across the diode can ionise further dopants. This is shown schematically in Figure 6.10 (a) for a standard Schottky diode. In contrast to standard diodes where the ionized dopants are frozen in the lattice, oxygen vacancies are free to move about the lattice under an applied field. In nanowire devices, the oxygen vacancies that define the depletion are drifting in response to the voltage stimulus, hence the depletion region width and built in voltage will be dynamic. The high electric field in the depletion region is ideal for separating electron hole pairs generated via UV stimulus. This serves to increase excess carrier lifetime and therefore current. Figure 6.10 (b) captures this proposed mechanism schematically.

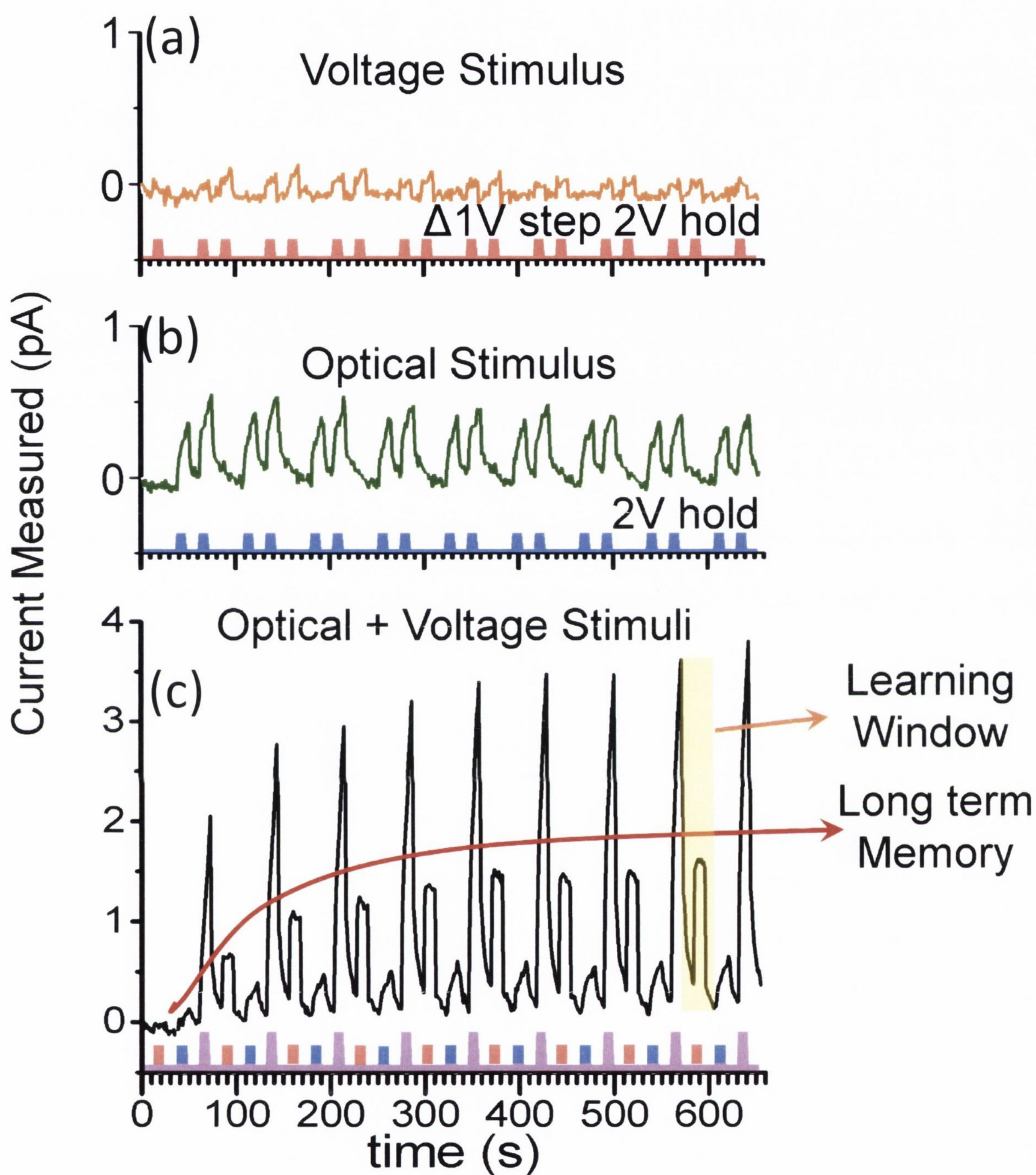


Figure 6.9 Associative memory in TiO_2 nanowire devices. (a) Voltage only pulse stimulus response. (b) Optical only pulse stimulus response. (c) The two heterogeneous stimuli – voltage and light – when applied simultaneously are associated to produce a high current response in the device. The next subsequent voltage-only pulse produces a similar high current response thereby demonstrating associative memory. Additionally, the excess current generated under coincident stimulus of light and voltage is greater than the sum of each stimulus applied separately as shown in two offset plots below the coincident pulse train.

Simultaneous optical and voltage stimulus produce a larger amount of excess carriers than the sum of the excess carriers of each stimulus applied separately. What's more, the coincident stimuli appears to affect a greater material change in the wire. This is evident in the high current response of the device following the application of a voltage pulse applied immediately after the coincident pulse. The mechanism by which the combined stimuli produce a long lasting material change in the wire may only be speculated upon. It may be related to the persistence lifetime of photogenerated carriers discussed earlier (cf. Figure 6.8 (d)).

The effect of the combined stimuli may be likened to Hebbain STDP learning introduced in an earlier section. The device, much like biological synapses has been made 'stronger', i.e. more conductive, due to the creation of more excess charge carriers after the two stimuli fired in quick succession. However this effect alone does not constitute learning or memory itself. The associative memory is revealed after a subsequent voltage-only pulse produces a greater current response in the device as seen in Figure 6.9. Associative memory was introduced earlier as the ability to associate two separate stimuli to produce one response. Through time and conditioning the same response can be produced using only one of the applied stimulus. In this case voltage and UV stimuli are associated together following their coincident pulse and produce a high current response. After the coincident pulse a voltage only stimulus is required to produce a similar high current response. This is associative memory and learning in response to heterogeneous stimuli and hence the device can be considered a novel type of neuromorphic semiconductor hardware.

Traditional photodiodes display a photocurrent independent of applied bias response with no history effects similar to those reported here. In this instance the device has a 30 second learning window after the coincident pulse during which the voltage only pulse can be applied and the device responds with a larger than normal current. The window is seen in Figure 6.9 as an apparent exponential decay (marked in yellow) in current following the coincident pulse stimulus, the time window is on the same time scale as that observed in Figure 6.8 (d). Pulsing voltage stimulus in this window produces the high current memory effect. Over the course of the entire pulse train the high current memory effect is observed to grow with each post-coincidence voltage-only stimulus. This action is more subtle and suggests a long term memory effect is taking place in the device.

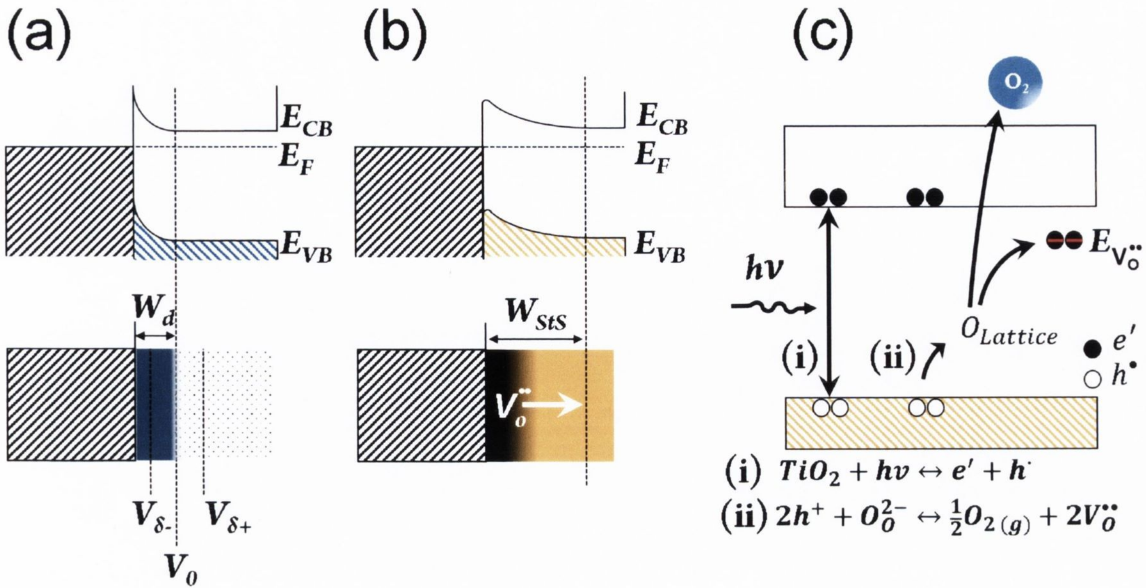


Figure 6.10 Depletion regions in semiconductors are regions of high electrical field with a built in voltage due to ionized dopant atoms. (a) The depletion layer width W_d is defined by the voltage applied to the semiconductor as more dopants become ionised under stronger voltages. Dopant atoms are frozen in the semiconductor lattice and lose or gain an electron in response to an electric field. (b) Oxygen vacancies are not distributed about the TiO_2 nanowire initially. They are introduced at the metal/wire interface under applied bias and must then drift under bias to generate a depletion region. The degree of band bending and built in field strength will therefore change dynamically as voltage is applied until a steady state depletion width is created - W_{StS}. (c) This effect serves to increase the degree of charge separation when UV stimulus is applied as the high field in the depletion region sweeps the excess carriers away before they can recombine.

6.4 Summary and Outlook

The effect of UV light stimulus on TiO_2 nanowire devices was investigated. Exposing the chip to UV light for 15 minutes dramatically increased device conductivity. UV exposure can reduce device forming time significantly in comparison to voltage forming. Using a custom built laser set up mounted in the probe station allowed the dynamic effects of pulsing UV laser light on the wires and the device current response to be monitored in real time. Holding both UV and voltage pulses on the device was found to develop the saturated state of the device faster than holing a voltage pulse alone.

The word "TiO_2" was successfully reproduced in Morse code while monitoring the current through the device in response to a specific UV laser pulse sequence. Dynamically pulsing UV light during a 10 staircase like bias with 1 Volt step increments revealed that the excess current generated by UV light interaction or photocurrent was linearly dependent on voltage. The drift velocity of excess carriers was then observe to saturate under high applied bias. Further UV pulsing experiments were carried out under pseudo steady state conditions where current levels through the device were not changing rapidly with time for a given voltage. Under these conditions, the excess carrier lifetimes were extracted by fitting single exponential decay functions to the decay of photocurrent. The carrier lifetimes appeared to persist longer at lower voltage bias and disappeared exponentially faster at higher voltage levels.

Finally, two heterogeneous stimuli are applied simultaneously to produce a surprisingly large amount of excess current in the device. Following the coincident pulse a voltage stimulus only is required to reproduce a high current state in the device once more demonstrating practical associative memory. The device displays many neuromorphic properties including a STDP-like strengthening of current as well as long term memory.

To date the associative memory effect has only been realised in semiconductor like devices for homogeneous stimulus by combining two separate voltage pulses [42]. The significance of this observation in our nanowire devices will be realised as sensor or novel neuromorphic hardware to tackle many of the challenges outlined at the start of this chapter. These include a reduction in periphery components needed to convert various stimuli into a stimulus the device can respond to and low power neuromorphic behaviour. This device may be developed to realise true neuromorphic computational systems on a similar level of biologic systems including the brain.

6.5 References

1. James, C.D., *Toward exascale computing through neuromorphic approaches*. 2010. p. Medium: ED; Size: 18 p.
2. Liu, S.-C. and T. Delbruck, *Neuromorphic sensory systems.* Current Opinion in Neurobiology, 2010. **20**(3): p. 288-295.
3. Costas-Santos, J., et al., *A Spatial Contrast Retina With On-Chip Calibration for Neuromorphic Spike-Based AER Vision Systems.* Circuits and Systems I: Regular Papers, IEEE Transactions on, 2007. **54**(7): p. 1444-1458.
4. Culurciello, E., R. Etienne-Cummings, and K.A. Boahen, *A biomorphic digital image sensor.* Solid-State Circuits, IEEE Journal of, 2003. **38**(2): p. 281-294.
5. Liu, W., A.G. Andreou, and M.H. Goldstein, Jr., *Voiced-speech representation by an analog silicon model of the auditory periphery.* Neural Networks, IEEE Transactions on, 1992. **3**(3): p. 477-487.
6. Koickal, T.J., et al., *Analog VLSI Circuit Implementation of an Adaptive Neuromorphic Olfaction Chip.* Circuits and Systems I: Regular Papers, IEEE Transactions on, 2007. **54**(1): p. 60-73.
7. Pearce, T.C., *Computational parallels between the biological olfactory pathway and its analogue `The Electronic Nose': Part II. Sensor-based machine olfaction.* Biosystems, 1997. **41**(2): p. 69-90.
8. Pearson, M., et al. *A Hardware Based Implementation of a Tactile Sensory System For Neuromorphic Signal Processing Applications*. in *Acoustics, Speech and Signal Processing, 2006. ICASSP 2006 Proceedings. 2006 IEEE International Conference on*. 2006.
9. Roy, D., *Design and Developmental Metrics of a 'Skin-Like' Multi-Input Quasi-Compliant Robotic Gripper Sensor Using Tactile Matrix.* Journal of Intelligent and Robotic Systems, 2006. **46**(4): p. 305-337.
10. *Official Titan Supercomputer Homepage*. Available from: https://www.olcf.ornl.gov/titan/.
11. Keleman, S., *Slow Attending: The Art of Forming Intimacy.* 2012.
12. Williams, R.W. and K. Herrup, *The Control of Neuron Number.* Annual Review of Neuroscience, 1988. **11**(1): p. 423-453.
13. ; Available from: http://commons.wikimedia.org/wiki/File:Complete_neuron_cell_diagram_en.svg#mediaviewer/File:Complete_neuron_cell_diagram_en.svg.
14. Pavlov, I., *Conditional Reflex, An Investigation of The Psychological Activity of the Cerebral Cortex*. 1927: New York, Oxford University press.
15. Hebb, D.O., *The Organization of Behavior: A Neuropsychological Theory*. 2012: Taylor & Francis Group.
16. Feldman, Daniel E., *The Spike-Timing Dependence of Plasticity.* Neuron, 2012. **75**(4): p. 556-571.
17. Indiveri, G., et al., *Neuromorphic silicon neuron circuits.* Frontiers in Neuroscience, 2011. **5**.
18. Arthur, J.V. and K.A. Boahen, *Synchrony in Silicon: The Gamma Rhythm.* Neural Networks, IEEE Transactions on, 2007. **18**(6): p. 1815-1825.
19. Ananthanarayanan, R., et al. *The cat is out of the bag: cortical simulations with 109 neurons, 1013 synapses*. in *High Performance Computing Networking, Storage and Analysis, Proceedings of the Conference on*. 2009.
20. Snider, G., et al., *From Synapses to Circuitry: Using Memristive Memory to Explore the Electronic Brain.* Computer, 2011. **44**(2): p. 21-28.
21. Chua, L.O., *Memristor-The missing circuit element.* Circuit Theory, IEEE Transactions on, 1971. **18**(5): p. 507-519.

22. Strukov, D.B., et al., *The missing memristor found.* Nature, 2008. **453**(7191): p. 80-3.
23. Chua, L., *Resistance switching memories are memristors.* Appl. Phys. A 2011. **102**(4): p. 765-783.
24. Sze, S.M. and K.K. Ng, *Physics of Semiconductor Devices.* 2006: Wiley.
25. Reyes-Coronado, D., et al., *Phase-pure TiO 2 nanoparticles: anatase, brookite and rutile.* Nanotechnology, 2008. **19**(14): p. 145605.
26. Glassford, K.M. and J.R. Chelikowsky, *Optical properties of titanium dioxide in the rutile structure.* Physical Review B, 1992. **45**(7): p. 3874-3877.
27. Asahi, R., et al., *Electronic and optical properties of anatase TiO2.* Physical Review B, 2000. **61**(11): p. 7459-7465.
28. Burke, A., et al., *The Function of a TiO2 Compact Layer in Dye-Sensitized Solar Cells Incorporating "Planar" Organic Dyes.* Nano Letters, 2008. **8**(4): p. 977-981.
29. O'Regan, B. and M. Gratzel, *A low-cost, high-efficiency solar cell based on dye-sensitized colloidal TiO2 films.* Nature, 1991. **353**(6346): p. 737-740.
30. Steven H. Szczepankiewicz, A.J.C., Michael R. Hoffmann, *Infrared spectra of photoinduced species on hydroxylated titania surfaces.* Journal of Physical Chemistry B, 2000(104): p. 9842-9850.
31. T. Berger, M.S., O. Diwald, E. Knozinger, D. Panayotov, T. L. Thompson, J. T. Yates, *Light-Induced Charge Separation in Anatase TiO2 Particles.* Journal of Physical Chemistry B 2005(109): p. 6061-6068.
32. Bityurin, N., A.I. Kuznetsov, and A. Kanaev, *Kinetics of UV-induced darkening of titanium-oxide gels.* Applied Surface Science, 2005. **248**(1-4): p. 86-90.
33. Karaagac, H., et al., *Au/TiO2 nanorod-based Schottky-type UV photodetectors.* physica status solidi (RRL) – Rapid Research Letters, 2012. **6**(11): p. 442-444.
34. Thornber, K.K., *Relation of drift velocity to low-field mobility and high-field saturation velocity.* Journal of Applied Physics, 1980. **51**(4): p. 2127-2136.
35. Lopez-Sanchez, O., et al., *Ultrasensitive photodetectors based on monolayer MoS2.* Nat Nano, 2013. **8**(7): p. 497-501.
36. Janotti, A., et al., *Hybrid functional studies of the oxygen vacancy in TiO_{2}.* Phys. Rev. B, 2010. **81**(8).
37. Banerjee, A.N., *The design, fabrication, and photocatalytic utility of nanostructured semiconductors: focus on TiO-based nanostructures.* Nanotechnol Sci Appl, 2011. **4**: p. 35-65.
38. Konstantatos, G., et al., *Hybrid graphene-quantum dot phototransistors with ultrahigh gain.* Nat Nano, 2012. **7**(6): p. 363-368.
39. Jeon, S., et al., *Gated three-terminal device architecture to eliminate persistent photoconductivity in oxide semiconductor photosensor arrays.* Nat Mater, 2012. **11**(4): p. 301-305.
40. Nagashio, K., et al., *Electrical transport properties of graphene on SiO2 with specific surface structures.* Journal of Applied Physics, 2011. **110**(2): p. -.
41. Late, D.J., et al., *Hysteresis in Single-Layer MoS2 Field Effect Transistors.* ACS Nano, 2012. **6**(6): p. 5635-5641.
42. Pershin, Y.V. and M.D. Ventra, *Experimental demonstration of associative memory with memristive neural networks.* Neural Netw., 2010. **23**(7): p. 881-886.