

AN INVESTIGATION OF THE ELECTRICAL BEHAVIOURS OF METALLIC, SEMICONDUCTING AND CORE-SHELL NANOWIRES

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in the application for the degree of

Doctor of Philosophy in Chemistry

By

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DECLARATION

I, the undersigned, declare that this work has not previously been submitted as an exercise for a degree at this, or any other University, and that unless otherwise stated is my own work. Elements of this work that have been carried out jointly with others or by collaborators have been duly acknowledged in the text. I agree to deposit this thesis in the University's open access institutional repository or allow the library to do so on my behalf, subject to Irish Copyright Legislation and Trinity College Library conditions of use and acknowledgement.

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SUMMARY

Discoveries surrounding nanoscale one-dimensional (1D) structures, such as nanotubes, nanoribbons, and nanowires have the potential to revolutionize existing processes, give rise to completely new technologies and have an enormous impact on our everyday lives. 1D nanostructures provide access to unique physical and chemical properties not found in bulk and thin-film analogues.

As an alternative to conventional transparent conducting materials such as indium-tin oxide, metallic nanowire networks have attracted the attention of researchers looking to develop the next generation of flexible transparent conducting electrodes. Metallic nanowire networks could provide a route to highly transparent, highly conductive, flexible, easy-to-fabricate, low-cost materials. The large-scale integration of metallic nanowire networks in commercial devices could bring new types of displays and touch-screens to market, as well as numerous emerging applications including flexible lighting, thin-film solar cells, electrostatic shielding, antistatic coatings and thin-film heaters. To assess the true potential of metallic nanowire network systems, it is crucial to establish a complete understanding of their individual physical properties and how these properties affect the performance of the network. The junctions allow for the conduction of current between wires and enables the interconnectedness of the system. Characterising and optimising these elements is a central goal of this thesis and critical to the development of high-performance transparent conductors based on metallic nanowire networks.

In Chapter 3, the material and junction resistance of Ag (11 Ω), Cu (205 Ω), and Ag-coated Cu (424 Ω) nanowires are determined through precise 4-probe electrical measurements and a detailed geometrical characterisation of each nanowire sample. These experimentally measured values are used in chapter 4 for the development of a predictive multi-nodal computational model which considers the resistance contribution from the nanowire segments and the nanowire junctions. Instead of random computer-generated networks to model the behaviour of experimentally measured networks, a computational approach was developed which captures the precise spatial distribution of wires from a SEM image analysis. Experimentally reported data was matched with the optoelectronic performance

described using an ab initio model derived from fundamental material properties, electrical equations and optical transmittances based on Mie theory scattering of light by small particles. The predictive power of this model enables a material-by-design approach, whereby suitable systems can be prescribed for specific applications.

A further goal of this research is to engineer the coating of bare Ag nanowires to add new and novel functionality. One highly desirable response is the memristive behaviour demonstrated by TiO_2 . Chapter 5 describes the fabrication and characterisation of individual TiO_2 nanowire devices which display a continuum of resistance levels when electrically stressed; rather than a singular high- or low-resistance state which is commonly found. Through an electroforming step, the resistance of the nanowire device is reduced from 10^{12} to $10^8 \Omega$. The dynamic resistance response of the nanowire facilitates the formation of 6 and 11 level memory. Through a combination of optical and voltage pulses, single nanowire devices demonstrate an associative memory effect whereby a significant enhancement of the current response is observed when both electrical and optical stimuli are applied simultaneously.

TiO_2 is incorporated as the active element in a core-shell nanowire which combined a highly conductive Ag core with a TiO_2 shell, shortening the active switching region to the nanometre scale. In chapter 6 Ag nanowires are coated in sheaths of TiO_2 of various crystalline qualities and contacted using passive (Au) and active (Ag) electrodes or order to identify the ingredients necessary for controllable resistive switching. A polycrystalline TiO_2 shell and Ag electrodes allowed for controllable operation of bipolar and unipolar resistive switching modes. The presence of both switching modes is termed nonpolar resistive switching, this work demonstrates controllable nonpolar operation for the first time in a single nanowire system. The memory retention time can be selected by controlling the magnitude of the current used to activate the device. This allows for a short-term retention (up to 10^3 s) to be established in the bipolar state with long-term memory ($> 10^6$ s) in the unipolar regime. ON/OFF ratios of 10^5 and 10^7 are demonstrated for bipolar and unipolar modes respectively. These results provide a foundation for engineering resistive switching behaviours for memory storage and neuromorphic applications in core-shell nanowire structures.

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LIST OF ABBREVIATIONS

AC	Alternating Current
AE	Active Electrode
AF	Area Fraction
AFM	Atomic Force Microscope
ANN	Artificial Neural Network
BRS	Bipolar Resistive Switching
BSE	Backscattered Electron
CAD	Computer-Aided Design
CBRAM	Conductive Bridge Random-Access Memory
CC	Compliance Current
CCD	Charge Coupled Device
CE	Counter Electrode
CF	Conductive Filament
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CRANN	Centre of Research for Adaptive Nanostructures and Nanodevices
CVU	Capacitance Voltage Unit
DC	Direct Current
DEHA	Diethylhydroxylamine
DNQ	Diazonaphthoquinone
DUT	Device Under Test
EBL	Electron-Beam Lithography
ECM	Electrochemical Metallisation
EDA	Ethylenediamine
EDX	Energy Dispersive X-Ray Spectroscopy
EG	Ethylene Glycol
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
EtoH	Ethanol
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FTO	Fluorine Doped Tin Oxide
FWHM	Full-Width Half Maximum
HRS	High-Resistance State
HSQ	Hydrogen Silsesquioxane
IC	Integrated Circuits
IPA	Isopropyl Alcohol
ITO	Indium Tin Oxide

JDA	Junction-Dominated Assumption
LRS	Low-Resistance State
LTD	Long-Term Depression
LTP	Long-Term Potentiation
MCAG	Materials Chemistry & Analysis Group
MEM	Metal-Electrolyte-Metal
MIBK	Methyl Isobutyl Ketone
MIM	Metal-Insulator-Metal
MMA	Poly(methyl methacrylate – methacrylic acid)
MNR	Multi-Nodal Representation
MTP	Multiply-Twinned Particles
PET	Polyethylene Terephthalate
PLED	Polymer Light Emitting Diode
PMC	Programmable Metallization Cell
PMMA	Poly(methyl methacrylate)
PMU	Pulse Measure Unit
PRAM	Phase Change Random-Access Memory
PVP	Poly(vinyl pyrrolidone)
ReRAM	Redox Random-Access Memory
RF	Radio Frequency
RPM	Remote Pre-Amplifiers
RS	Resistive Switching
SAD	Selected-Area (electron) Diffraction
SCS	Semiconductor Characterisation System
SE	Secondary Electron
SEM	Scanning Electron Microscope
SERS	Surface Enhanced Raman Spectroscopy
SMU	Source Measure Unit
STDP	Spike Timing Dependent Plasticity
STEM	Scanning Transmission Electron Microscope
STP	Short-Term Plasticity
TBT	Tetrabutyl Titanate
TCM	Thermochemical Memory
TCO	Transparent Conducting Oxide
TEM	Transmission Electron Microscope
TMO	Transmission Metal Oxide
UHV	Ultra-High Vacuum
URS	Unipolar Resistive Switching
UV	Ultraviolet
VCM	Valence Change Memory
VLS	Vapour Liquid Solid

PUBLICATIONS

Resistance of Single Ag Nanowire Junctions and Their Role in the Conductivity of Nanowire Networks

ALLEN T. BELLEW, HUGH G. MANNING, CLAUDIA GOMES DA ROCHA, MAURO S. FERREIRA, AND JOHN J. BOLAND
ACS NANO, **2015**, 9 (11), 11422-11429

Ultimate Conductivity Performance in Metallic Nanowire Networks

CLAUDIA GOMES DA ROCHA, HUGH G. MANNING, COLIN O'CALLAGHAN, CARLOS RITTER, ALLEN T. BELLEW, JOHN J. BOLAND AND MAURO S. FERREIRA
NANOSCALE, **2015**, 7, 13011-13016

Effective Medium Theory for the Conductivity of Disordered Metallic Nanowire Networks

COLIN O'CALLAGHAN, CLAUDIA GOMES DA ROCHA, HUGH G. MANNING JOHN J. BOLAND AND MAURO S. FERREIRA
PHYSICAL CHEMISTRY CHEMICAL PHYSICS, **2016**, 18, 27564-27571

Associative Enhancement of Time Correlated Response to Heterogeneous Stimuli in a Neuromorphic Nanowire Device

CURTIS J. O'KELLY, JESSAMYN A. FAIRFIELD, DAVID MCCLOSKEY, HUGH G. MANNING, JOHN F. DONEGAN, AND JOHN J. BOLAND
ADVANCED ELECTRONIC MATERIALS, **2016**, 2 (6), 1500458

Nonpolar Resistive Switching in Ag@TiO₂ Core-Shell Nanowires

HUGH G. MANNING, SUBHAJIT BISWAS, JUSTIN D. HOLMES, AND JOHN J. BOLAND
ACS APPLIED MATERIALS & INTERFACES, **2017**, 9 (44), 38959-38966

CONFERENCE PRESENTATIONS

Oral Contributions:

‘Selected Area Deposition of Nanomaterials for Truer Simulations of Ag Nanowire Networks’

IEEE NANOTECHNOLOGY MATERIALS AND DEVICES CONFERENCE, CATANIA, SICILY.
OCTOBER 2014.

‘Selected Area Deposition of Nanowire Networks, Combining Experiment and Simulation for High-Performance Transparent Conductors’

E-MRS FALL MEETING, WARSAW, POLAND. SEPTEMBER 2015.

‘Nanowire Networks, From High-Performance Transparent Conductors to Engineered Resistive Switching’

TRINITY COLLEGE / UNIVERSITY COLLEGE DUBLIN DUBCHEM 3RD YEAR
POSTGRADUATE TALK, DUBLIN, IRELAND. MAY 2016.

‘Nanowire Networks, From High-Performance Transparent Conductors to Engineered Memristive Switching’

MRS FALL MEETING, BOSTON, UNITED STATES OF AMERICA. DECEMBER 2016.

‘Nonpolar Resistive Switching of Core-Shell Nanowires’

7TH ANNUAL WORLD CONGRESS OF NANOSCIENCE AND TECHNOLOGY, FUKUOKA,
JAPAN. OCTOBER 2017

1

INTRODUCTION

‘The true delight is in the finding out rather than in the knowing’

-Isaac Asimov

In 1959 Richard Feynman gave a lecture entitled ‘There’s Plenty of Room at the Bottom’.^[1] A great physicist, visionary and considered by many to be the father of nanoscience, his imagination outreached the capabilities of his time. The subtitle for this lecture was ‘An invitation to enter a new field of physics’, during his talk the term ‘nanotechnology’ was not used, as it did not yet exist. Nevertheless, it is fair to say that this lecture was a vision of what we now call nanotechnology. Feynman foretold the enormous advances that could be made if the properties of materials could be engineered at the nanoscale, stressing the potential breakthroughs in many areas of science if it were possible to ‘just look at the thing!’. Once scientists had the right tools and had developed the right techniques the age of nanotechnology began.

As society’s reliance on digital technology continues to increase, the importance of nanotechnology and the scope for potential impact broadens to cover almost every aspect of our lives. All high-tech products and everything digital in the modern world depends on nanotechnology, all material properties are controlled at the nanoscale; surface chemistry defines reactivity, all biological systems are grown by nature from nano-sized DNA, and inside digital micro-chips the interactions at the nano-level drive device performances. Today’s scientists deliberately engineer materials at the nanoscale to take advantage of their enhanced properties such as higher strength, lighter weight, increased control of the light emitted by luminescence, and greater chemical reactivity than their larger-scale counterparts.

Nanoscience is hugely interdisciplinary and describes the study of objects with one of their spatial dimensions smaller than 100 nanometres (nm), ten million times less than one metre. It has facilitated the scaling of electronics and integrated circuits to what we currently possess and will continue to bring innovations in the future.

Objects at these length scales can behave quite differently to bulk materials. Moreover, their classification depends on the number of nanoscale dimensions and exists in one of three categories: zero-dimensional (0-D), one-dimensional (1-D) and two-dimensional (2-D). Objects such as quantum dots and nanoparticles are sub-100 nm in all dimensions and are considered pseudo 0-D. 2-D objects have two dimensions outside of the nanoscale size range and in recent years have become a focal area in materials research, due to their heightened optical, electrical and catalytic properties; examples of which include graphene and other layered materials. 1-D materials are nano-sized in two dimensions but stretched to macroscopic length scales in the third. 1-D materials present as promising candidates to enable the next generation of electronic and optoelectronic components. Furthermore, they are ideal systems for exploring a large number of novel phenomena at the nanoscale. The electrical conduction properties manifest interesting emergent phenomena such as resistive switching as we will see in subsequent chapters. Investigating the electrical behaviour of nanowires of different composition, characterising and engineering new behaviours, this thesis provides original knowledge to the now enormous field of nanoscience.

The realisation of nanoscale objects through state-of-the-art synthesis and characterisation techniques continues to bring us toward Feynman's ultimate goal; a material-by-design approach, whereby behaviours and characteristics are tailored to specific needs, unlocking the ability to fine tune materials, create device components with new and exotic properties and reduce material waste. For this we need to further our understanding of how the fundamental building blocks of materials behave at a nanoscale level, develop tools which model and predict how these objects will come together, and what the material limits for application are.

This introductory chapter will begin with a discussion of nanowires and nanowire networks, introducing the field and then discussing the state-of-the-art and potential applications of both metallic and semiconducting nanowires. Following this, the fundamentals of resistive switching will be provided along with a relevant literature review, as the manipulation, characterisation, and application of different forms of resistive switching will be found throughout the subsequent chapters. This section will conclude with a discussion of memristors and memristive devices for use as synaptic emulators in hardware-based neuromorphic applications.

1.1 1-D Objects: Nanotubes and Nanowires

In 1991 Iijima first reported on the carbon nanotube (CNT),^[2] which are seamless cylinders of one or more layers of rolled up graphene; typically a few nanometres thick and up to half a metre long.^[3] Due to their ultra-high strength, high electron mobility and nanoscale dimensions they have been used in numerous applications such as composite materials, coatings and films, microelectronics, energy storage and biosensors. Most notably, CNT composites are commercially available in high-end sporting equipment, antifouling CNT paint is used to coat ship hulls, and the Juno spacecraft orbiting Jupiter uses a CNT based electrostatic-discharge (ESD) shield.^[4] Working with CNTs brings several challenges associated with synthesising or separating out all but one of the different chiralities which endow the CNT with semiconducting, metallic or insulating properties.^[5]

The interest toward 1-D research has reached other systems including metallic, semiconducting and core-shell nanowires. Whereas nanotubes are hollow structures, nanowires are solid (with atoms inside). A variety of techniques exist for the growth of different nanowire types, these include but are not limited to; vapour-liquid-solid (VLS) growth of semiconducting and phase change nanowires,^[6, 7] core-shell nanowires by single step solvothermal methods or post-synthesis coating,^[8-10] a polyol sol-gel approach for metallic nanowires (Pb, Pt, Ag, Au)^[11-14] and electro-deposition for template assisted monolithic or segmented axial heterostructured nanowires.^[15, 16] The next three sub-sections describe the current scientific research on individual metallic, semiconducting and core-shell nanowires (Figure 1.1).

1.1.1 Metallic Nanowires

Metallic nanowires are highly conducting; their small scale makes them perfectly suited as interconnects in future nanodevices.^[17] Despite the unprecedented level of control that is currently possible of the nanowire structure and physical dimensions, manipulation and electrical contacting of individual nanowires is an extremely laborious task. Single metallic nanowires are primarily used in research to explore the unique physical properties at the nanoscale. Individual metallic nanowire devices are generally used to characterise fundamental mechanical,^[17, 18] electrical,^[11, 19, 20] plasmonic^[21] and thermal transport properties^[22] (Figure 1.1(a-c)).

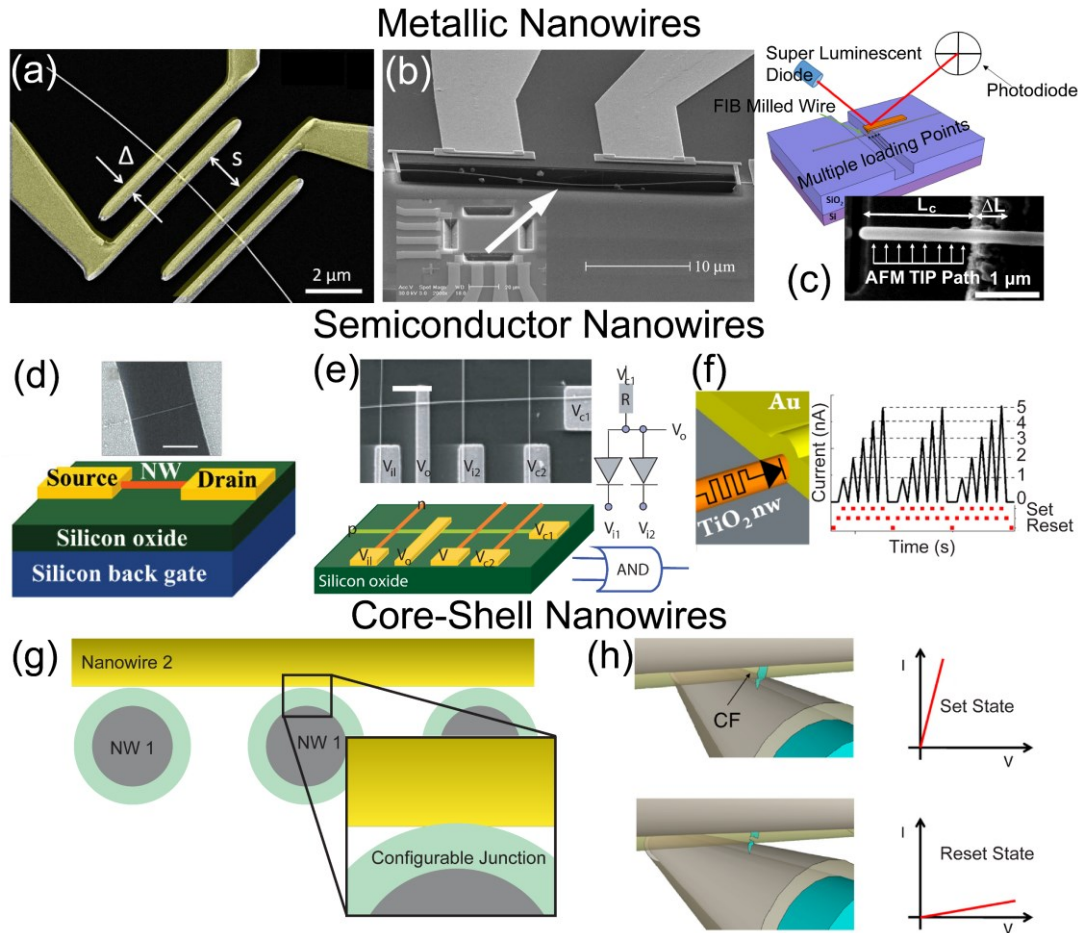


FIGURE 1.1. Examples of metallic, semiconducting and core-shell single nanowire devices. (a) Scanning electron microscope (SEM) image of a 4-probe electrical measurement of Ag nanowires.^[19] (b) Electrical and thermal transport of a single Ni nanowire.^[22] (c) Characterisation of the mechanical properties of Ag nanowires by an atomic force microscope (AFM) cantilever experiment.^[18] (d) Schematic of a GaN nanowire field effect transistor (FET), scale bar 2 μm .^[23] (e) Nanowire and nanotube-based transistor logic, schematic of logic and gate, scale bar 1 μm .^[24] (f) Schematic of a single TiO_2 nanowire demonstrating a range of controllable conductance states.^[25] (g) Schematic illustration and cross-sectional view of a crossbar nanowire memory switch.^[24] (h) Nanowire crossbar device, two perpendicular core-shell nanowires. A conductive filament (CF) shunts the insulating shell in the low-resistance ‘set’ state. The CF is broken in the high-resistance state.

1.1.2 Semiconductor Nanowires

Semiconducting nanowires have been utilised mostly as field effect transistors (FET)^[23, 26, 27] and gas sensors.^[27] Thin-film FETs are the building blocks of modern integrated circuits (IC), it is therefore understandable that researchers have been exploring the merits of nanowires for IC design (Figure 1.1(d)). While impractical to build in large quantities, proof of concept nanowire and nanotube-only transistor logic

has been demonstrated (Figure 1.1(e)).^[24] As well as traditional device architectures, single semiconducting nanowires of TiO₂ have been shown by our group to be capable of multilevel memory operation,^[25] and can respond in unique ways to time correlated heterogeneous voltage and optical stimuli (Figure 1.1(f)).^[28]

1.1.3 Core-Shell Nanowires

Core-shell nanowires have been explored as gas sensors,^[29, 30] supercapacitors,^[31, 32] photocatalysts,^[9] transparent conductors,^[10, 33] memristors^[34, 35] and resistive switching memory devices (Figure 1.1(g-h)).^[24, 36-38] One motivation for the use of nanowires is their extremely small dimensions, and control of physical parameters through the synthesis process, rather than through lithographic and deposition techniques. For resistive switching in core-shell wires, the shell behaves as the active switching layer, while the core plays the role of the electrical contact. By carefully choosing core/shell materials, different resistive switching behaviours can be demonstrated. This is a key ingredient to the core-shell structure and important for engineering desired behaviours in nanowire systems.

1.1.4 Resistivity in Nanowires

The electrical resistance (R) of an individual nanowire, depends on the length (l) of the wire, the nanowire cross sectional area (A) and the resistivity of the nanowire material (ρ_{nw}).^[39]

$$R = \frac{\rho_{nw}l}{A} \quad (1-1)$$

As the mean free path of the propagating electrons (in bulk Ag this is ~ 40 nm)^[40] becomes comparable to, or even larger than the nanowire diameter there is expected to be an increase of electron scattering due to grain boundaries and surface roughness of the nanowire.^[41] Solution grown nanowires (Au, Ag) typically have surfaces with extremely low roughness and when measured experimentally, have exhibited very little enhancement of ρ_{nw} .^[42] Surface scattering, internal grain boundary scattering, as well as impurity or point defect scattering all constitute the temperature-independent components of ρ_{nw} . The temperature-dependent aspects in non-magnetic metallic nanowires arise from electron-phonon interactions.^[43] An undesirable consequence of the current flow through thinner wires with a larger ρ_{nw} is a substantial increase in the local heating due to the Joule effect (also referred to as resistive or ohmic heating),

since the power per unit volume is expressed as $\rho_{nw}j^2$ where j is the current density. Moreover, the thermal stability and the maximum j a nanowire can withstand falls as the nanowire diameter shrinks.^[44] Since no single model can accurately predict the diameter-dependence of the nanowire resistivity, in this work, a range of values for ρ_{nw} are experimentally measured for each nanowire system under investigation.

1.2 Nanowire Networks

In 1999 Adelung et al. first introduced nanowire networks to the scientific community;^[45] their technique formed metallic and semiconducting percolating meshes of nanowires by adsorption onto strain lines on extremely flat surfaces. Since then, low-cost, high-throughput, solution-based methods such as dry-transfer,^[46] spray deposition,^[47] Mayer rod coating,^[48] inkjet printing,^[49] and roll to roll slot die printing^[50] have been used to assemble networks of randomly orientated nanowires. The performance of any collective is controlled by the interaction between the individual components; these properties are not only defined by the material but garnished with additional functionalities from being incorporated into the network. This includes; high porosity, optical transparency, a controllable level of interconnectedness and mechanical flexibility. Recently the term ‘nanowire network’ has been broadened to describe a random arrangement of nanowires on a surface, such that its connectivity allows for at least one and in most cases multiple pathways across the network. The annual growth of publications and citations in this field since the seminal paper in 1999 is shown in Figure 1.2. It is in this expanding area that nanowire networks have shown promise in a plethora of applications, including transparent thin-film heaters,^[44, 51] electromagnetic interference shielding,^[52] emergent programmable and tunable memories,^[53, 54] stretchable radio-frequency (RF) antenna,^[55] and polymer light-emitting diodes (PLEDs).^[56] Nanowire networks also appear to be promising substitutes for conventional transparent conducting materials, where their inherent flexibility, high porosity and high conductivities make them natural successors to current materials.^[40] In the following section, the evolution of nanowire networks for transparent conductor applications will be discussed.

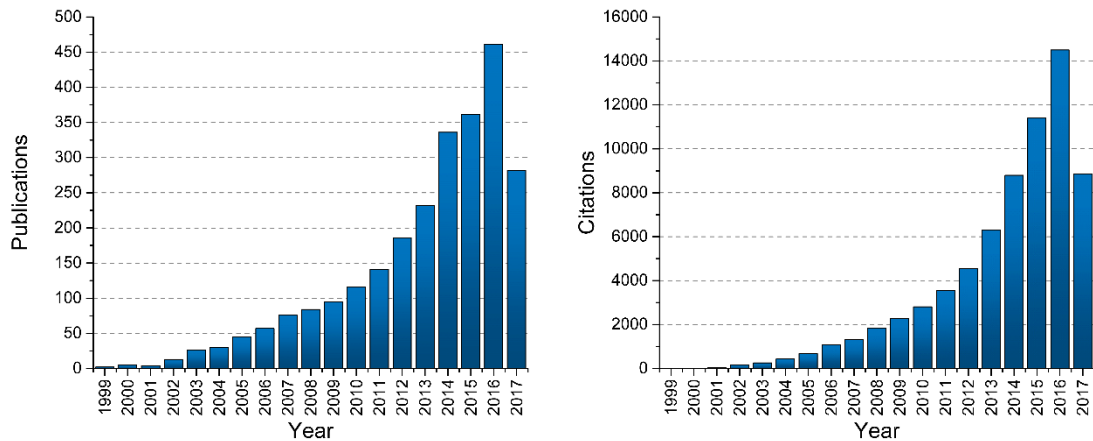


FIGURE 1.2. A bar chart illustrating the rising trend of publications and citations for the term ‘nanowire networks’ since 1999. Data downloaded from Thomson-Reuters Web of Science,^[57] September 2017.

1.2.1 Transparent Conductor Applications

Current photovoltaics, flexible light-emitting devices, touch screens and transparent thin-film heaters all rely on a highly transparent, highly conducting panel for operation. The current market leaders of transparent conducting thin-films have been transparent conducting oxides (TCOs), typically tin-doped indium oxide (ITO) and fluorine-doped tin oxide (FTO).^[58] ITO suffers from some major drawbacks: indium scarcity, high deposition temperatures and brittleness. Indium is a rare and highly expensive element that is only obtained through the by-product of mining other ores such as Zn and Pb. In fact, there are no ‘Indium mines’ as its concentration in minerals is too low to allow for economic extraction. Thus, the supply of indium cannot meet its demand without a significant price increase associated with its extraction.^[59] ITO films are deposited at a slow rate (the fastest film throughputs are around 0.01 m/s) and at a high processing temperature (400 °C).^[60] Additionally, less than 30 % of the ITO sputtered from a target is actually deposited on the substrate. This requires additional recycling infrastructure which further adds to the cost.^[61] Not only does the high temperature of deposition make it incompatible with plastic substrates, but also the brittleness of the oxide film can make screens rather fragile. As the market for electronic devices continues to shift toward thinner, and curved devices, flexible transparent conducting platforms will account for a huge share of the marketplace in the coming decades.^[62] ITO is therefore inherently incapable of keeping up with the

market demands for robust and flexible transparent conductors.^[63]

The search for ITO replacements has led the research community to consider some alternative materials.^[40] In particular, metallic nanowire networks have the potential to deliver next-generation devices based on flexible transparent conductors and electronics. Metallic nanowire networks possess key qualities which make them forerunners as replacements for conventional transparent conductors. Nanowire networks possess outstanding mechanical properties, showing excellent stability under both compressive and tensile bending,^[64, 65] and even when stretched.^[55, 66] Networks can be transferred to flexible substrates using a number of high-speed, low-cost manufacturing techniques, including established methods such as roll-to-roll slot-die coating.^[50]

To find their way into consumer products, these network films must exhibit similarly impressive transparency, and conductivity performances as TCOs currently guarantee. Industry standards for most applications require high optical transmission values, $T > 90\%$ (measured at a wavelength of 550 nm, which represents the maximum sensitivity of the human eye)^[67] over a range of sheet resistances (R_s) measured as ohms per square (Ω/\square) depending on the application (Figure 1.3). Typically $R_s \sim 10 - 100 \Omega/\square$ for screen, photovoltaic and lighting technologies.^[68] For transparent heater applications $R_s \sim 20 - 50 \Omega/\square$.^[40, 44] $50 - 200 \Omega/\square$ (capacitive) and $300 - 750 \Omega/\square$ (resistive) for touch sensors^[69, 70] and $1000 - 1300 \Omega/\square$ for electromagnetic interference (EMI) shielding and static dissipation coatings.^[59, 68, 70] Of all the metallic nanowire materials, Ag was the first to be considered as a promising substitute to ITO. Another aspect to consider is the haze factor (HF) of the nanowire network; this is defined as the proportion of the diffusive component of the transmitted light through the material. The scattering of light causes a loss in transmissive contrast and the ability to see through the material. For use in displays, where the ability to resolve light through the material is critical, haze must be kept to a minimum. However, large HFs are desirable in solar cells to increase optical path length within the active layer of the device.^[40] For nanowire networks, increasing the diameter of the nanowires increases the HF,^[71] decreasing the length also increases the HF.^[72] To minimize the HF one must reduce the amount of silver on the substrate or the thickness of the film.^[73]



FIGURE 1.3. A schematic of the resistance ranges required for each potential application of metallic nanowire networks as transparent conductors. Adapted from Bae et al.^[74]

Many research groups around the world have been committed to bringing this network material to market.^[46, 48, 56, 75-77] Today, companies are starting to manufacture Ag nanowire networks for flexible transparent conductor applications. For example, Cambrios Technologies promises $R_s < 50 \text{ } \Omega/\square$ at transmittance values of $T \sim 95 \%$ for its Ag nanowire ink ‘Clearohm technology’.^[78]

1.2.2 Optimising Nanowire Network Performance

The optical performance (transmittance) of a nanowire network is set at the time of fabrication, it is determined by the number of nanowires per unit area (density) and physical dimensions of the nanowires which form the network. The electrical sheet resistance of some metallic nanowire networks as deposited is typically immeasurable. This is due to the presence of surface layers – molecules, surfactants, polymers^[12] and native oxides^[10]; essential to stabilise these materials during synthesis and processing, presenting as a barrier to electrical connectivity. For example, the widely-used polyol synthesis process for Ag nanowires results in a thin polymeric coating on the surfaces of the wires. This non-conducting polymer layer prevents a low-resistance contact from being formed at the nanowire contact points (junctions) as deposited.

If the junctions inside a nanowire network are highly resistive, the sheet resistance of the network will be very high. Conversely, if the junction resistances can be optimised to be very low, the network properties will be a combination of the resistance contributions from both the junctions and the nanowires themselves.

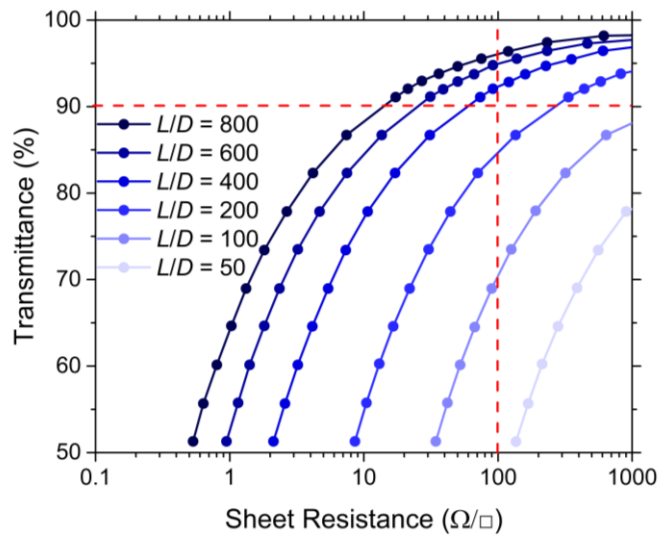


FIGURE 1.4. A plot of the calculated transmittance vs simulated sheet resistance of Ag nanowire films for L/D ratios ranging from 50-800. Red lines indicate the criteria for transmittance $> 90\%$ and sheet resistance $< 100 \Omega/\square$. Reproduced from Mutiso et al.^[68]

A variety of methods have been used to try to optimise the network by improving its junction resistances (R_{jxn}). Thermal treatments on a hotplate or in a furnace are most common and have yielded low-resistance networks.^[65, 79] Other methods such as mechanical pressing,^[80] capillary-force-induced cold welding,^[81] plasmonic welding due to excitation by a broadband white light source^[75] and removal of the polymer coating by a room temperature plasma treatment have also created, low-resistance networks.^[82] The improved conductivity of nanowire networks can also be obtained by passing appropriate current through the material. In fact, controlled electrical activation and breakdown of these layers allows for tunable conductivity of networks as more and more junctions activate and are strengthened relative to the current allowed to flow through them.^[54] It has also been shown that by increasing the nanowire aspect ratio L/D , where L is the nanowire length and D is its diameter, the nanowire networks performance could be improved as less junctions are necessary to construct a percolating pathway (Figure 1.4).^{[83] [68, 84]} The scaling of D is only viable to a certain limit, as discussed in section 1.1.4, when D approaches the mean free path of the electrons in Ag (roughly 40 nm in pure bulk Ag) there will be an increase in the electrical resistivity of the wire caused by scattering. The increase in resistivity means that thinner nanowires will be subjected to larger Joule heating effects, and have also been shown to possess lower thermal stability. As of September

2017, the highest reported Ag nanowire aspect ratio is held by Li et al. who have demonstrated conducting films with a transmittance of 99 % composed of Ag nanowires with an aspect ratio of 2000 ($L = 40 \mu\text{m}$, $D = 20 \text{nm}$).^[85] The work presented in chapter 3 includes an extensive study and measurement of the electrical properties of metallic nanowires.

1.2.3 Predicting the Optical Transmittance in Nanowire Networks

Various approaches have been outlined in the literature to correlate the density of nanowire networks with their optical performance. Early techniques involved relating the R_s and T of nanowire networks to the thickness of a thin film through the extrapolation of bulk to percolative behaviours, however, this semi-empirical model does not account for the nanowire dimensions.^[86, 87] Another approach, is to combine experiment and theory to model the optical properties and predict the transmittance of the network. Bergin et al.^[84] and others^[40, 68] have developed models with good agreement to experimental data. However, these calculations are limited in their use, that is, they may rely on diameter and wavelength dependent fitting parameters, or may only apply for networks within the percolation regime *i.e.* networks which are quite sparse ($T > 90 \%$), these fitting parameters will be investigated in chapter 4.

A Mie light scattering theory of nanowires was developed to predict the transmittance and haze depending on the diameter of the wires and the surface fraction coverage (density) of the network.^[73] This method relies an exact theory (*i.e.* a series approximation to a solution of Maxwell's equations) which has no fitting parameters and depends only on the diameter of the nanowire and the optical constants of the material.^[88] The solution of the scattering of electromagnetic waves by a sphere was developed by Gustav Mie in 1908 to explain the colourful effects of colloidal Au dispersions. Today, Mie theory is widely used in astrophysics, physics, chemistry, meteorology and engineering. The cross-section of scattering by a sphere illuminated with non-polarized light is defined as,^[88]

$$\sigma_s = \frac{2\pi}{k^2} \sum_{n=1}^{\infty} (2n+1)(|a_n|^2 + |b_n|^2) \quad (1-2)$$

Where $k = \frac{2\pi}{\lambda} n_1$ is the wavenumber; λ is the wavelength of light; n_1 is the real part of the refractive index of the medium which surrounds the scattering particle; a_n and b_n

represent the expansion coefficients of a scattering electromagnetic field in vector spherical harmonics,

$$a_n = \frac{m\psi_n(mx)\psi'_n(x) - \psi_n(x)\psi'_n(mx)}{m\psi_n(mx)\xi'_n(x) - \xi_n(x)\psi'_n(mx)} \quad (1-3)$$

$$b_n = \frac{\psi_n(mx)\psi'_n(x) - m\psi_n(x)\psi'_n(mx)}{\psi_n(mx)\xi'_n(x) - m\xi_n(x)\psi'_n(mx)} \quad (1-4)$$

Where $m = \frac{n_s}{n_i}$ is the relative refractive index; n_s is the real part of the refractive index of the scattering particle; $x = ka = \frac{2\pi n_1 a}{\lambda}$ is the size parameter; a is the radius of the scattering particle; $\psi_n(\rho) = \rho J_n(\rho)$, $\xi_n(\rho) = \rho H_n^{(1)}(\rho)$ are the Riccati-Bessel functions; $J_n(\rho)$ is the Bessel function of the 1st kind of n -order; $H_n^{(1)}(\rho)$ is the Bessel function of the 3rd kind of n -order.

Another scattering structure for which an analytical solution has been developed is the infinite cylinder, which allows the application of Mie theory to nanowires. In this formulation, the incident plane wave, as well as the scattering field are expanded into radiating spherical vector wave functions; the internal field of the wire is expanded into regular spherical vector wave functions. A boundary condition is imposed on the surface of the object and the expansion coefficients of the scattering field can be computed.^[89] The scattering field is measured at a certain distance to the scattering structure so that the relationship between the electric field and magnetic component behave like a freely propagating wave and have equal magnitudes at any point in space, this is known as the far field solution. Considering the case where an infinite cylinder of radius a interacts with an incident wave, the extinction coefficient (C_{ext}) at normal incidence is equal to,^[73]

$$c_{ext.s} = \frac{2\lambda L}{\pi} Re[T_s(0)] = Re\left[\frac{2\lambda L}{\pi} (a_0 + \sum_{n=1}^{\infty} a_n)\right] \quad (1-5)$$

$$c_{ext.p} = \frac{2\lambda L}{\pi} Re[T_p(0)] = Re\left[\frac{2\lambda L}{\pi} (b_0 + \sum_{n=1}^{\infty} a_n)\right] \quad (1-6)$$

$$T_s(\theta) = a_0 + 2 \sum_1^{\infty} a_n \cos(n\theta)$$

$$T_p(\theta) = b_0 + 2 \sum_1^{\infty} b_n \cos(n\theta)$$

$T_s(\theta)$ and $T_p(\theta)$ are dimensionless quantities which describe the angular dependence of scattering, for scattering in the forward direction $\theta = 0$. Furthermore, if the incident field is perpendicular to the axis of the cylinder the coefficients of scattering are given by,

$$a_n = \frac{mJ_n(mx)J_n'(x) - J_n'(mx)J_n(x)}{mJ_n(mx)H_n^{(1)'}(x) - J_n'(mx)H_n^{(1)'}(x)} \quad (1-7)$$

$$b_n = \frac{J_n(mx)J_n'(x) - mJ_n'(mx)J_n(x)}{J_n(mx)H_n^{(1)'}(x) - mJ_n'(mx)H_n^{(1)'}(x)} \quad (1-8)$$

For non-polarized light, the extinction coefficients for parallel (p) and perpendicular (s) components of the electric field which is incident on the cylinder contribute equally,

$$c_{ext} = \frac{c_{ext.p} + c_{ext.s}}{2} \quad (1-9)$$

It is important to note that the amount of light scattered is dependent on the diameter of the rods and their relative refractive indices to the surrounding medium, but not the length. For metallic nanowires, the refractive index is complex in the form $n_m + ik_m$ and dependent on the wavelength.

The analytical solutions to these equations are currently implemented in several computer programs originating in Fortran, but are also available in Java, C++, Pascal, as well as Python and MATLAB.^[90] In all instances, the above equations are solved in terms of an infinite series and involve the accurate calculation of spherical Bessel functions.^[91] There has been limited use of Mie theory to predict the optoelectronic properties of metallic nanowire networks despite the fact that it has accurately described experimental data.^[73, 92, 93]

1.2.4 Alternatives to Ag in Nanowire Networks

Ag nanowire networks have drawn considerable attention as replacements for conventional transparent conducting materials, however, due to the high cost and scarcity of Ag it could be economical to consider other cheaper materials. Cu is only 6 % less conductive than Ag, but is 1000 times more abundant and 100 times cheaper.^[94] In 2005, Chang et al. demonstrated a synthesis method which resulted in ultra-long Cu nanowires with aspect ratios $\sim 350 - 450$.^[95] Five years later, Rathmell et al. improved on this method and reported the properties of Cu nanowire networks

as flexible transparent conducting films with sheet resistance of $15 \Omega/\square$ at $T = 65\%$.^[96] Recent developments in Cu nanowire synthesis have allowed nanowires with aspect ratios as high as 5700 to be grown.^[94] Such ultra-high aspect ratios with performances of $50 \Omega/\square$ at 90 % transmittance make Cu a viable alternative to Ag.

Cu, however, has a naturally occurring oxide coating which needs to be removed by an annealing step, or by selectively dissolving the copper oxides with a suitable acid.^[10] These processing steps are inconvenient and do not protect the nanowire from future corrosion. An additional issue faced by Cu is the red hue of the nanowire network films; tinted electrodes may be undesirable for many applications.^[96] Both of these issues have been tackled head-on by many research groups looking to make Cu nanowires a viable alternative to ITO. One method involves coating Cu nanowires in an electroless plating procedure. Stewart et al. have shown that plating Cu nanowire networks in Ni results in a remarkable resistance to oxidation at high temperatures and a more desirable grey hue of the transparent conducting film.^[61] Rather than coating networks post deposition, Cu nanowires can also be coated in a variety of metals (Ag, Au, Pt) in a solution-phase process, allowing for metallic core-shell nanowires. These films exhibit optoelectronic performances equivalent to Ag networks with similar aspect ratios. Cu core with a Ag shell (Cu@Ag) nanowires assembled into networks are not only conducting as printed but are far more resistant to oxidation.^[10] The electrical properties of individual Cu and Cu@Ag core-shell nanowires will be investigated in chapter 3.

Metallic nanowire networks appear as excellent substitutes to ITO as the flexible transparent conductor in a wide range of future electronics. For each application, the nanowire network may consist of materials chosen to suit the required criteria; these include transparency, sheet resistance, stability at high temperatures, mechanical robustness and price, this requires a materials-by-design approach. In this work, direct experimental data will be integrated with computer simulation, building a model which can predict network performances. This tool will be used to grade nanowire networks and suggest their potential for transparent conductor applications. Furthermore, it can predict the optimum performance of a network and its scope for improvement.

1.3 Resistive Switching Memory

This section will provide an introduction, the basic definitions and the main operating modes of *resistive switching* elements as it pertains to the work in this thesis. Redox-based resistive switching random-access memory (usually called *ReRAM*) is a term which is used to describe an element that can change its resistance value upon application of a suitable electrical stimulus, typically operating between a high-resistance state (*HRS*) and a low-resistance state (*LRS*). Volatility describes the length of time (retention time) for which the resistance change remains after the memory is set and the stimulus is removed. Retention is important as it distinguishes volatile (which requires constant power, such as conventional RAM) from non-volatile (retains information after the power is removed, as in solid state storage, hard drives and flash drives). Resistive switching memory cells are generally built as a capacitor-style cell where an insulator or highly resistive material ‘I’ is sandwiched between two (possibly different) metals, forming a metal-insulator-metal (MIM) structure. For nanowire devices, the MIM structure can be found at each junction between two overlapping nanowires, and at each of the electrode/nanowire interfaces. In this way, a nanowire network can be considered as an array of randomly interconnected MIM junctions. The emergent behaviours and convolutional nature of this system can be difficult to interpret. Therefore we first consider the fundamental building blocks of a network and perform electrical measurements on individual nanowires and their respective junctions.

1.3.1 Resistive Switching Mechanisms

Many physical phenomena are known to lead to resistive switching memory behaviour. The actual physical mechanism, while electrically induced in all cases, can be very different^[97] and will be discussed in subsequent subsections. The two most common operational modes of ReRAM devices are either bipolar or unipolar resistive switching (BRS and URS respectively). Figure 1.5 shows a classification of the resistive switching behaviour and a schematic current-voltage (I-V) diagram for voltage sweeps of an idealised bipolar and unipolar device. In typical operation, voltage pulses are used to operate the device, I-V curves are used in research to characterise conduction features and to determine the threshold voltages; at ‘ V_{SET} ’ the

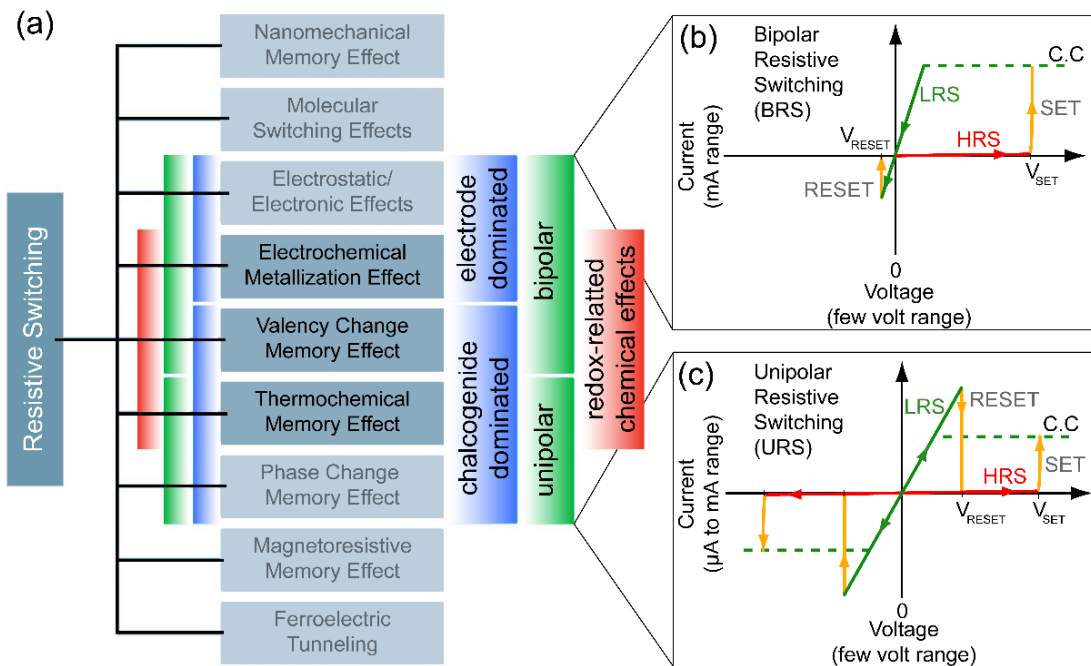


FIGURE 1.5. The classification and idealised I-V sweep operation of the resistive switching effects for the two most common operational modes of ReRAM elements. (a) Switching mechanisms based on thermal, chemical, and electronic/electrostatic effects are described in subsequent sections. (b) Bipolar resistive switching forms a LRS in the positive voltage direction up to a current compliance (CC) limit. Application of a negative voltage causes the device to reset. (c) The unipolar resistive switch is set in either positive or negative direction: a reset occurs when the current reached in the LRS exceeds the CC value and is sufficiently high to trigger a thermally assisted break of the conducting pathway. Adapted from Waser et al.^[97]

device turns ON whereas at ' V_{RESET} ' the device switches OFF.^[98] Moreover, I-V curves can provide important information which can help in deciphering the switching mechanism. Figure 1.5(b) shows a bipolar memory element which is SET to a LRS using voltage of one polarity (positive) and RESET to a HRS when subjected to a voltage applied in the opposite polarity (negative).^[97]

In contrast to this polarity dependence, a unipolar memory element, such as the one shown in Figure 1.5 (c) can be SET and RESET at the same voltage polarity, switching the device from a LRS to a HRS depends only on the magnitude of the current flow. In each case, a *current limiting compliance* (CC) is enabled during the SET procedure to avoid damaging the element and to optimise its operation. READ operations are performed at much smaller voltages ($V_{READ} \ll V_{SET}$) to detect the state of the system without a noticeable change in the resistance state.

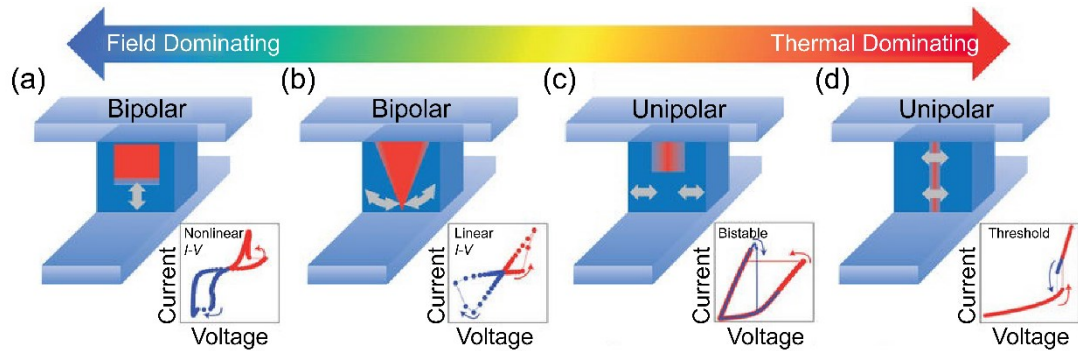


FIGURE 1.6. A schematic of the driving forces and electrical characteristics for the switching of ionic based devices. (a-d) A simplified schematic of a typical crossbar-style cell. The conduction channel is shown in red through the blue switching matrix for four types of switching driven by electric fields and Joule heating effects. Inset to each schematic are the I-V curves for (a) bipolar nonlinear switching, (b) bipolar linear switching, (c) unipolar non-volatile switching and (d) unipolar threshold switching. Adapted from Yang et al.^[99]

Establishing an ohmic LRS requires that a conducting filament (CF) or channel is formed between the two electrodes. Cycling between the LRS and HRS means that this CF can exist in a connected and disconnected state.^[100] Operation of BRS or URS modes are generally not chosen by the user, but decided by the materials used in the construction of the MIM cell and ultimately by the physical forces which influence the nanoscale CF.^[101] This can depend on the atomic and electronic structure of the material, the presence of defects and how the insulator transports electrons or ions. The CF can result from dielectric breakdown,^[54] movement of metallic ions,^[102] oxygen vacancies,^[103] or the formation of a conductive phase.^[104]

Figure 1.6 adapted from Yang et al.^[99] displays schematics of MIM nanodevices exhibiting different switching behaviours. Sourcing a voltage across the MIM cell of nanoscale dimensions generates two main effects: the formation of intense electric fields across the junction ($\sim 10^6$ V/cm) and Joule heating. Both effects coexist in all switching devices however their relative importance varies. This can be broken down into four main classes of switching which are most commonly observed in MIM switches. Figure 1.6(a) displays a device where the growth and retraction of the conductive region is driven by an electric field. The I-V inset shows what could be attributed to a rectifying Schottky-like barrier behaviour in the OFF state and a nonlinear residual tunnelling-like response in the ON state.^[99] Figure 1.6(b) shows an

alternate type of bipolar switching which has a linear I-V curve in the ON state. The CF bridges the top and bottom electrode allowing for the metallic conduction. The driving force in this switching class is a combined effect of electric-field induced drift and thermally enhanced diffusion of the ionic species. Increasing the function of the thermal effect leads to unipolar type switching as shown in Figure 1.6(c). The SET process can resemble the voltage driven dielectric breakdown but with a greater reliance on heat assisted ionic motion.^[105] The RESET of a unipolar device is generally attributed to a thermal rupture (as in a macroscopic fuse) of the CF. Figure 1.6(d) evidences that a significant current flow is required to change the insulating material to metallic conduction, however, this is a volatile transition, i.e. the LRS is not retained once the electrical stimulus is removed.

1.3.1.1 Electrochemical Metallisation Memories (ECM)

This section describes a resistance change that relies on metal cation transport and redox reactions in MEM or MIM structures. Various names and acronyms have been applied to this type of switching mechanism: programmable metallisation cell (PMC)^[106], conductive bridge random access memory (CBRAM)^[107] and *electrochemical metallisation* (ECM) memory.

In 1547, Ercker reported the growth of Ag dendrites from heated argentite (α -Ag₂S).^[108] Almost 300 years later, Michael Faraday grew and electrically measured Ag whiskers from Ag₂S and established the thermodynamic theory of ionic conduction.^[109] In 1976, Hirose was the first to report electrical switching behaviours due to Ag dendrite formation and dissolution using Ag-photodoped α -As₂S₃ in a lateral MEM structure.^[110] Later on Kozicki et al. adapted the lateral arrangement to a vertical structure and demonstrated non-volatile resistive switching,^[111] since then ECM has become the focus of intense research. It has been shown to be a non-volatile memory with low-power operation and excellent prospects of scalability to atomic dimensions.^[108]

Figure 1.7 shows a typical ECM cell which is constructed by sandwiching a solid ion conductor (which can be one of a large list of known oxides, chalcogenides or halide materials, the only stipulation being that the material is a metallic ion (M^{z+}) conductor^[102]) between two metal electrodes. The device typically uses an oxidizable

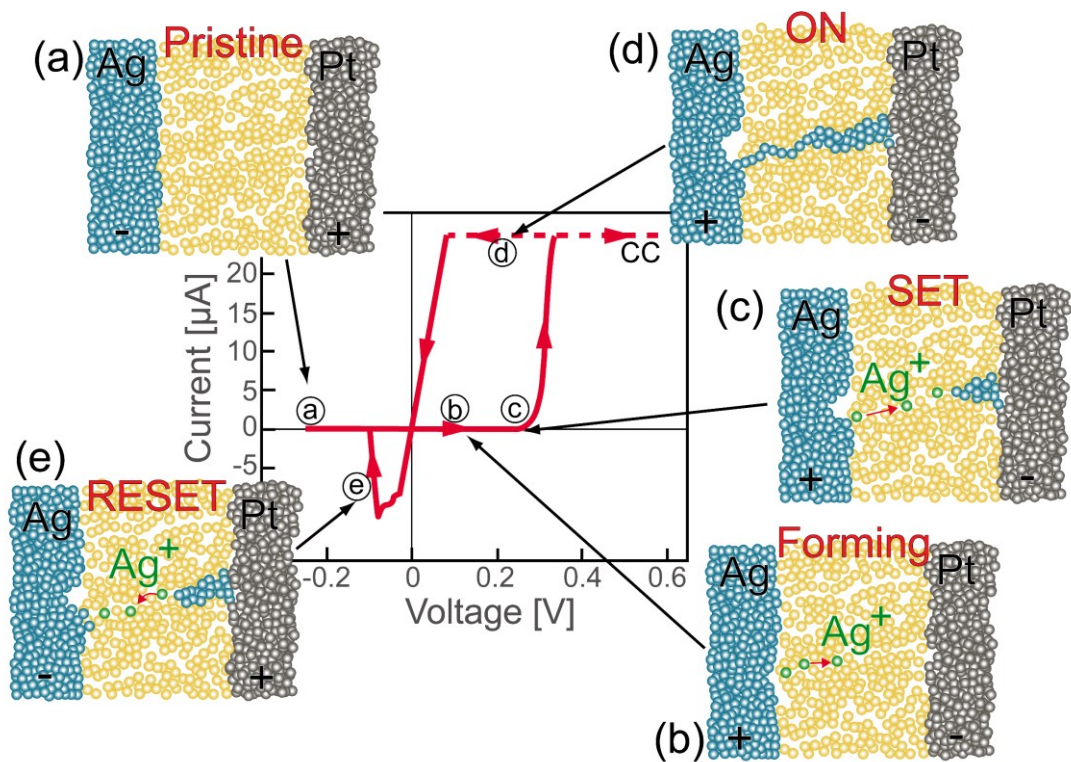


FIGURE 1.7. The operation of an electrochemical metallisation (ECM) memory cell through a full SET (a-d) and RESET (e) cycle. When voltage is applied to a cell which is in the pristine HRS, as in panel (a), no current flows. (b) Electrochemical reactions begin within the cell when the Pt electrode is sufficiently negatively-biased with respect to the Ag electrode causing Ag cations to move towards the Pt electrode. (c) Once they reach the electrode, the cations electrodeposit and a CF begins to grow towards the Ag electrode. (d) Once a metal filament has bridged the electrodes, the cell switches into a LRS. (e) The cell retains the ON-state unless voltage of an opposite polarity is applied and the metallic filament breaks down. CC denotes the current limiting compliance which is set during the experiment. Adapted from Valov et al.^[112]

or soluble active electrode (AE) such as either Ag or Cu. The counter electrode (CE) is usually electrochemically inert, for example, Au, W, TiN, Pt etc.^[98] In its pristine state, an ECM cell is non-conducting and does not show any metallic electrodeposit on the inert electrode (cf. Figure 1.7(a)). As a positive bias voltage is applied to the AE anodic dissolution of Ag occurs per the reaction,



where Ag^+ denotes the metal cations which drift across the solid-electrolyte towards the CE under the force felt by the electric field gradient (Figure 1.7(b)). When a cation reaches the CE, reduction and electro-crystallisation of the Ag occurs according to the

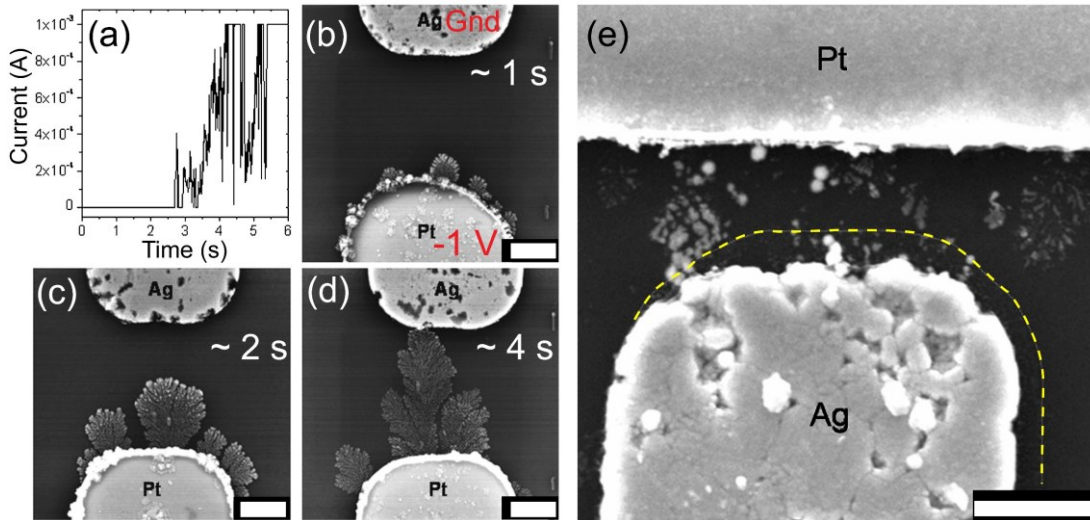


FIGURE 1.8. Visualisation of the ECM processes. (a) The switching-ON process with -1 V applied to the Pt electrode of a Pt/H₂O/Ag cell and a separation of 3 μ m between electrodes. (b), (c) and (d) are SEM images which show the Ag dendrite forming after applying the -1 V bias for 1, 2 and 3 seconds respectively. (e) SEM image of a Pt/H₂O/Ag cell after resistive switching to the ON state. The yellow dashed lines represent the original size of the Ag electrode. All scale bars represent 1 μ m, adapted from Guo et al.^[113]

cathodic deposition reaction given by,^[112]



Figure 1.7(c) shows the electrodeposit on the Pt CE and the metallic Ag filament growth towards the AE. The filament becomes a virtual cathode capturing Ag^+ species as they drift across the solid electrolyte. As sketched in Figure 1.7(d), once a metallic filament bridges the two electrodes there is a sudden increase in current, and the LRS is established. When the voltage is removed, the CF remains in place for a certain time, giving the non-volatile nature of the memory. The robustness of the filament has been shown to depend on the current limiting compliance set during the experiment.^[102] The connection is broken when a suitably large positive bias is applied to the CE causing the dissolution of the metallic filament (Figure 1.7(e)). The initial formation of the CF by these redox processes is widely accepted to occur in a winner-takes-all scenario,^[98, 114] whereby multiple filaments begin to nucleate initially from the CE and race to reach the AE as shown in Figure 1.8(b-d). Figure 1.8(e) clearly shows the anodic dissolution of the Ag electrode with the original size of the electrode before operation of the device depicted by the yellow dashed line. This experiment highlights the ease at which these reactions can occur; a -1 V bias applied

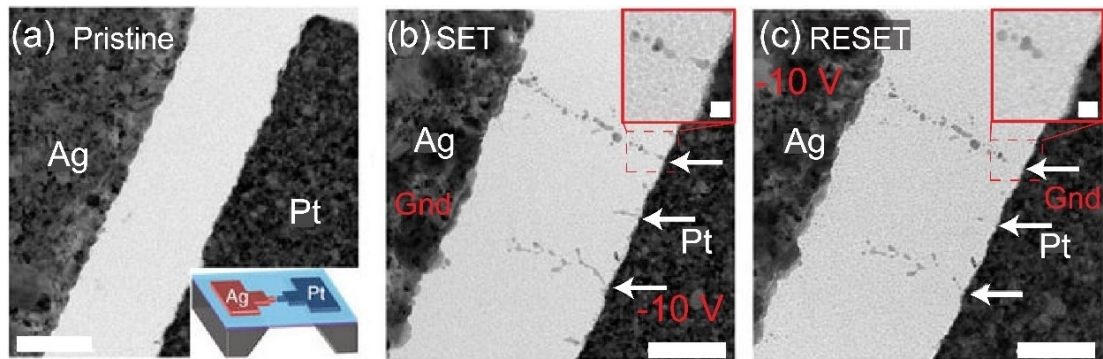


FIGURE 1.9. The observation of metallic filament formation and dissolution in SiO₂-based resistive switches. (a) Transmission electron microscopy (TEM) image of a pristine Ag-SiO₂-Pt cell fabricated on a SiN_x membrane. (b) TEM of the device after -10 V is applied to the Pt electrode for ~ 14 s. (c) TEM of the same device after +10 V was applied to the Pt electrode to RESET the device. Scale bars in main panels represent 200 nm while in the inset images represent 20 nm. Adapted from Yang et al.^[115]

to the Pt electrode for 4 s is enough to grow a bridging connection of Ag atoms across a 3 μm gap bridged by a small amount of deionised water.

The formation and dissolution process was superbly captured by Yang et al.^[115] and is displayed in the images of Figure 1.9. The first image shows the Ag/SiO₂/Pt device in the pristine state with an electrode separation ~ 465 nm (Figure 1.9(a)). When a -10 V bias is applied to the Pt electrode, electrodeposit Ag filaments were observed to grow from the CE towards the AE. Figure 1.9(b) shows the device once it has reached a current compliance level of 1.2 nA after ~ 14 s. Sourcing -10 V on the AE causes dissolution of the Ag dendrites (Figure 1.9(c)). Note that a substantial amount of material can remain in the switching area after the RESET. This may explain the large initial power requirements to form the device and lower voltages needed for subsequent programming. The growth of multiple branching dendritic filaments has been experimentally observed in lateral structures,^[113, 115, 116] but has proved to be challenging to visualise in vertically stacked memory cells with in-situ experiments. Further evidence of a spatially localised CF has been drawn from reports which show no dependence of the LRS resistance with device area.^[117, 118] Since Ag and (to a lesser extent) Cu are used throughout the work presented in this thesis, the ECM mechanism is very relevant to subsequent chapters.

1.3.1.2 Valence Change Memories (VCM)

Another major class of resistive switching devices are based on transition metal oxides (TMOs) such as HfO_x , SrTiO_3 , TaO_2 , ZnO , AlO_2 and TiO_2 .^[119] Resistive switching in metal oxides was first introduced in 1962 when Hickmott reported on a range of metal-oxide-metal cells.^[120] Today the electrical properties of TMOs are investigated for use as non-volatile memories, reconfigurable logic, analogue circuits and neuromorphic computing.^[121] In this section, we focus on TiO_2 based devices which are considered to be the archetypal resistive switching system. Here we provide a physical basis for the observed behaviours in chapter 5. TiO_2 has been shown to exhibit either BRS,^[122-124] URS,^[104, 125] or both, which when occurring in the same device is termed nonpolar resistive switching.^[126-129]

Anion-based memories are popularly referred to as *valence change memories* (VCMs).^[98] The valence change is triggered by the drift of anions (or their defects) due to internal electric fields. In general, the oxygen anion or the equivalently positively charged oxygen vacancy $V_{\text{O}}^{\bullet\bullet}$ (in Kröger-Vink notation)^[130] are the mobile species. VCM materials are most likely to be insulating and highly resistive in their pristine (as fabricated) states. Metal/semiconductor contacts are typically ohmic in the case of highly doped semiconducting material, and rectifying (Schottky-like) in the case of low doping.^[131] $V_{\text{O}}^{\bullet\bullet}$ are known to act as n-type dopants with the ability to transform the insulating oxide into a more electrically conductive doped semiconductor.^[132] Yang et al.^[133] illustrated these effects when two pairs of Pt and Pt/Ti electrodes were placed on top of a thin-film of single crystalline TiO_2 (Figure 1.10(a)). Figure 1.10(b) shows an energy band diagram for the Pt/ TiO_2 contact which results in a Schottky-like barrier and rectifying I-V characteristics between electrodes 1-3 and 2-4 (cf. Figure 1.10(c)). The addition of a chemically reactive Ti layer causes a further reduction of TiO_2 and a locally high concentration of non-stoichiometric TiO_2 (TiO_{2-x}) close to the metal/semiconductor interface collapsing the Schottky-like barrier and leading to ohmic conduction between electrodes 2-3 (Figure 1.10(c)).

Another significant attraction of VCM type memories is that the generation of $V_{\text{O}}^{\bullet\bullet}$ can be achieved electrochemically in a ‘self-doping’ process whereby $V_{\text{O}}^{\bullet\bullet}$ generation occurs at the anode interface by the following equation,^[97, 133]

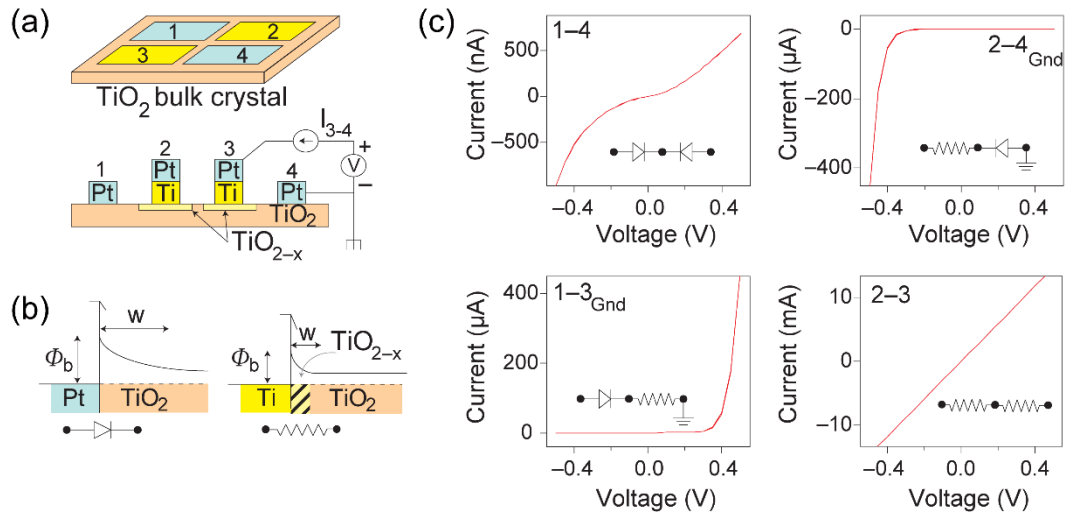
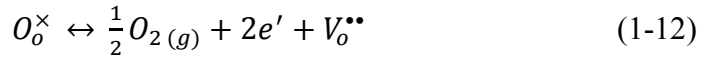
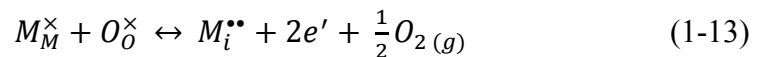


FIGURE 1.10. Junctions on single-crystal TiO_2 to illustrate the role of the interfaces in determining the electrical behaviour. (a) Schematic of the device layout. Four electrodes deposited on-top of a TiO_2 single crystal as Pt (blue) and Pt/Ti (yellow). (b) Energy diagram illustrating the low oxygen vacancy concentration under the Pt pads which results in a Schottky-like barrier (denoted by a rectifier). The high concentration of oxygen vacancies at the Pt/Ti interface causes the collapse of the Schottky-like barrier and produces an ohmic contact (denoted by a resistor). Φ_b and w are the electronic barrier height and width, respectively. (c) Four-probe I-V curves between combinations of the four pads shown in (a). The inserts to the I-V diagrams are the corresponding equivalent circuit diagrams. Adapted from Yang et al.^[133]



Oxygen vacancy formation is not the only cause of hypostoichiometric Ti, *i.e.* TiO_{2-x} . Cation (Ti) interstitials can also lead to hypostoichiometry by,



where M_M^{\times} denotes a cation species on a cation site with neutral charge and $M_i^{\bullet\bullet}$ represents a cation interstitial with a double positive charge. The dominant type in TiO_2 is dependent on the temperature; $V_o^{\bullet\bullet}$ and M_M^{\times} are low- and high-temperature stable defect types respectively.^[98]

Many VCM cells require an electroforming step to generate a population of charge carriers before repeatable and reproducible operation. During the electroforming step, oxygen vacancies introduced at the anode can drift toward and pile up at the cathode due to the applied electric field (Figure 1.11(a)). A large concentration of oxygen vacancies at the cathode can lead to an instability of the TiO_2 mother-phase.^[98] Sub-oxide phases, commonly known as Magnéli phases ($\text{Ti}_n\text{O}_{2n-1}$)

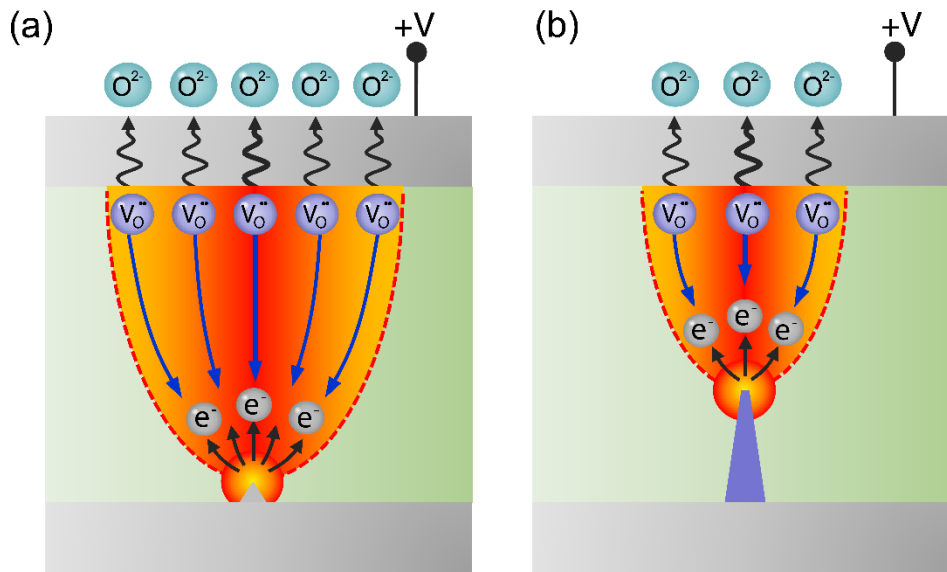


FIGURE 1.11. A schematic diagram of CF formation process in TiO₂. (a) Oxygen vacancies produced at the cathode drift toward the anode by the applied electric field. (b) At a critical concentration of defects, Magnéli phase CF can propagate back towards the cathode (blue pyramid, bottom to top), incoming oxygen vacancies deposit on the upper part of the growing CF giving the tapered shape. Reproduced from Kim et al.^[134]

can be formed and act like CFs growing towards the defect source (Figure 1.11(b)). Ultimately this increases the cell conductivity as the conducting paths have much lower resistivities than the TiO₂ phase.^[119, 135] The CF can be dissolved by running the cell in the opposite voltage direction making the device bipolar.^[136] CFs in Pt/TiO₂/Pt cells have been directly observed and characterised by TEM. Figure 1.12(a) shows a conical shaped CF composed of a single Magnéli phase which initiated growth from the cathode interface and progressed towards the anode.^[104] Hwan et al.^[137] reported that the CF can also be composed of multiple Magnéli phases and can be generated in the anatase form of TiO₂ (Figure 1.12(b)). This is remarkable as the Magnéli phase is a crystallographic shear plane from the TiO₂ rutile phase.^[119] Not only has hypostoichiometric TiO₂ been observed and characterised by TEM studies, but also by scanning transmission X-ray microscopy.^[136] This showed the phase transition involved with the formation of a sub-100-nm Magnéli phase as a result of the electroforming step. The observation of phase transitions driven by point defect accumulation adds further complexity to the switching mechanism. Currently, Magnéli CFs are the most generally accepted base mechanism to resistive switching, but the specifics are very much dependent on material and electrode composition.

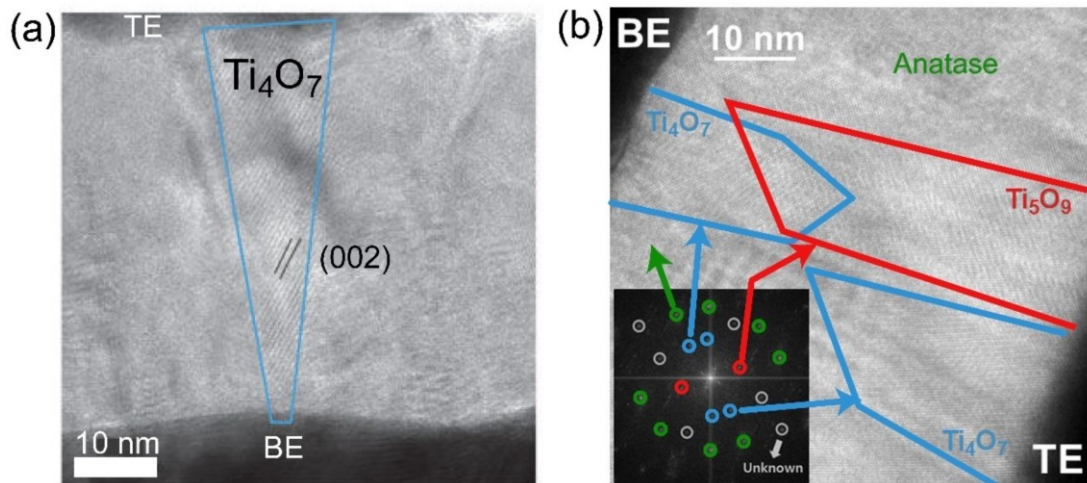


FIGURE 1.12. High-resolution TEM images of Magnéli phases in TiO_2 thin-film devices. (a) A single Ti_4O_7 CF bridging the top and bottom electrode. Adapted from Kwon et al.^[104] (b) Two different Magnéli phases Ti_4O_7 and Ti_5O_9 . The inset image shows the Fourier transform pattern. Adapted from Hwan et al.^[137]

It should be noted that forming induced phase-transitions have also been observed in other resistive switching TMOs, such as Ta_2O_5 ^[138] and CuO .^[139] Moreover, phase transition CFs may be vital in guaranteeing the long-term stability of the LRS in a memory cell, as an aggregation of point defects are supposed to undergo fast (coefficient of diffusion controlled) relaxation as soon as the external electric field disappears.^[140, 141]

1.3.1.3 Thermochemical Memory (TCM)

As mentioned in the previous section, TMOs may also display unipolar, or voltage polarity-independent resistive switching. It has been shown that in specific oxide systems, the resistive switching is not dominated by electrically driven forces but rather through thermally controlled diffusion and redox reactions (cf. Figure 1.6). This distinct class of resistive switching devices are referred to as *thermochemical memory* (TCM).^[142] URS was first described in 1964 by Gibbons and Beadle for thin NiO films.^[143] A significant number of materials have been investigated for URS behaviours in the past decade. The investigations have focused on thin-film devices to ensure compatibility with traditional complementary metal–oxide–semiconductor (CMOS) processing techniques. A large family of oxides have since been shown to exhibit TCM switching. NiO being the most studied system with other examples including TiO_2 ,^[144] HfO_2 ,^[145] and CuO_x ^[146] to name but a few.^[141] This section will

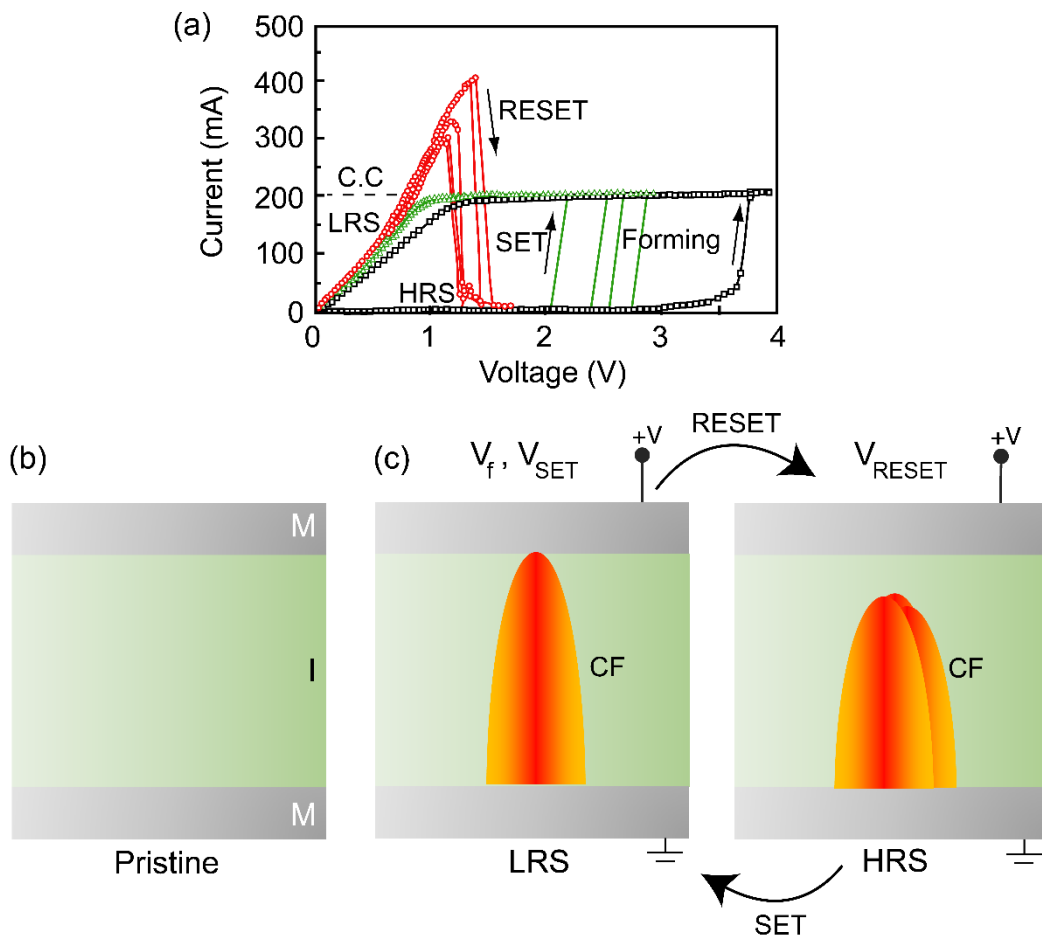


FIGURE 1.13. Overview of the TCM mechanism. (a) The I-V response of a unipolar ReRAM device. (b) The MIM structure of a unipolar cell in the pristine state. (c) Formation of the CF through the cell during SET and RESET operations. Adapted from Ielmini et al.^[98]

cover the basic operation and theory of TCM devices, as thermochemical resistive switching mechanisms are addressed in chapters 3 and 6 of this thesis.

As mentioned earlier URS cells typically require an electrical breakdown of the insulating oxide, or dielectric layer and the formation of a local path of increased conductivity.^[147] The initial forming step generally requires larger voltages than subsequent SET operations; the forming step also requires that a current-limiting compliance (CC) is set to prevent damage of the cell and determine the ‘strength’ of the CF.^[142] The CF can be composed of oxygen vacancies or metallic ions depending on the specifics of the TCM cell. During the forming sweep, an increasing voltage is sourced across the device until a sudden increase in current is observed and the CC is met (Figure 1.12(a)). The device is RESET by removing the CC and sourcing a voltage; when the current flow through the CF is sufficiently large the measured

current will suddenly drop, and the device is brought into the HRS. Subsequent SET operations occur at lower voltages than the forming voltage indicating that the pathway is only partially disrupted. The device can be cycled between the LRS and the HRS by repeating the SET / RESET process. As schematically shown in Figure 1.12(c), RESET and SET operations are related to the rupture/restoration of the conducting pathway due to a thermochemical assisted mechanism. The large currents required for the RESET are necessary to generate the large amount of Joule heating which disrupts the CF much like a traditional household fuse but on the nanoscale.^[108] Hence TCM is also referred to as the fuse/anti-fuse mechanism. It should be noted that localised filamentary switching has only been observed in TCM cells and uniform areal (across the whole contact area) switching has not yet been evidenced in URS systems.^[98]

Due to the filamentary nature of the switching process, TCM ReRAM cells are highly scalable. Moreover, the unipolar operation mode allows the use of two terminal diode selectors which have inherently higher scalability when compared to three-terminal transistor-based selectors.^[98] Advances in TCM ReRAM technology still face major challenges, e.g. the large power consumptions and high switching currents. While unipolar devices typically show high ON/OFF ratios and long retention times, the power densities required to invoke the RESET of the CF by Joule heating can cause device failure.^[142]

The previous three sections have provided a brief history, the basic definitions of ReRAM switching elements and their main switching modes. The reversible switching phenomena results in a non-volatile change in their resistance which is memorised by the element, therefore, in a broader sense, these types of elements have also been described as *memristive systems*.^[148] The term *memristive* will be used to describe the general characteristics of ReRAM elements which display analogue or multilevel features, rather than a binary resistive switching mode. It is therefore pertinent to discuss the basics of a memristor; its classification and potential application in hardware based neuromorphic systems

1.3.2 Memristors and Memristive Devices.

In 1971, Leon Chua proposed a new type of two-terminal fundamental circuit element called the memristor (memory-resistor).^[149] He devised a conceptual symmetry that sets the memristor as the fourth fundamental nonlinear circuit element as depicted in

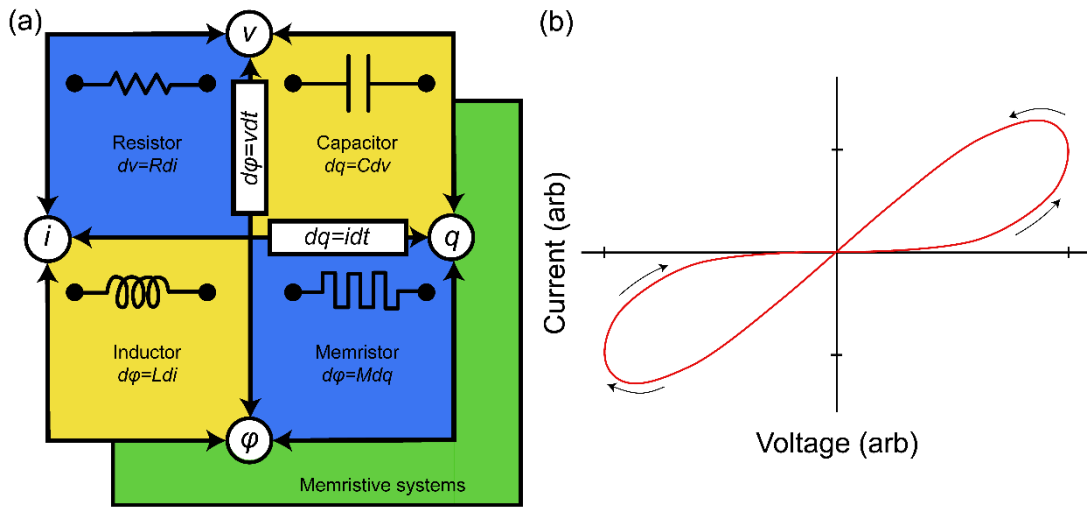


FIGURE 1.14. (a) The four fundamental two-terminal circuit elements as proposed by Leon Chua: resistor, capacitor, inductor and memristor. The more general term ‘memristive systems’ considers deviations from the ideal memristor case. (b) I-V plot of an idealised memristor showing a pinched hysteresis loop response. Adapted from Strukov et al.^[148]

Figure 1.14(a). A memristor is defined as a non-linear, passive, two-terminal circuit element whose memristance (M) is given by,

$$M(q) = d\phi_m/dq \tag{1-14}$$

$$M(q(t)) = \frac{d\phi_m/dt}{dq/dt} = V(t)/I(t) \tag{1-15}$$

Where ϕ_m is the magnetic flux linkage, q is the charge, and t is the time. The nonlinearity arises as q and ϕ are time dependent integrals of the circuit measurable quantities current (I) and voltage (V).^[119] This causes the memristor to be a continuously tunable resistor according to the operational history of applied voltage and current flow (Figure 1.14(b)).

In 1976 Chua and Kang expanded the concept of a memristor to that of a memristive system which has two (or more) state variables (a variable which describes enough about the system that its future behaviour in the absence of any external forces can be determined) that could now describe the response of thermistors and neuron ion channels.^[150] It was not until 2008 that HP Labs reported they had found the ‘missing memristor’ element when Strukov et al. demonstrated memristive behaviour in Pt/TiO₂/Pt thin-film cells and demonstrated a simple memristive model based on a linear-drift picture.^[148] While the model Strukov et al. have proposed captured the main signature of memristor-behaviour (recognised by a pinched hysteresis I-V loop),

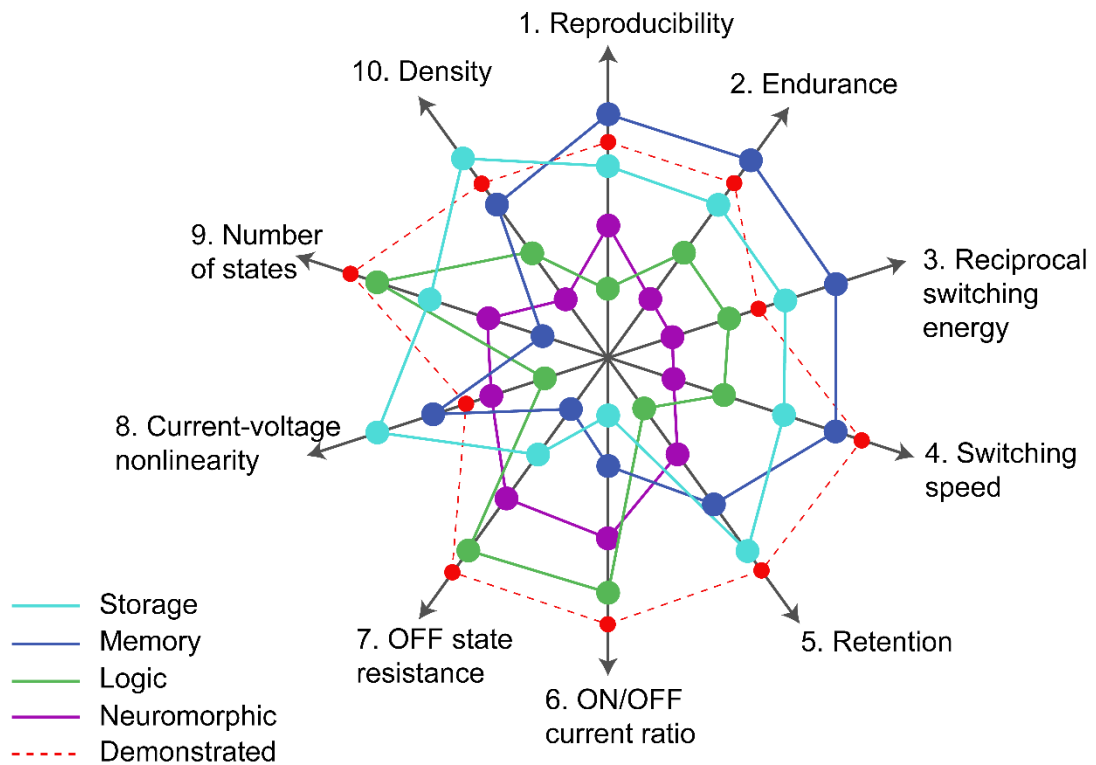


FIGURE 1.15. Device requirements for memristive applications. Device requirements are qualitatively ranked for four considered applications of memristive systems. Position on the axis further from the origin implies a higher requirement for the specific metric. The dashed line indicates the best reported memristive data in 2013 (for different devices). Quantitative estimates can be found in the referenced manuscript. Adapted from Yang et al.^[99]

it did not explicitly include the flux as in Chua's definition. In 2011 Chua published a manuscript in which he claimed all 'two-terminal non-volatile memory devices based on resistive switching are memristors, regardless of the device material and physical operating mechanisms'.^[151] This created a crisis of terminology with ReRAM and memristor scientific communities often failing to acknowledge one another.^[152] Typically, a VCM cell can display the pinched hysteresis response, induced by the dynamic self-doping characteristics which mimic memristor-like behaviours.^[34] Memristive qualities have also been shown in some ECM devices such as Ag/Si active layers where an engineered gradient leads to the formation of Ag-rich and Ag-poor regions.^[35, 153]

Recently, the term 'memristive' has been preferentially used to describe general characteristics of elements which display a continuum of resistance states rather than a binary classification. This inherently makes a memristor suitable for reconfigurable logic operations.^[154] Moreover, a memristor remembers its last state

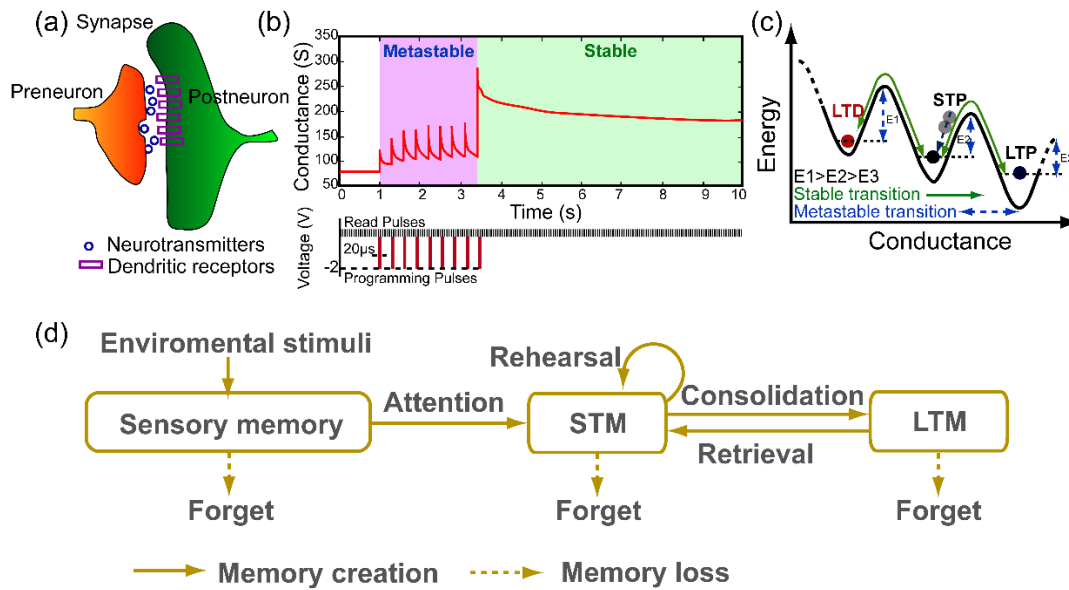


FIGURE 1.16. Short-term to long-term memory transition in memristive systems, which is analogous to biological synaptic strengthening. (a) Schematic illustration of a neural synapse where the strength (synaptic weight) of the connection is dependent on the quantity of neurotransmitters and dendritic receptors. (b) Schematic of identical - 2 V pulses inducing a transition from a metastable (volatile) to stable (non-volatile) regime in a memristive device. (c) Illustration of possible conduction mechanism that can cause an increase/decrease of conductance corresponding to long-term depression (LTD), short-term plasticity (STP) and long-term potentiation (LTP) along with the metastable transitions between each case. (d) Schematic of the multistore memory model. Adapted from Wang et al.^[34]

(even after the input stimulus is ceased) making it incredibly desirable for memory applications.^[99] In fact, the operation of a memristor is analogous to biological synapses making it perfectly suited for neuromorphic computing.^[155] In this way, memristors have the potential for industry-disruptive memory and logic applications. The required criteria for these applications were gathered by Yang et al.^[99] and are organised in Figure 1.15. While it is unlikely that one memristive device will be suited to dominate all these four areas, it currently represents the best option for hardware-based neuromorphic systems.

The adaptive nature of memristive devices provides an inherent learning ability directly in hardware, something that is mostly achieved nowadays on a software level via artificial neural network (ANN) algorithms. Despite its notable advances in bio-inspired computing/programming, the latter faces the characteristic bottlenecks associated with conventional CMOS computing.^[156] The learning ability at a hardware level has generated much interest in recent years as associative memory and other

typical neural operations can be mimicked directly in hardware (and not on programming instructions from software).^[157]

The human brain is a highly efficient computational system containing approximately 10^{11} neurons and 10^{15} synapses. The high efficiency and highly parallel processing power of biological systems result from the interconnectedness of the neurons, which is ultimately governed by synaptic activities.^[153] Synapses can be viewed as memristive systems whereby the device resistance can be associated to synaptic weights. The strengthening (potentiation) and weakening (depression) of a synaptic weight can be controlled from repeated stimuli (Figure 1.16(a)). A transition from a volatile to non-volatile state in a memristive system is analogous to a transition of short-term memory to long-term memory.^[158] Figure 1.16(b) is exemplary of this type of behaviour; a single pulse causes the transient storage of information as a conductance level, which decays at a certain rate. Multiple stimuli at a suitable interval can transition the system from a metastable to stable state, which has a much longer retention time.^[159] To induce the stable state, a critical energy barrier must be overcome. This is shown schematically in Figure 1.16(c); multiple programming pulses can supply enough energy for the transition through the metastable state. These effects emulate biological systems where by the stimulation rate and total number of stimulations represent a rehearsal and consolidation of certain information moving it from short-term to long-term memory (Figure 1.16(d)).

The concepts addressed in this section are key to understanding the behaviours of the memristive devices presented in chapters 5 and 6. As part of this thesis, heterogenous stimuli are used to illicit a nonlinear response in a single TiO₂ nanowires. Furthermore, the transition of short-term to long-term memory is explored in Ag core TiO₂ shell nanowires.

1.4 Thesis Scope and Summary

This chapter has served as a motivation and background to the areas which will be investigated in subsequent chapters: transparent conductor applications, resistive switching, memristive and neuromorphic behaviours. This thesis aims to describe and characterise the fundamental electrical behaviours of a group of metallic and semiconducting nanowires to engineer new types of memory behaviours and bio-inspired devices.

Chapter 2 will describe the background and theory of the equipment used in the measurements and discuss the experimental methods and procedures. Chapter 3 will describe the electrical measurements performed on single and crossed nanowires (Ag, Cu and Cu@Ag) to determine their conduction properties. The results of which demonstrate their potential for transparent conductor applications. In chapter 4, the results taken from individual Ag nanowires will be combined with precise electrical measurements on isolated Ag nanowire networks to develop a model which can describe the full electrical behaviour of random nanowire networks. This model incorporates not only the junction resistance contribution, but also the resistance contribution of the material, allowing for a precise determination of the ultimate performance of these networks. The electrical measurements on individual nanowires (Cu and Cu@Ag) will be used to describe the potential of these nanowire network materials for a wide range of transparent conductor applications through a materials-by-design approach. Chapter 5 will explore the rich electrical behaviours of semiconducting TiO₂ nanowires. The memristive properties of this system will be investigated for multilevel memory applications. An associative memory effect will be presented which shows an enhanced current response and learning behaviour when interrogated with correlated electrical and light stimuli. Chapter 6 will present a combination of the metallic and semiconducting materials in a core-shell structure. The shell structure and electrode composition will be designed in a way that results in controllable bipolar and unipolar resistive switching in a single nanowire device. The overlap between these two regimes will be investigated and a mechanism for the observed behaviours will be presented. Finally, the main conclusions and outlook resulting from this work will be summarised in chapter 7.

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2

EQUIPMENT AND METHODS

Nanofabrication requires the use of advanced tools and techniques for sample preparation, imaging, and measurement. This section describes in detail the methods used, equipment operation and background theory, as well as the specifics for sample fabrication and electrical characterisation which are used extensively throughout this thesis.

2.1 Microscopy

There are three basic types of microscopes: optical, charged particle (ion and electron) and scanning probe. The most familiar and most limited of these is the conventional optical microscope, where visible light and transparent lenses are used to resolve objects. However, there are constraints to the achievable resolution. Fundamentally, the resolving power of a microscope is not only bound to the quantity and quality of the lenses, but also by the wavelength of the light used to probe the specimen. This was formulised in 1873 by German optician Ernst Abbe as $d = \lambda/2n \cdot \sin\theta$ where n is the refractive index of the lens medium and θ is the half-angle subtended by the lens at the object.^[1] For white light, this corresponds to ~ 300 nm resolving power. A little more than 50 years later in 1924, Louis de Broglie showed that an electron could act as a wave, with an associated wavelength (de Broglie wavelength) given by $\lambda = h/m \cdot v$, where h is Planck's constant, m and v are the mass and velocity of the electron respectively.^[2] Using this principle, Ernst Ruska and Max Knoll pioneered the field of electron microscopy and surpassed the resolution limitations of optical microscopy. This powerful and versatile tool is now a key enabler of nanotechnology and vital for both fabrication and analysis in this work. The operation and theory behind each are described in this section.

2.1.1 Scanning Electron Microscopy

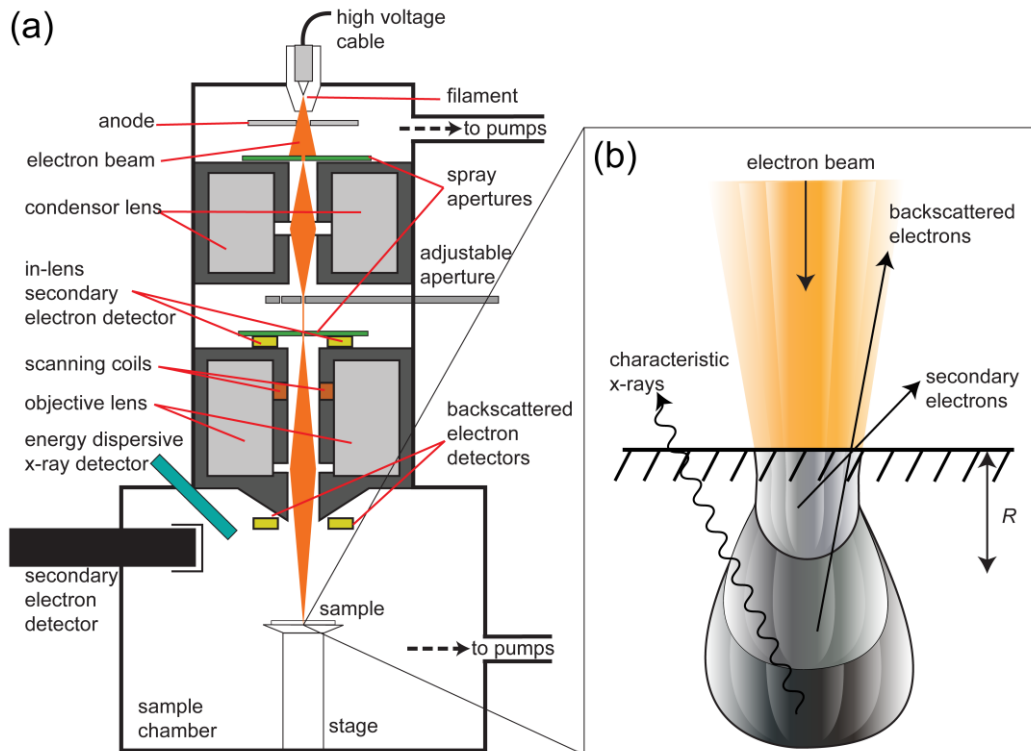


FIGURE 2.1. (a) A schematic illustration of a scanning electron microscope (SEM). The electron gun produces an electron beam, which is focused into a fine spot on the specimen surface using magnetic condenser and objective lenses. The beam is scanned in a rectangular raster over the specimen and the various signals created by the interactions between the beam electrons and the specimen are recorded. (b) Electron beam – surface interactions. The incident electron beam interacts with the sample volume in a number of different ways. Secondary electrons generated from the sample within the escape distance, R , are emitted from the surface. Backscattered electrons are deflected through elastic collisions in the sample material. Characteristic x-rays are produced by recombination of an electron and a hole created by the ejection of a secondary electron.

In 1931 Ruska and Knoll developed the first electron microscope, using electric and magnetic fields the paths followed by beams of electrons could be controlled in a similar way to how glass lenses are used to bend and focus visible light.^[3] With this, the pair heralded a new age in analytical techniques and fabrication possibilities earning Ruska the Nobel Prize in 1986.

It is not completely clear who first proposed the principle of scanning the surface of a specimen with a finely focused electron beam to produce an image. The first published description appeared in 1935 in a paper by the German physicist Max

Knoll.^[4] Another German physicist, Manfred von Ardenne, improved on Knolls design and performed experiments with what could be called a scanning transmission electron microscope (STEM) in 1937.^[5] Regardless, it was not until 1942 that three Americans, Zworykin, Hillier, and Snijder first described a surface scanning electron microscope (SEM) with a resolving power of 50 nm.^[6] The first commercially available SEM was brought to market by the Cambridge Instrument Company in 1965. Modern SEMs are a versatile platform with additional capabilities that extend far beyond basic imaging. This includes high-resolution imaging from multiple detectors, quantitative material analysis using energy dispersive x-ray spectroscopy (EDX), as well as nanofabrication capabilities through electron-beam lithography (EBL). All microscopy in this work was carried out on the microscopes provided by the Advanced Microscopy Laboratory of Trinity College Dublin, which includes the Zeiss Supra 40 SEM, the Zeiss Ultra Plus SEM, and the FEI Titan transmission electron microscope.

Figure 2.1(a) schematically details the main body of components inside a SEM, it also illustrates typical interaction types of a standard SEM electron beam. In an ultra-high vacuum (UHV) chamber, typically 10^{-8} Pa, a high energy electron beam (0.5 – 30 kV) is emitted from the electron gun and accelerates down the column. The beam of electrons are limited in width by the variable apertures and are focused using condenser and objective magnetic lenses into a fine spot on the sample surface. The focused beam is then rastered over the surface line by line in a rectangular pattern by the scanning coils. A multitude of detectors located inside the microscope measure the intensities of various signals created through the interaction between the beam electrons and the specimen. This information is stored in computer memory and mapped as variations in brightness in greyscale images on the computer display, colour can be added post-imaging for purely aesthetic reasons. Each type of interaction potentially constitutes a signal that carries information about the sample. High energy electrons interact with the atoms in the sample by inelastic and elastic collisions (Figure 2.1(b)). Most frequent interactions are inelastic collisions, whereby an electron is ejected from the sample atom with relatively low energy (< 50 eV). If this occurs close to the sample surface, within an escape distance, R , the liberated electron may be emitted to the vacuum and detected as a *secondary electron* (SE). This gives SE images very high spatial resolution and a strong topographic contrast of the sample

surface. The ejection of a core electron leaves a hole in the electronic orbital of the atom, the resulting electron vacancies are filled by electrons from a higher state, and an x-ray is emitted to balance the energy difference. The resulting x-ray energy is characteristic of the element from which it was emitted. This will be further expanded in section 2.1.1.2 as characteristic x-rays are key to the operation of EDX spectroscopy. Incident electrons may also interact with the nucleus of a sample atom and can be reflected after many elastic collisions. *Backscattered electrons* (BSE) can also cause the emission of SE as they travel through and exit the sample. The energy of a BSE varies significantly depending on the number of collisions, and the amount of BSEs is largely dependent on the atomic number of the scattering atoms in the sample.^[7] Through the use of the BSE detector, it is possible to determine regions of different elemental composition.

2.1.1.1 SEM Imaging and Contrast

All the phenomena involving electron beam/sample interactions are interrelated and all of them depend, to some extent, on the topography, the atomic number and the chemical state of the specimen. An image using a standard Everhart-Thornley SE detector^[8] (more commonly referred to as the SE2 detector) is shown in the main image of Figure 2.2. The SE2 detector is housed outside the column while the in-lens detector is situated within the electron column (Figure 2.1). The SE2 signal is used primarily for its strong atomic number contrast, this can be seen in the image as the higher atomic number materials (Ni and Au) appear brighter. The in-lens detector does not display the same sensitivity to atomic number, however it is much more surface sensitive. These characteristics can be observed in the inset of Figure 2.2 which is a composite, high-magnification image of the Ni electrode contacting a Ag core, TiO₂ shell (Ag@TiO₂) nanowire on a SiO₂ substrate using both SE2 and in-lens detectors. The in-lens detector gives information on the surface of the nanowire, it is unable to discern the core-shell structure. The difference in contrast and surface sensitivity is primarily due to the difference in energies of the SE reaching the detectors. It is postulated that the lower energy SE generated from the incident electron beam (type- I) make up the in-lens image, while only higher energy type-II electrons generate images from the SE2 detector.^[9]

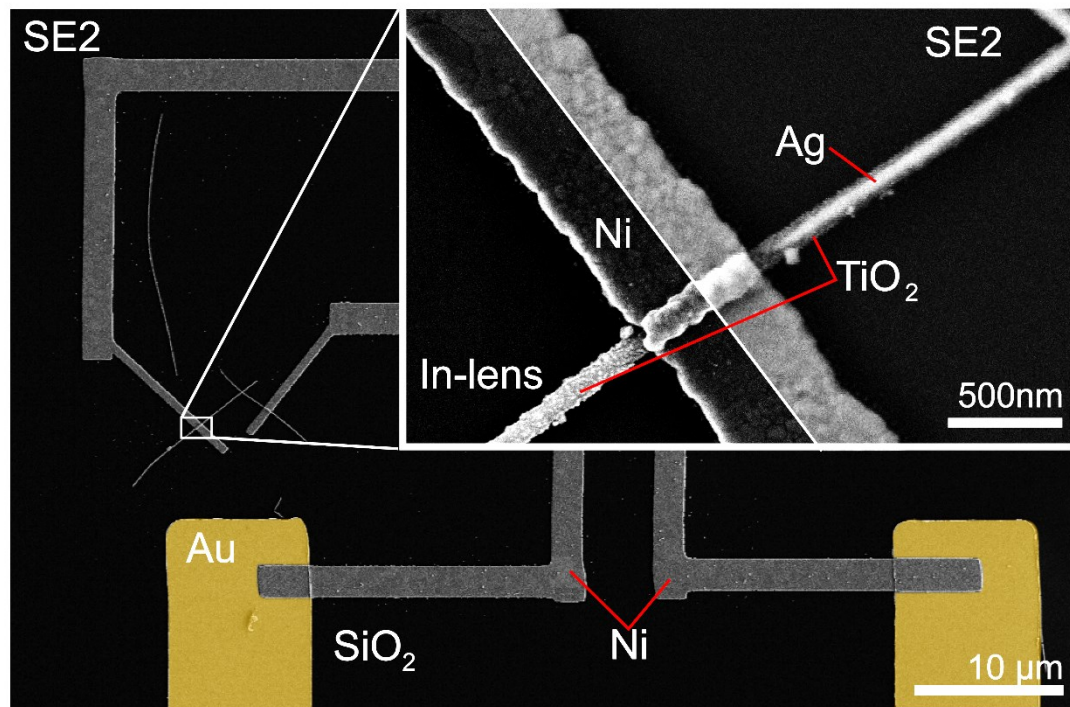


FIGURE 2.2. False-colour SEM image illustrating the differences between the two electron detectors. Main image, secondary electron micrograph of Au and Ni electrodes on a SiO₂ substrate. Inset is a high magnification composite image of the nanowire / electrode interface using both the in-lens (left) and SE2 (right) detector. The surface sensitivity of the in-lens detector is clearly visible. The SE2 material contrast allows for the co-axial nature of the wire to be distinguished. Both images were taken using an accelerating voltage of 5 kV.

2.1.1.2 Energy Dispersive X-ray Spectroscopy

Energy dispersive x-ray (EDX) spectroscopy is a chemical microanalysis technique used in combination with a SEM. When a material is bombarded with an electron beam it produces two kinds of x-rays. *Bremsstrahlung* radiation is the continuum of x-rays which are produced when incident beam electrons are slowed to varying degrees by the strong electromagnetic field of atomic nuclei in the sample.^[10] The second, and more quantitatively useful radiation are known as the *characteristic x-rays*. Incident beam electrons can knock a small fraction of electrons from inner-shell orbitals of the sample atoms, in a process called *inner-shell ionisation*. The inner-shell vacancies are filled by outer-shell electrons, this recombination emits a characteristic x-ray. Characteristic x-rays are referred to by either the IUPAC system or by Siegbahn notation.^[11, 12]

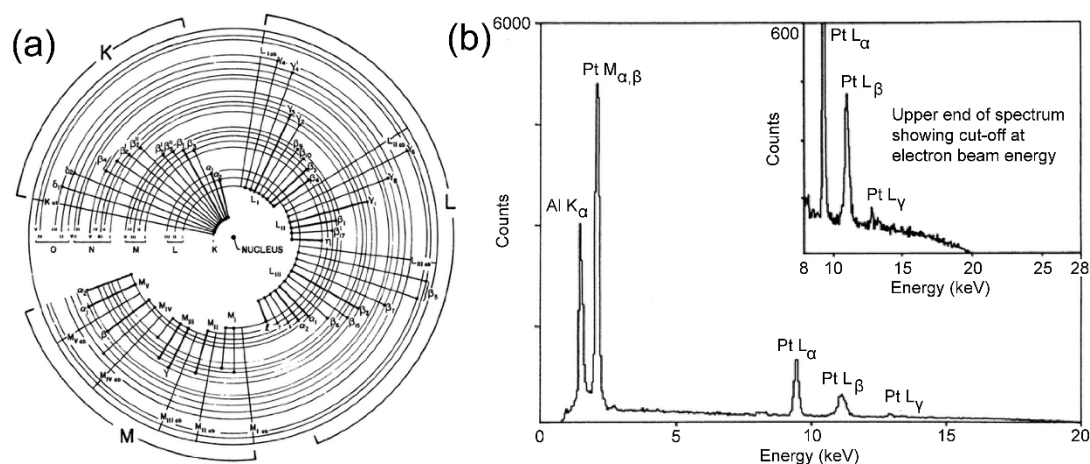


FIGURE 2.3. (a) The origin of the fine structure in characteristic x-ray spectra produced by electron bombardment. (b) EDX spectrum from Pt on Al_2O_3 bombarded by 20 keV electrons. The characteristic lines of both Al and Pt are visible but not O, as the O K_α line is located at 0.525 keV, which is below the soft cut off. The inset shows the tail end of the spectrum and the gradual decay of the Bremsstrahlung background up to 20 keV. Adapted from Watt et al.^[7]

Siegbahn notation is used in this work, meaning the radiation produced as a K-shell hole is filled by an L-shell electron is deemed the K_α line. Figure 2.3(a) shows the origin of the fine structure in characteristic x-ray spectra, incident electrons which are not energetic enough to excite K radiation may still have sufficient energy to excite L or M radiation. Figure 2.3(b) shows a spectrum for Pt on Al_2O_3 using an accelerating voltage of 20 keV, the count of x-ray detection against x-ray energy is plotted in the graph. The ionisation of core electrons requires a critical threshold energy to be attained, therefore, suitable accelerating voltages must be chosen which correspond to the desired element's *excitation potential*. For the most efficient x-ray generation, the energy of the incident beam should be 3-4 times that of the desired line. A soft cut off at low x-ray energy (below 1 keV) also exists, where the x-rays are absorbed before reaching the detector.

EDX performed inside a SEM requires a thick sample, this is because the characteristic x-rays are generated deep within the material. At nanoscale thicknesses EDX may be unable to provide quantitative analysis, as substrate signals will become dominant. For these types of samples, EDX analysis performed inside a TEM may be more suitable and give quantitative elemental analysis, additionally, much higher accelerating voltages (300 keV) are available.

2.1.2 Electron-Beam Lithography

As mentioned at the beginning of this chapter, electron-beam microscopes can also be adapted for the fabrication of nanostructures. This practice dates back over 50 years when in 1961 Mollenstedt and Speidel first demonstrated the use of what is today termed ‘electron-beam lithography’ (EBL).^[13] This came just over a year after Richard Feynman delivered his seminal lecture entitled ‘There’s Plenty of Room at the Bottom’. Only 15 years later sub-10-nm features were patterned.^[14] In recent years, high-resolution EBL has become accessible outside of the semiconductor industry. Indeed, interest in EBL has reached far beyond the semiconductor industry to an interdisciplinary field consisting of engineering, biology, physics, chemistry and advanced materials.

All EBL performed in this study was carried out using a Carl Zeiss Supra 40 SEM with a field emission source and a Raith Elphy Plus attachment. The processes involved in EBL are schematically illustrated in Figure 2.4. EBL involves spin coating a substrate with a thin electron-sensitive resist layer. The solubility of the resist is modified when exposed to an electron beam delivering the appropriate amount of charge per area ($\mu\text{C}/\text{cm}^2$), known as the clearing dose. Subsequently, it is susceptible to removal in a suitable developer. EBL is classified as a direct-write serial lithography technique; meaning it does not require a hard mask, but rather, an electron beam rasters over the surface in the pattern designed by the user. This flexibility allows for sample specific patterning, critical to the fabrication of contacts to randomly deposited nanowires. The beam is controlled by proprietary software (Raith GmbH) which has an inbuilt computer aided design (CAD) element for drawing patterns. The software also controls the beam blanker which directs the beam away from the sample at high speed (2.5 MHz) and allows for step sizes amenable to the exposure of nanoscale features.

In 1975, Michael Hatzakis discovered that the common polymer poly(methyl methacrylate) (PMMA) was an e-beam sensitive resist.^[15] Subsequent to this, many different electron-sensitive resists have been developed in the form of positive-or negative-tone resists. Positive-tone resists become soluble in the developer and are therefore removed where the area has been exposed to the e-beam. Negative-tone resists work to the opposite effect, whereby, upon e-beam exposure the resist becomes

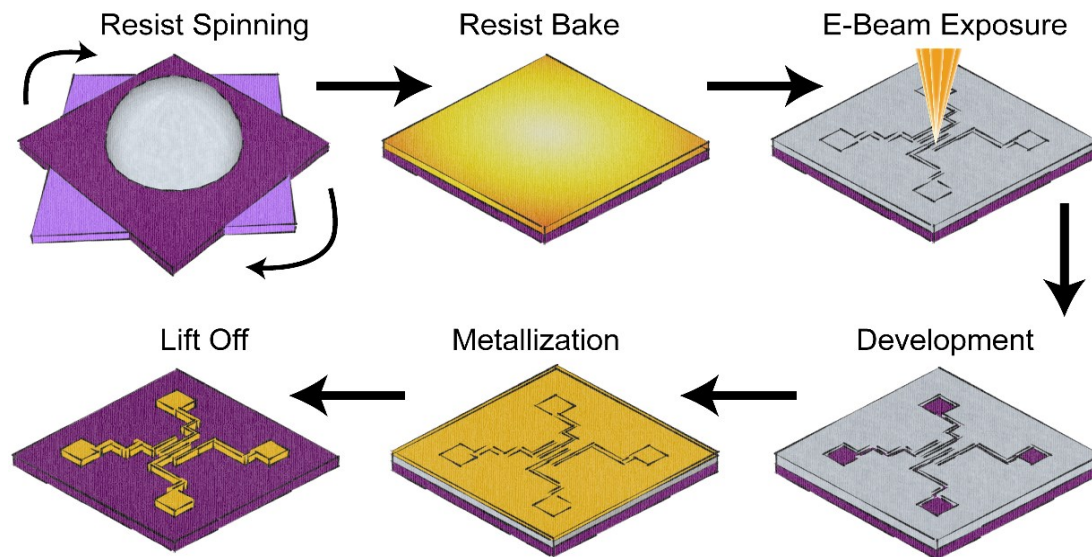


FIGURE 2.4. Electron beam lithography process work flow, resists are spun onto clean substrates and subsequently baked. Following e-beam exposure the sample is developed in a suitable developer. The surface is then coated in a thin layer of metal, which adheres to the surface through the openings in the resist. Superfluous metal is removed using a lift-off step in acetone, revealing the final metal features on the substrate.

less soluble and hence only written areas of the resist remain once developed. PMMA and poly(methyl methacrylate – methacrylic acid) (MMA) are two of the most common positive resists and are used throughout this work. The chemical processes which govern the solubility of a resist are bond-breaking and polymerisation of crosslinking hydrocarbon chains. In the case of PMMA, bond-breaking primarily occurs with e-beam exposure (however with extremely large e-beam doses polymerisation can occur), this is due to the relatively weak carbon-carbon and carbon-hydrogen bonds, which increases solubility in a suitable developer.^[16] Hydrogen silsesquioxane (HSQ) is a negative tone resist. Exposure to the e-beam causes polymerisation via cross-linking of the polymer chains, reducing solubility.

EBL relies on irradiating the thin-film of electron sensitive resist, it is therefore important to understand the interactions of the e-beam and the sample. Figure 2.5 highlights the importance of choosing suitable accelerating voltages. Shown in this figure are Monte-Carlo simulations of interaction trajectories between an incident electron beam and the PMMA/MMA/SiO₂/Si sample at various accelerating voltages generated using the CASINO simulation software.^[17] At low accelerating voltages, like 2.5 keV the beam does not possess enough energy to fully penetrate the first layer

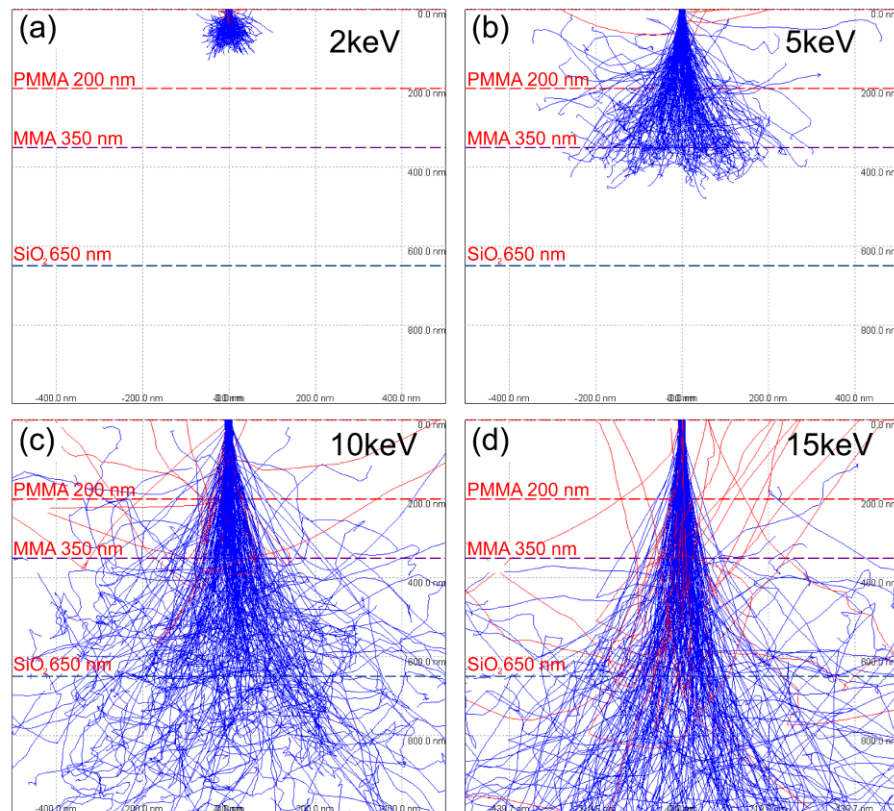


FIGURE 2.5. Monte-Carlo simulations of interaction trajectories between the incident electron beam and the specimen at various acceleration voltages: (a) 2 keV, (b) 5 keV, (c) 10 keV and (d) 15 keV. The sample is a PMMA (200 nm) / MMA (150 nm) / SiO₂ (300 nm) / Si stack. Simulations were generated using the CASINO software. Blue lines represent primary electrons, with red lines representing back scattered electrons.^[17]

of PMMA resist (Figure 2.5(a)). Forward scattered electrons can broaden the beam profile within the resist due to small angle scattering events. Beam profile widening causes an undercut resist profile which aids in subsequent metallisation and lift-off steps. Figure 2.5(b) shows how 5 keV beam energies are sufficient to penetrate the resist but cause too much forward scattering and beam profile widening. At 10 keV and 15 keV accelerating voltages the beam broadening is most appropriate (Figure 2.5(c-d)).

As with conventional SEM the apertures and accelerating voltages dictate the beam current. Higher beam currents allow for shorter beam dwell times which speed up production, however this reduces the maximum attainable resolution. Suitable accelerating voltages and aperture sizes must be chosen for the desired features. These will be further discussed in section 2.2.3

2.1.3 Transmission Electron Microscopy

In a conventional optical slide projector, a light source is manipulated into a parallel beam by a condenser lens and made pass through the slide, it is then focused and enlarged into an image on the screen by the objective lens. In a TEM the light source is replaced by an electron source and the glass lenses are replaced by magnetic lenses. A fluorescent screen is used, which emits light when struck by electrons, or, more commonly in modern microscopes, an electronic sensor typically known as a charge-coupled device (CCD) camera. The whole trajectory from the source of the e-beam to the screen is under UHV.

As the name suggests TEM relies on the transmission of electrons through a sample. Detectors on the opposite side of the specimen collect the transmitted electrons which gives information about the specimen. To allow this to occur, TEM samples must be ultra-thin, typically less than 100 nm and samples must be placed on an electron-transparent holder, known as a TEM grid. For the purposes of this work, nanowires which already satisfy thickness requirements need only be dropcast from solution onto lacey carbon grids to allow for TEM imaging.

As the TEM images are constructed from the electron signal which passes through the sample the ultimate resolution depends on several factors. Typical accelerating voltages of 80 – 300 keV are used, it is worth noting that in a conventional TEM, the ultimate resolution is not limited by this accelerating voltage but spherical aberration. Chromatic aberration can be minimised by using very thin samples and keeping a stable accelerating voltage. Astigmatism can be corrected by using variable electromagnetic compensation coils, like a beam inside a SEM. Depending on the TEM, STEM and EDX capabilities may also be available. Selected area (electron) diffraction (SAD) mode may also be engaged which allows the operator to characterise crystalline samples. The TEM used in this study is an FEI Titan Microscope operated by Dr Eoin McCarthy.

2.2 General Nanowire Device Fabrication

The fabrication of electrical contacts to nanowires requires a complex, multi-step process generally referred to as mix-and-match lithography. Mix-and-match lithography is a combination of lower resolution high throughput ultraviolet (UV) lithography, for defining larger (mm to μm) features, and EBL for when high-resolution lithography and alignment is critical, such as defining electrical contacts to individual nanowires. The following section will outline the materials and steps required for general device fabrication, while details specific to each wire type will be discussed in later chapters.

2.2.1 Dicing

Dicing saws are precision instruments which cut semiconductor wafers into individual chips or dies; this technology is crucial in the semiconductor, electronic and optical component industries. Wafers are held to the chuck-table by a vacuum and partially cut by a high-speed rotating blade. Si wafers with 1 μm of thermally grown SiO_2 were used as substrates for sample preparation unless otherwise stated. 100 mm wafers were coated with a sacrificial resist (S1813) and cut into 2.2 cm^2 tabs by a DAD3220 – Disco Automatic Dicing Saw. The 1-2 μm UV sensitive photo resist protects the surface from Si cutting debris which can penetrate the underlying structure. The resist layer and the particles are easily removed by an acetone bath and sonication post-cutting. Dicing substrates as opposed to cleaving them gives greater edge uniformity and prevents rough edge pieces from chipping and subsequently damaging the UV mask, the contact vacuum membrane, and/or obstructing the levelling procedure.

2.2.2 UV Lithography

The cornerstone of many electronic, semiconductor and optical processes is the well-developed parallel writing method of UV lithography. Using the photons from a 365 nm mercury vapour discharge lamp a photosensitive layer known as the resist, is exposed through a photomask. UV masks were designed using CleWin 5^[18] and written to a chromium coated fused-quartz mask by Delta Mask.^[19] The photosensitive resist used for all UV lithography in this work is the positive-tone, novolac-type resist

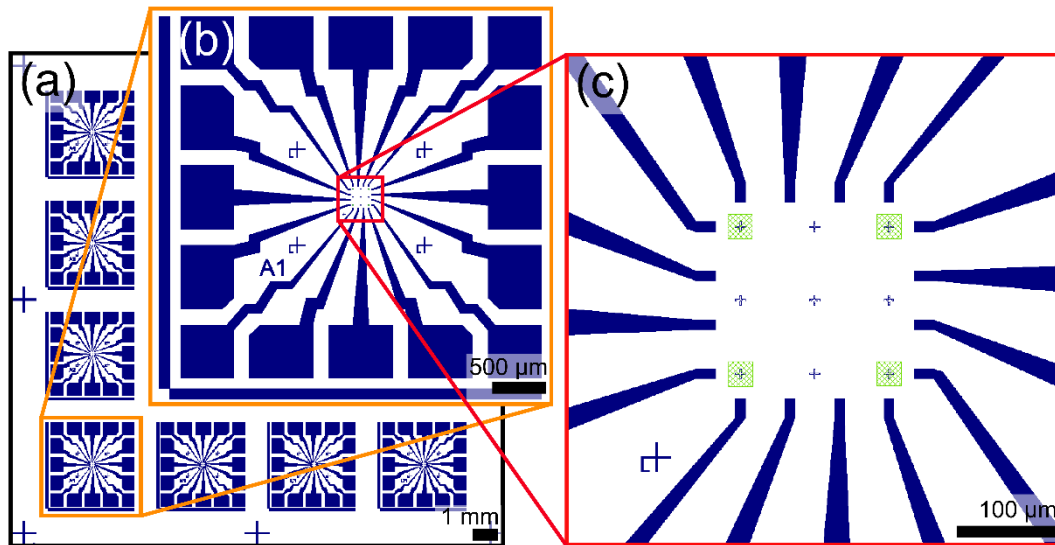


FIGURE 2.6. Schematic of the photolithographic ‘Cryomask’ for mix-and-match lithography. (a) Full chip design comprising of a 4 x 4 individual device array. (b) Close-up of a single device area with identification marker and sixteen perimeter pads for making electrical contact. (c) Further magnification of the ‘working area’, with alignment markers for EBL highlighted by the green squares.

S1813. Novolacs are phenol-formaldehyde resins, they are soluble in aqueous and basic media. Mixed with this is diazonaphthoquinone (DNQ) which is insoluble in those media. Upon exposure to UV light, a photo-induced reaction occurs increasing the solubility of the resist in a suitable developer.

Figure 2.6 shows an image of the ‘Cryomask’ design under various magnifications. The mask consists of a 4 x 4 array of device areas (Figure 2.6(a)), each containing sixteen large 600 x 500 μm perimeter contact pads, this can be seen in Figure 2.6(b). The large pads are used for electrical contacting by the microprobers of the electrical system and may also be contacted by wire bonding. Crosses can be seen in the 200 x 200 μm working area of the chip in Figure 2.6(c), these serve as alignment markers for subsequent EBL steps. Figure 2.7 shows the alternate mask design used in this work, the ‘Tarek mask’. This design features a higher density of devices when compared to the Cryomask, it is however limited to four contacts per working area. Figure 2.7(a) shows an image of the 6 x 6 array of device areas. Each contain a 2 x 2 array of 250 μm square pads used for electrical contacting (Figure 2.7(b)). Figure 2.7(c) shows an optical image of the working area which includes EBL alignment markers.

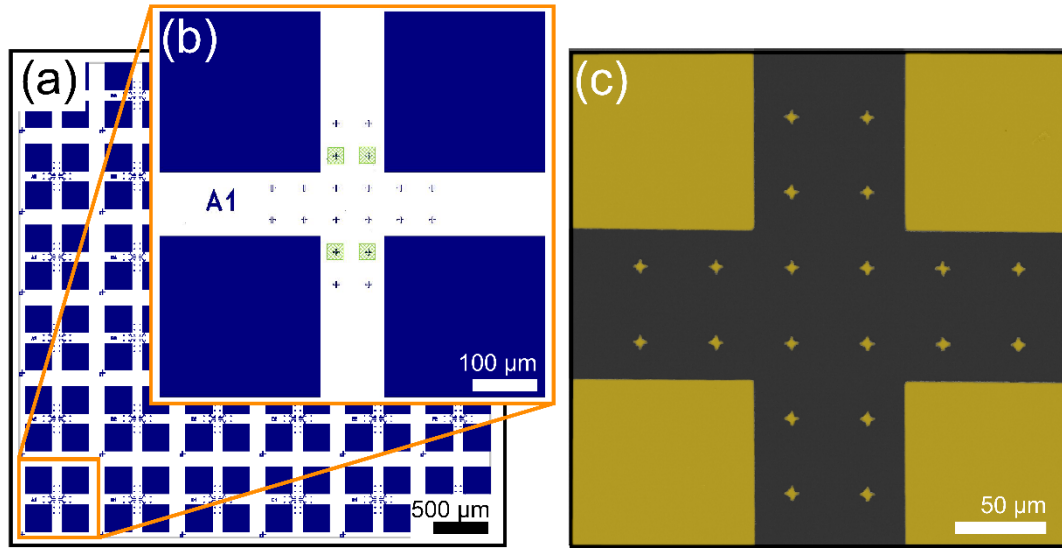


FIGURE 2.7. Schematic of the photolithographic ‘Tarek mask’ for mix-and-match lithography. (a) Full chip design comprising of 6 x 6 individual device array. (b) Close-up of a single device area with identification marker and four large pads for making electrical contact. (c) False coloured SEM image of Au contact pads on SiO₂ substrate.

Diced 2.2 x 2.2 cm substrates were cleaned by sonication in acetone for 5 minutes, followed by sonication in isopropyl alcohol (IPA) for a further 5 minutes and dried under a stream of N₂ gas. Substrate preparation is intended to aid in the adhesion of the photoresist material to the SiO₂ substrate. Clean substrates first undergo a dehydration bake at 150 °C for 2 minutes to remove volatilizing organic contaminants. Microposit S1813 (Shipley) positive photo-resist was spun onto the substrates, baked to remove solvent on a hotplate and subsequently processed as per the protocol set out in Table 2.1 below.

TABLE 2.1. UV Lithography Protocol.

UV lithography recipe
1. Spin S1813 resist at 5000 rpm for 45 s, with 5 s ramp at 500 rpm.
2. Soft bake on hotplate at 115 °C for 75 s.
3. Expose to 365 nm for 5.5 s (dose = 66 mJ cm ⁻²).
4. Develop in MF319 (Shipley) for 45 s, stop in deionised H ₂ O.

The thickness of the S1813 film depends on the speed at which the resist is spin-coated, 5000 rpm results in a resist thickness of 1.2 μm .^[20] After chemical development, a thin-film of Ti-Au (5 nm-25 nm) was deposited onto the sample by electron beam evaporation using a Temescal FC-2000, where Ti is used as an adhesion layer between the gold layer and the SiO_2 substrate. The metallised sample is then placed into an acetone bath to remove the remaining resist and allow the superfluous metal to lift-off. The time for lift-off is dependent on the success of the UV lithography, but was typically left overnight. Several factors can affect the outcome of the photo lithographic process. Variation in beam intensity, sample or substrate holder tilt as well as poor mask, substrate or contact vacuum can result in regions of under or overexposure. To avoid these occurring, and verify processing conditions, a test exposure is performed on one sample prior to the main run.

2.2.3 Electron Beam Lithography

After UV lithography, EBL was used to contact individual nanowires. EBL was also used to expose regions in an e-beam sensitive resist to spray deposit nanomaterials into, further details on the spray deposition method will be given in section 2.3.1 Optical microscopy was used to identify and photograph suitable nanowires for contacting. These nanowires were free from debris fields, somewhat isolated, and within the working area of 500 x 500 μm . ImageOverlayUtility^[21] was used to overlay a semi-transparent version of the optical images on top of the Raith software. Using UV defined contacts and alignment markers as reference points, EBL patterns for the electrical contacts connecting the nanowire to the predefined UV contacts were drawn.

To facilitate easier metal lift-off, a bilayer e-beam resist was used for all EBL carried out in this work (Figure 2.8(a)). A bilayer resist causes a much more pronounced undercut profile which prevents metal adhering to the resist walls and creating ‘rabbit ears’ on the desired features. Poly(methyl methacrylate – methacrylic acid (8.5 %)) (MMA) in ethyl lactate is used as a bottom layer with poly(methyl methacrylate) (PMMA) in anisole used as the top layer of the bilayer configuration. Figure 2.8(b) shows a SEM image of a sample post exposure and development, with the undercut resist profile visible, AFM analysis, carried out by Dr Shaun Mills shows the thickness of the bilayer resist to be 400 ± 3 nm.

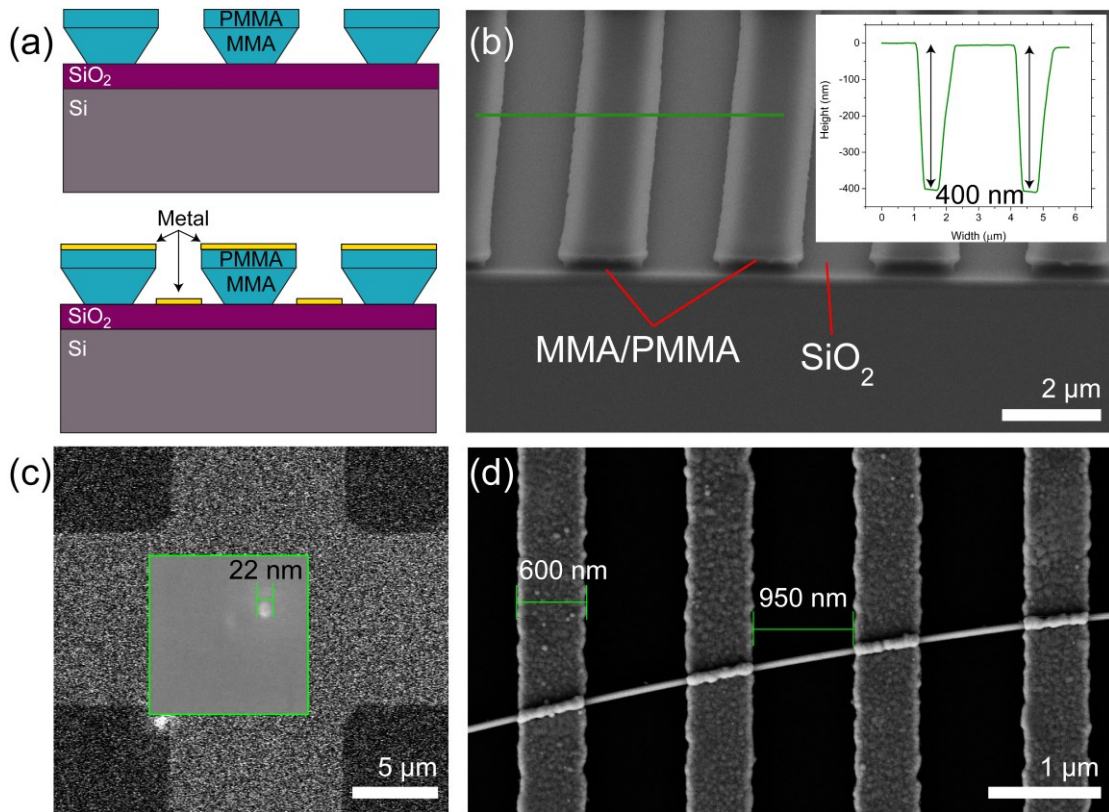


FIGURE 2.8. (a) Bilayer resist schematic after development (above) and metal deposition (below). (b) SEM image of PMMA/MMA bilayer resist profile, inset shows the height profile measured by AFM along the green line, which spans across two trenches. (c) Carbon contamination spot with a diameter of 22 nm confirms good alignment and focus of the e-beam. (d) SEM image of a single nanowire contacted with four EBL defined electrodes, the electrodes are 600 nm in width with 950 nm between each.

Key to high resolution EBL is a correctly focused and stigmated beam on the surface, this results in a sharp circular beam spot, which when left to dwell on the surface causes build-up of a carbon contamination spot, this can be seen in Figure 2.8(c). Figure 2.8(d) shows EBL fabricated contacts onto an individual Ag nanowire.

Prior to aligning, the beam current is measured by focusing the beam onto a Faraday cup located on the sample holder. Larger beam currents require shorter dwell times, but are not suitable for realising high resolution features. There is a trade-off between resolution size and exposure time which needs to be considered and chosen accordingly. Successful exposure of the EBL design requires careful alignment between the sample and the Raith design, this is done in three alignment procedures before exposure.

First is compensating for the rotation of the sample, this is done by taking a long straight edge feature on the sample and marking two points which are separated by as far a distance as possible. The second procedure involves driving to a known area of the sample where final beam alignment is made, and setting the co-ordinates of the current beam position in the Raith software. Finally, a ‘layer 63’ alignment is run, where a manual alignment is made to small predefined alignment crosses close to the write area. These alignment crosses can be seen in green boxes of Figure 2.6(c) and Figure 2.7(b). The Raith software then exposes the design.

As previously mentioned the magnitude of the beam current depends on the accelerating voltage and aperture size, it is therefore necessary to use beam voltages and aperture sizes specific to the scale of the features desired. These parameters are outlined in the recipe found in Table 2.2.

TABLE 2.2. EBL Bi-Layer Resist Protocol.

Bi-layer resist recipe.		
1. Spin MMA EL9 at 6000 rpm for 45 s, with 5 s ramp at 500 rpm.		
2. Soft bake on hotplate at 180 °C for 120 s.		
3. Spin PMMA 495 K A3 at 3000 rpm for 45 s, with 5 s ramp at 500 rpm.		
4. Soft bake on hotplate at 180 °C for 180 s.		
5. Electron exposure using the following settings.		
• Feature Size	Small (nm)	Large (µm)
○ Accelerating voltage:	10 kV	15 kV
○ Aperture size:	20 µm	60 µm
○ High Current	Disabled	Enabled
○ Beam Current	90 pA	900 pA
○ Clearing dose:	120 µC cm ⁻²	
6. Develop in MIBK : IPA (1 : 3) for 50 s, stop in IPA.		

For small features, such as electrical contacts to nanowires, the lower accelerating voltage of 10 kV and an aperture size of 20 µm was used. For larger areas, higher accelerating voltages and larger aperture sizes were chosen, along with the option for high current. High current mode increases the probe current by a stronger activation

of the condenser lens. It is typically used in analytical applications such as EDX, but has the advantage of effectively doubling the beam current for EBL, reducing exposure times. When used in imaging mode, high current can also give a better depth of field.^[22] After exposure, the sample is developed in a methyl isobutyl ketone (MIBK) and IPA mixture of ratio 3:1 for 50 s, after which it is washed in IPA and dried under a N₂ stream.

2.3 Nanowire Network Fabrication

In this section, the techniques used to fabricate nanowire networks are outlined. A discussion on the development of this technique into a general and self-assembly style process based on surface adhesion effects will be presented in chapter 4.

2.3.1 Spray Deposition

The ability to finely control the placement of nanomaterials for study and device fabrication would have a dramatic effect on the incorporation of nanomaterials into useable devices. Realizing structures which include nano and macro elements demands the controlled placement of nanomaterial features on the surface of solid and flexible substrates. This has traditionally been achieved either by in-situ growth, or post-fabrication patterning and deposition. In-situ growth being impossible for solution synthesized nanomaterials and ordinarily requiring high temperatures which are not compatible with soft substrates. Solution-based deposition techniques are typically simple, low-cost and relatively easy to scale up. Current solution based post-fabrication deposition methods include inkjet printing,^[23-25] template directed self-assembly,^[26] micro and nano contact printing methods,^[27, 28] as well as drop-casting,^[29] spin,^[30] slot-die,^[31] and spray coating.^[32, 33]

Spray deposition is a simple, scalable technique where solution based dispersions of nanomaterials are sprayed onto a surface. In this work a modified artists spray gun is used, an annotated image of which can be seen in Figure 2.9(a) (Infinity model, Harder & Steenbeck).^[34] The dispersion which is typically in a volatile solvent is put into the solution reservoir. The solution is atomized into micro-sized droplets when forced by a large N₂ backing pressure (50 psi)^[32] through the small aperture created by the needle and the top of the gun (Figure 2.9(b)). The gun is held 8-10 cm

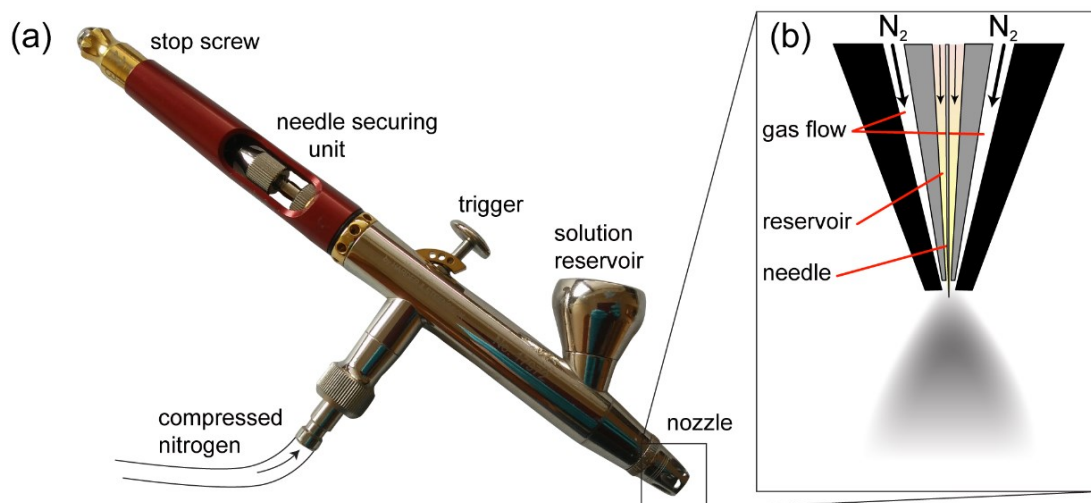


FIGURE 2.9. (a) Annotated image of the Harder and Steenbeck spray gun used to spray deposit nanomaterials. (b) Schematic of spray nozzle mechanism.

from the target substrate and the impinging droplets evaporate immediately upon impact preventing solvent drying effects such as coffee staining or aggregation of the nanomaterial.

2.4 Characterisation of Nanowire Devices

The section will focus on the direct current (DC) electrical characterisation of nanowire materials. Each type of low-level electrical measurement is subject to different types of error sources, these will be discussed, as well as the equipment and methods used.

2.4.1 DC Electrical Measurements

Many applications require the ability to measure extremely low currents, such as nanoamps or less. The electrical characterisation system used in this work is a Keithley 4200 ‘Semiconductor Characterisation System’ (SCS), this is a fully integrated unit which is completely configurable to user specifications. The specific unit used in this work contains four source measure units (SMUs), two of which are installed with current pre-amplifiers. Two high powered pulse measure units (PMUs). A capacitance-voltage unit (CVU) for alternating current (AC) measurements and two remote pre-amplifiers (RPMS). A computer running windows and the Keithley proprietary software is also inside the unit.

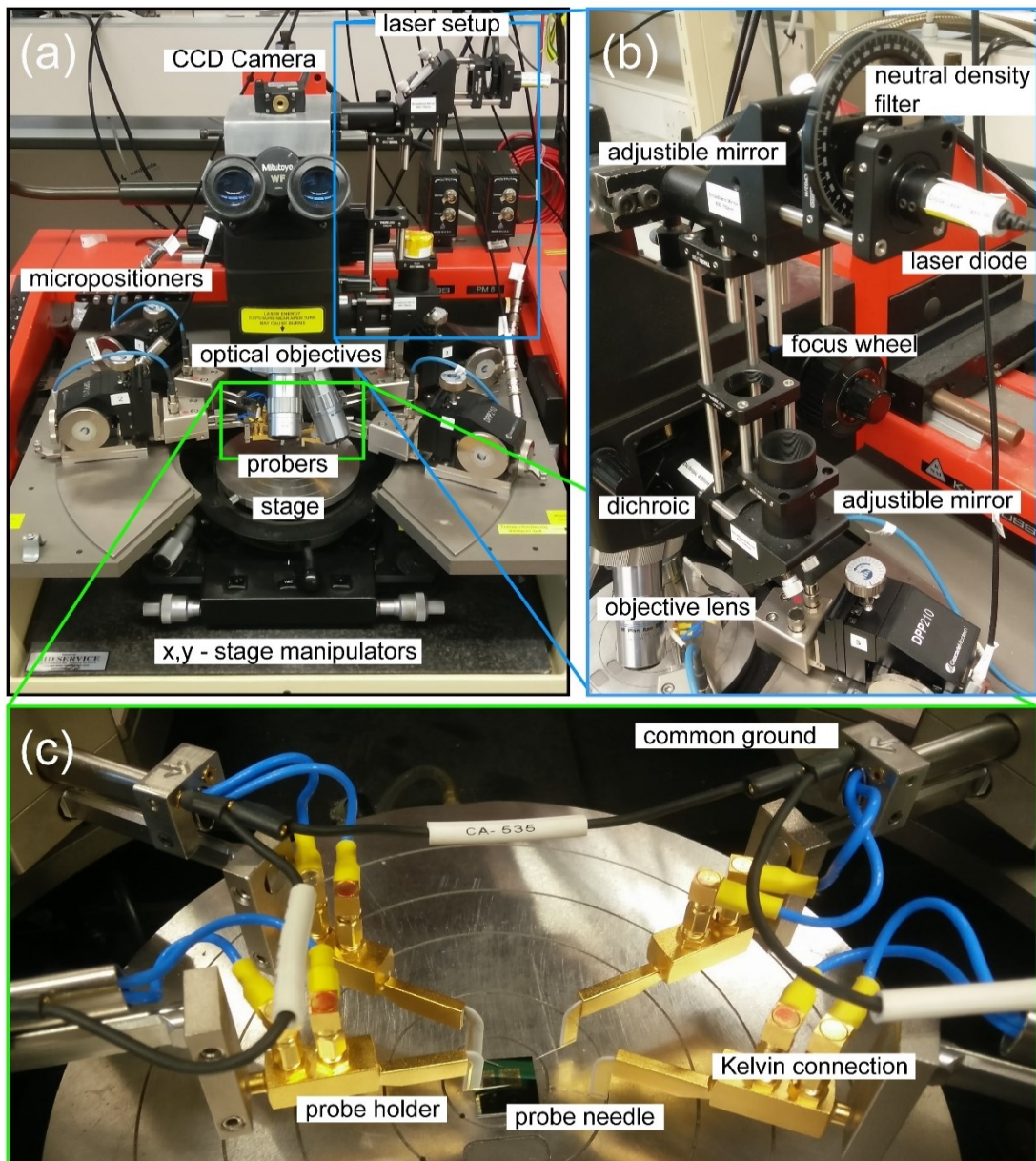


FIGURE 2.10. Electrical characterisation system, with optical attachment. (a) Front view of the Carl Suss PM-8 probe table with optical microscope, Cascade micro-positioners and laser set up. (b) Laser attachment set up with 405 nm 5 mW laser, neutral density filter and adjustable mirrors. (c) Magnified image of the tips of the cascade micro-positioners. A shielded Kelvin connection is in place up until the probe needle which makes contact to the electrical contact pads on the sample. All guards are held at a common ground.

The SMU terminals are connected to micro-positioners which are magnetically mounted to a Carl Suss PM-8 probe table using low noise triaxial (triax) cables, as seen in Figure 2.10(a). Triax cables contain a centre conductor (HI), an inner shield (LO or GUARD) and an outer shield (chassis ground or LO). This arrangement allows the cable to carry two signals, neither of which is at ground potential, while ensuring

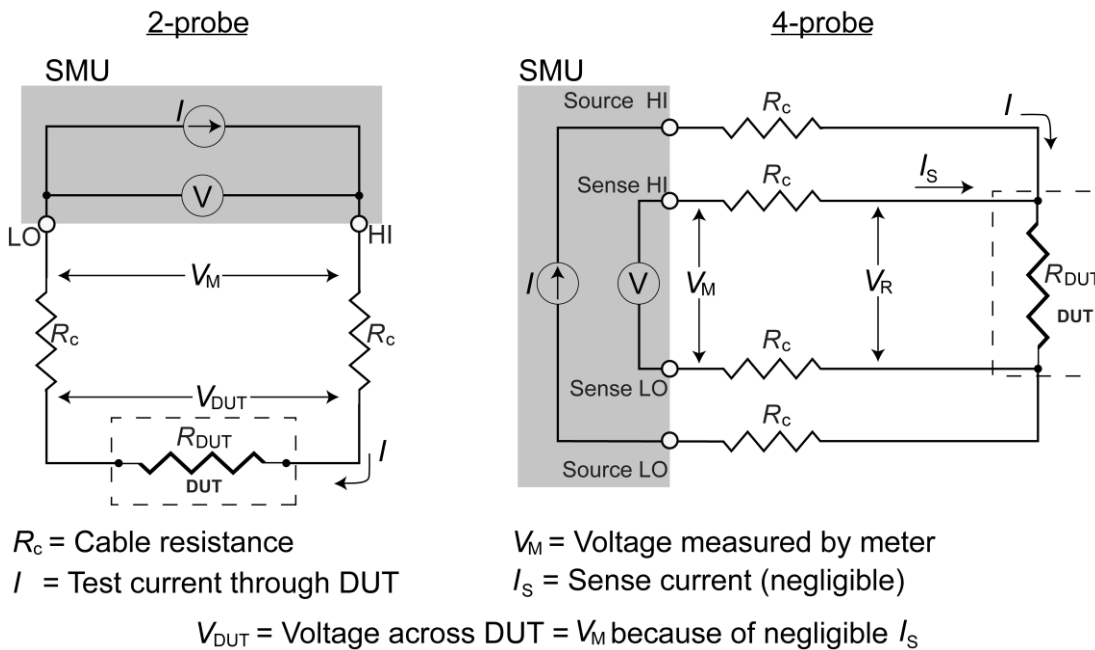


FIGURE 2.11. Equivalent circuits for both two-point and four-point measurement set ups.

high impedance integrity by shielding both leads and maintaining a high resistance between each conductor and ground. When using a SMU to measure low current, the guard terminal reduces leakage current of the cable and test fixturing. The optical turret of the probe station contains a laser set up (Figure 2.10(b)), this will be discussed in section 2.4.2 Figure 2.10(c) is an optical image of the micro-positioner (Cascade Microtech) and the tungsten micro-needle (DPP210) probes above a device under test (DUT).

Typical DC measurements are made using a two-probe set up, this uses a single SMU to source either current or voltage across a sample and then read the corresponding current or voltage after it has passed through the test circuit. To determine the resistance, Ohm's law is used where $R=V/I$, R is the resistance, V is the voltage and I is the current. For high impedance samples where the resistance of the device under test (R_{DUT}) is much greater than the lead and contact resistance, this type of measurement can provide accurate results. However, for low impedance samples, or where subsequent analysis relies on the exact measurement of R_{DUT} , the contact and lead resistance can have an appreciable contribution to the overall measured resistance. A solution to the problem of two-point measurements is the four-wire or 'Kelvin' measurement. In the Kelvin measurement, a second pair of probes are used for

sensing. Negligible current flows through the inner sense probes and therefore, only the voltage drop across the DUT is measured. The equivalent circuits for two-probe and four-probe can be seen in Figure 2.11. Material properties such as resistivity, ρ may then be calculated per,

$$\rho = \frac{RA}{d} \quad (2-1)$$

Where R is the measured resistance, A is the cross sectional area, and d is the distance from the outer edges of the inner contacts.^[35] For thin-films and nanowire networks the measured four-probe resistance is known as the sheet resistance (R_s) with units of Ω/\square .

2.4.2 Laser Setup

For real-time electrical monitoring of a materials photo-response the Karl Suss PM-8 optical turret was modified during the work of Dr O'Kelly.^[36] This resulted in a laser setup as shown in Figure 2.10(b), consisting of a CCD camera, a 405 nm wavelength 4.5 mW laser. A neutral density filter for controlling laser power and two adjustable mirrors for focusing the elliptical beam spot shape are also included in the set-up. The laser could be focused to 470-490 nm full width half maximum (FWHM) spot size using the Mitutoyo brand 50x microscope objective. A physical optical shutter can be placed between the adjustable mirrors and can be controlled by a shutter controller receiving a trigger from the Keithley 4200-SCS. This allows for synchronised voltage and optical stimuli to be applied to the DUT. This set up will be used in quantifying the learning and memory behaviours of single TiO₂ nanowires when subjected to singular and coincident voltage and optical stimuli in chapter 5.

2.5 Nanowire Network Simulation

To fully understand the conduction properties of nanowire networks, computer simulations were employed to deconvolute the various parameters which govern the flow of charge through the network. These fundamental parameters, such as, interwire contact resistance (R_{jxn}) and inner-wire resistance are key for matching experiment and simulation. A deeper discussion into the simulation of metallic nanowire networks will be provided in chapter 4.

Exploiting the ultimate performance of nanowire systems requires a robust predictive model to define material limits and enable a materials-by-design approach. A model such as this could also be used as a guide for choosing nanowire compositions for specific applications, for example, by visually grading high/low resistance networks for transparent conductor applications. Moreover, the complicated electrical activation process which occurs in a nanowire network can also be simulated. Ultimately, the capacity of a network to connect is determined by the properties of the connecting junctions. Understanding how networks of highly connected objects ‘turn on’ is extremely desirable for telecommunications, the internet of things, neuromorphic and reservoir computing. Work in this thesis has provided direct experimental data to facilitate the building of a predictive computer model for the simulation of the electrical properties of nanowire networks. Experimental models were developed by the Theory and Modelling Group lead by Prof. Mauro Ferreira.

2.6 Conclusion

The operating principles of the many techniques used in this thesis have been described in detail in this chapter. Electron microscopy, which enables fabrication through EBL, imaging through SEM and TEM, and quantitative analysis using EDX. Key to the nanofabrication work undertaken in this study is the mix-and-match lithography techniques required to make electrical contacts to individual nanowires, as well as the spray deposition techniques needed to fabricate isolated self-assembled nanowire networks. The electrical and optical characterisation tools and techniques have also been outlined. In chapter 3, the first experimental chapter, the electrical behaviours of metallic nanowires will be presented. This includes precise electrical measurement of single and crossed metallic nanowires for the simulation of the optoelectronic properties of metallic nanowire networks in chapter 4. The use of a computer model with uses experimentally measured values of the inner wire resistivity, and junction resistance allows for the prediction of the ultimate limit of these materials for transparent conductor application. We present a robust first principles framework for determining and predicting the optoelectronic performances of Ag nanowire networks.

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3

THE ELECTRICAL PROPERTIES OF METALLIC NANOWIRES

This thesis aims to examine the electrical properties of single nanowires with a goal of engineering resistive and memristive behaviours by combining metallic and semiconducting qualities in a single nanowire structure. This chapter will present electrical measurements performed on single metallic nanowires and nanowire junctions, measuring material properties such as *resistivity* (ρ), and the nanowire - nanowire *junction resistance* (R_{jxn}). My original contribution to knowledge in this chapter are the precise measurements on the fundamental electrical properties of Ag, Cu and Cu@Ag nanowires for the development of realistic computational nanowire network models. These models will be used to predict the optoelectrical properties of nanowire networks in chapter 4. Aspects of the work presented in this chapter have been published in *ACS Nano*, *Nanoscale* and *Physical Chemistry Chemical Physics*.

[1-3]

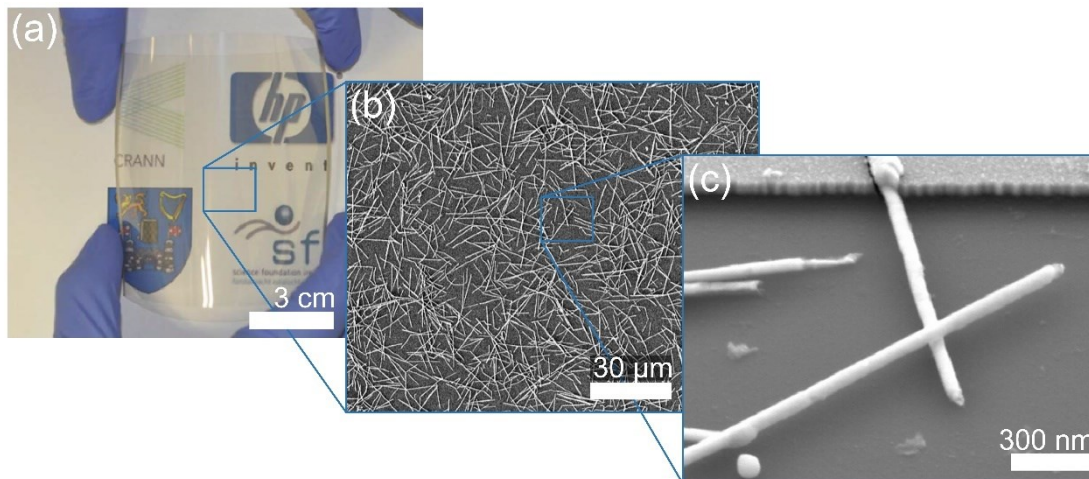


FIGURE 3.1. (a) Ag nanowire network sprayed onto a flexible polyethylene terephthalate (PET) substrate. (b) SEM image of a sprayed Ag nanowire network on SiO₂. (c) Two overlapping Ag nanowires forming a junction.

3.1 Motivation

To correctly predict the electrical and optical properties, a complete understanding of each aspect of the nanowire network is required. Defining optical properties requires knowledge on how the wire length, diameter distribution and density of the network affect the optical transmittance. A number of studies have already determined the relationships between physical, optical and resulting electrical properties.^[4-8] The electrical properties of nanowire networks are ultimately decided by the material resistivity (ρ), the length of the current pathway, the number of connections along that pathway, and the electrical resistance at each of those nanowire junctions (R_{jxn}). It is therefore important to determine R_{jxn} to accurately simulate the electrical properties and calculate the potentiality and performance limits of metallic nanowire networks.

Previous studies have attempted to indirectly determine the R_{jxn} through a combination of experimental and computer simulations. Lee et al. experimentally measured the sheet resistances for Ag nanowire networks of varying densities.^[9] Using experimentally measured nanowire lengths, diameters and nanowire ρ , the group then simulated networks of similar sizes, but varying R_{jxn} . From the fit of theoretical and experimental data they found a range of R_{jxn} values between 1 – 100 Ω . Since no direct measurement of R_{jxn} was made, the values obtained are only estimates. Furthermore, it is not specified whether 2-probe or 4-probe measurements of the network were made; this is important to consider as lead and contact resistances

between mechanical probers and electrical pads would have a significant contribution to such low impedance measurements, and should be avoided when determining accurate values. Another study which indirectly estimates the value of R_{jxn} is the work by Mutiso et al. where junction dominated transport was assumed and the contribution of the nanowire inner resistance was neglected.^[10] Through this approach, they extracted an average effective R_{jxn} of 2 k Ω . Simulations that output the combined material and R_{jxn} contributions are not useful in guiding the atomistic optimisation of these materials. Development of a true materials-by-design approach requires that resistance contributions from the nanowires are separated, as these vary depending on the size of the nanowire and the material of which it is composed.

Both aforementioned studies show that determining R_{jxn} by fitting simulations to experimental R_s values is not the correct approach. A direct electrical measurement of the junction is required, so that this can then be incorporated into a complete nanowire network model. Electrical measurements of a single Ag nanowire junction by the 2-probe method was performed in two further studies.^[11, 12] These however do not provide an accurate measurement of R_{jxn} as they include a series component caused by lead and contact resistance. The 4-probe measurement approach of Hu et al. measured a value of 450 Ω , but only after Au coating of the Ag nanowire junction.^[13] This again is not representative of the contact resistance of bare nanowire-nanowire junctions. The most in depth studies were performed by our group and most recently by Selzer et al.^[1, 14]

TABLE 3.1. Summary of Ag nanowire junction resistance values in the literature.

author	year	R_{jxn} (Ω)	method
Lee et al. ^[9]	2008	1-100	Fitting simulations to experimental R_s values
Mutiso et al. ^[10]	2013	$\sim 2 \times 10^3$	Fitting simulations to experimental R_s values
Song et al. ^[11]	2014	185	2-probe measurement of single junction
Garnett et al. ^[12]	2012	$\sim 1 \times 10^4$	2-probe measurement of single junction
Hu et al. ^[13]	2010	450	4-probe measurement of single junction
Bellew et al. ^[1]	2015	11	4-probe measurement of single junctions
Selzer et al. ^[14]	2016	25.2	4-probe measurement of single junctions

A summary of each of the Ag nanowire R_{jxn} studies can be found in Table 3.1. The work presented in this chapter was carried out in addition to the experiments performed in the 2014 thesis by Dr Bellew,^[15] and subsequently published in *ACS Nano*.^[1] It provides accurate measurements of nanowire ρ and single Ag nanowire junctions subjected to various processing conditions. This seminal work provided the first measured distribution of R_{jxn} values for Ag nanowires, which have since been corroborated by the later work of Selzer et al.^[14] This work is expanded upon by considering other prospective metallic nanowire systems such as Cu and Cu@Ag. Experimental data in this section was also used to simulate Ag nanowire networks which were constructed in silico to match experimental samples, and hence provide a one-to-one comparison^[2] this will be further discussed in chapter 4.

3.1.1 Other Metallic Nanowire Systems: Cu, Cu@Ag

Although Ag nanowire networks appear to be promising substitutes to ITO and have been incorporated into consumer devices,^[16] there are several kinds of stabilisation issues that need to be addressed, including aging and electrical/chemical/thermal stability.^[17-20] Ag nanowire networks can break down due to electromigration and Joule heating at the current carrying junctions, which destroys the connections between nanowires. However, the network is never entirely broken, and can be recovered as observed in the work by Kholid et al.^[21] Ag nanowire chemical stability is most affected by hydrogen sulphide, ozone, chlorine, and hydrogen chloride concentrations.^[22, 23] Post-deposition coating strategies, and capping procedures have also been investigated but these add cost and processing steps.^[7] Cu networks have been considered due to the materials high conductivity, but are also prone to oxidation. In response to these challenges, other metallic nanowire systems have been proposed such as core-shell Cu@X wires, where X= Ag, Au, Pt.^[24] The core-shell structure of the Cu nanowires enables networks to be conductive as printed and protects them from oxidation, solving one of the major disadvantages of raw Cu nanowires relative to Ag nanowires.

3.2 Nanowire Characterisation and Device Fabrication

In this section, the metallic nanowire systems under investigation will be characterised. Also, the methods used to fabricate single and crossed nanowire devices for DC electrical measurements will be outlined.

3.2.1 Ag Nanowires

Ag nanowires used in this work were purchased from Seashell Technology^[25] as a nanowire ink dispersed in isopropyl alcohol (IPA). The as-received ink was diluted to an approximate concentration of 12.5 $\mu\text{g/ml}$. Ag nanowires are typically fabricated using a polyol reduction process. During this reaction, heated ethylene glycol (EG) serves as both the solvent and a precursor to the reducing agent.^[26] During the synthesis process solutions of AgNO_3 and poly(vinyl pyrrolidone) (PVP) in EG are simultaneously added using a two-channel syringe. At a critical concentration of elemental Ag, metallic clusters start to nucleate.^[27] Crucial to the formation of high-yield Ag nanowires is, firstly, the molar ratio between AgNO_3 and the PVP and secondly, the rate of AgNO_3 addition must be sufficiently slow to prevent supersaturation of the reaction media with Ag seeds. With careful control of these conditions, it is possible to lower the chemical potential for growth to the extent that the thermodynamically favourable multiply twinned particles (MTP) grow, rather than the kinetically favoured single-crystal seeds. The twin boundaries on the surface of a MTP are sites of highest energy, which drives the diffusion of Ag atoms toward them. The preferential crystallisation of Ag atoms at the twin boundaries leads to the uniaxial elongation of the MTPs. PVP further facilitates the growth process by preferentially passivating the $\{100\}$ side surfaces of the wire, directing the addition of Ag to the $\{111\}$ faceted ends. The addition of trace amounts of salts to the polyol synthesis has also been shown to influence the morphology, with CuCl - or CuCl_2 mediated polyol process showing excellent results in preferentially growing Ag nanowires.^[28]

Figure 3.2(a) and (b) shows SEM and TEM images of the Ag nanowires. TEM imaging confirms a thin (2 - 5 nm) coating of PVP along the surface of the nanowire. The PVP layer is a consequence of the synthesis process; the nonconducting polymer coating is a barrier for conduction at the nanowire junctions, strategies to connect through this barrier will be discussed in section 3.3.1

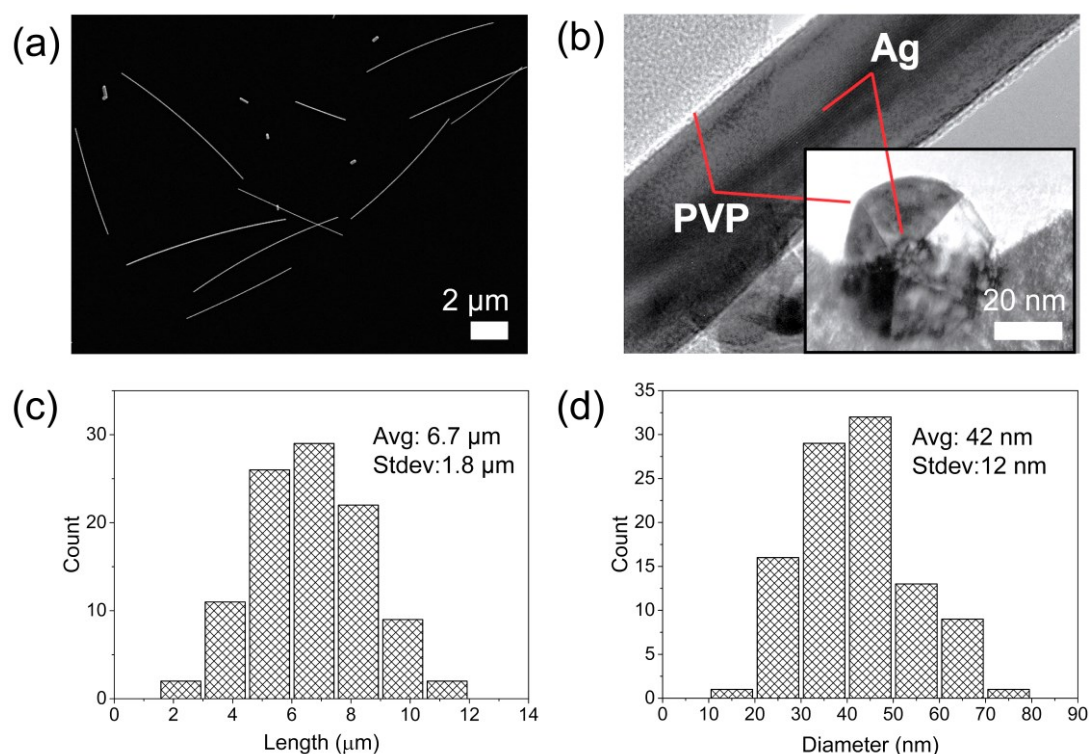


FIGURE 3.2. Characterisation of pentagonally twinned, PVP coated Ag nanowires. (a) SEM image of Ag nanowires dropcast onto a SiO₂ substrate. (b) High resolution TEM image of a Ag nanowire, displaying the thin PVP surface coating, the inset shows a cross-section of a nanowire which demonstrates the pentagonally twinned structure. (c) and (d) display distributions of lengths and diameters respectively of the Ag nanowires used.

The pentagonally twinned structure of the wire is observed in the inset of Figure 3.2(b). Length and diameter distributions generated using SEM and AFM imaging are also given. The nanowires used in this study has an average length of $6.7 \pm 1.8 \mu\text{m}$ and an average diameter of $42 \pm 12 \text{ nm}$ resulting in an average aspect ratio of 160.

3.2.2 Cu Nanowires

Cu nanowires were synthesized in the group lead by Prof. Ben Wiley in Duke University. The synthesis method involves reducing Cu(NO₃)₂ with hydrazine in an aqueous solution containing NaOH and ethylenediamine (EDA), an approach first reported by Zeng and coworkers.^[29] This method was improved in the method described by Rathmell et al.^[30], where the reaction mixture was only heated for a short time (3 mins at 80 °C) to induce a reduction of Cu ions. PVP was then added to the mixture to prevent aggregation. The mixture was quickly cooled in an ice bath which resulted in longer thinner morphologies Cu wires were received in a 5 wt % PVP(10,000 MW), and 1 wt% diethylhydroxylamine (DEHA) dissolved in water, with

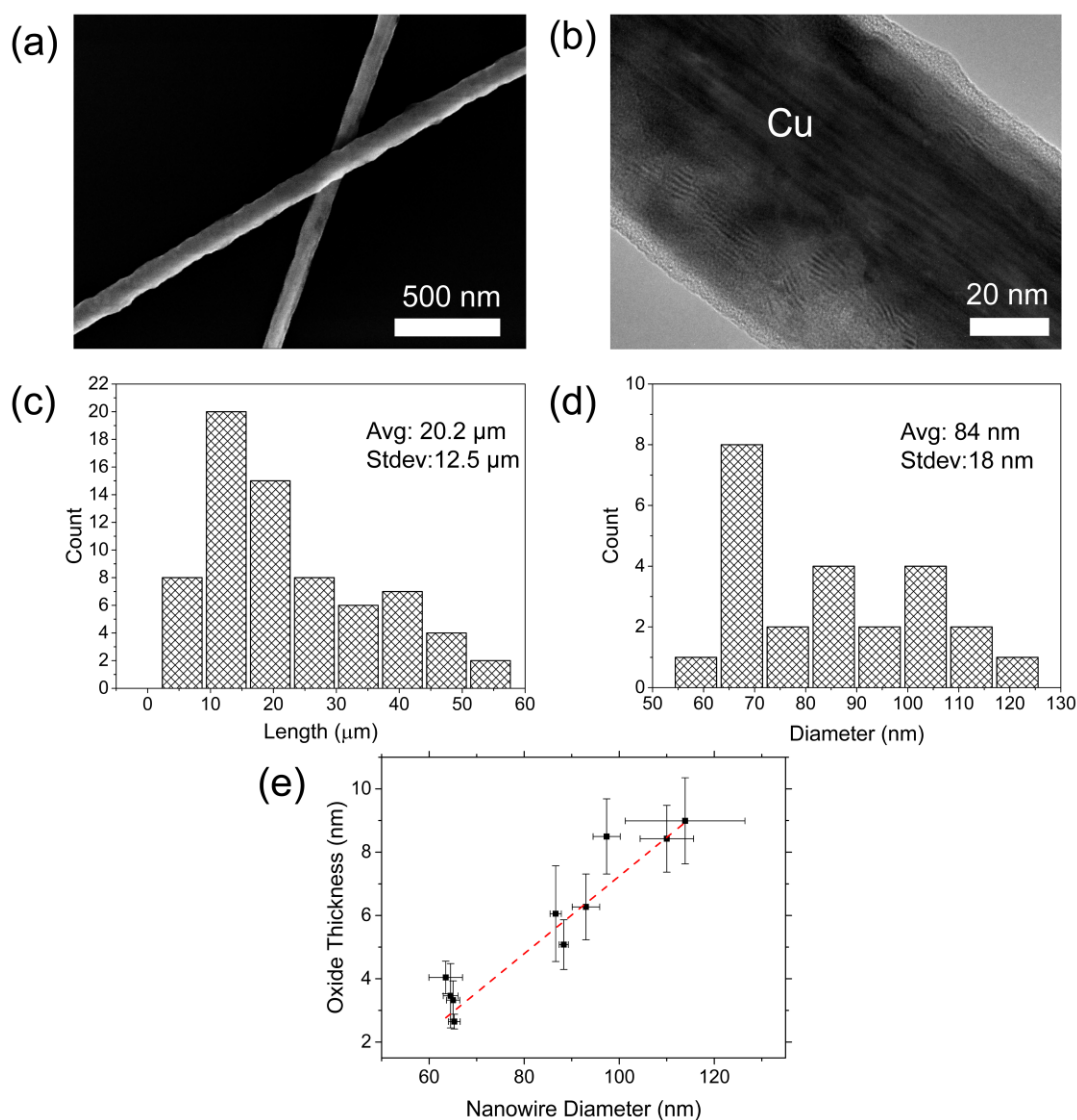


FIGURE 3.3. Characterisation of Cu nanowires. (a) SEM image of two overlapping Cu nanowires dropcast onto a SiO₂ substrate. (b) High resolution TEM image of Cu nanowire with a thin native oxide coating the surface. (c) and (d) show length and diameter distributions of the batch of Cu nanowires used. (e) From TEM inspection a correlation between native oxide thickness with respect to nanowire diameter is shown, errors are generated from the 10 measurements performed on each wire, the red line is a linear fit to the data.

the headspace of the container topped off with Ar gas. This solution protects the wires from oxidation for years once the headspace is re-filled each time with N₂ after the container is opened. To remove the PVP and DEHA, the nanowires were transferred into a volatile solvent using the following protocol: (1) Disperse the nanowires by shaking; (2) Take a sample of the wires, centrifuge at 2000 RPM for 3 mins and remove supernatant; (3) Using a 1 wt% DEHA solution the nanowires were rinsed three times to remove the PVP; (4) The nanowires were then rinsed with ethanol (EtOH) to

remove the water and DEHA; (5) Nanowires were then rinsed with IPA to remove the EtOH. (6) Finally, wires were suspended in IPA at the desired concentration. SEM and TEM images of the Cu nanowires can be seen in Figure 3.3. TEM analysis was performed by Dr Eoin McCarthy using a FEI TITAN microscope. Cu nanowires form a very thin native oxide during the washing and deposition process. Thus, post-processing steps are always necessary to make them highly conductive. The oxide shell can be seen by TEM in Figure 3.3(b). Length and diameter distributions generated using SEM and TEM are shown in Figure 3.3(c) and (d) respectively. The nanowires have an average length of $20.2 \pm 12.5 \mu\text{m}$ and an average diameter of $84 \pm 18 \text{ nm}$ yielding an average aspect ratio of 240. The oxide thickness for several nanowires was measured by TEM and plotted against the nanowire diameter, Figure 3.3(e) shows the near linear scaling of these two quantities, allowing for oxide thicknesses to be accurately estimated from SEM imaging of the nanowire post electrical measurement. The reason for this dependency is unknown and beyond the scope of the current study, but could be explored in future work as a similar dependency was observed for the oxide thickness of Ni nanowires. Larger diameter wires were found to be less uniform along their length as indicated by the large variation in the error bars for the nanowire diameter.

3.2.3 Cu@Ag Nanowires

Core (Cu) shell (Ag) nanowires, denoted as Cu@Ag were synthesized in Prof. Ben Wiley's research group. As previously mentioned, Cu nanowire films are insulating after deposition due to the formation of native copper oxides on the surface of the wires. While methods can be used to sinter, etch and dissolve the oxide, it does not inhibit future oxidation or protect the wires from corrosion. To avoid this, the Wiley group have developed a method of coating Cu nanowires with various metals and oxides.^[24, 31] The system most promising for transparent conductor applications and investigated here is the Cu@Ag core-shell nanowire. The Ag shell has been shown to protect the Cu from oxidation in dry air at 160 °C and under humid conditions (85 % relative humidity) at 85 °C for 24 hrs.^[24] However, due to the reactivity of Ag questions remain about the long-term stability (> 24 hrs) of these films under ambient conditions. The synthesis process for Cu@Ag nanowires is now briefly described from the methods of Steward et al.^[24]

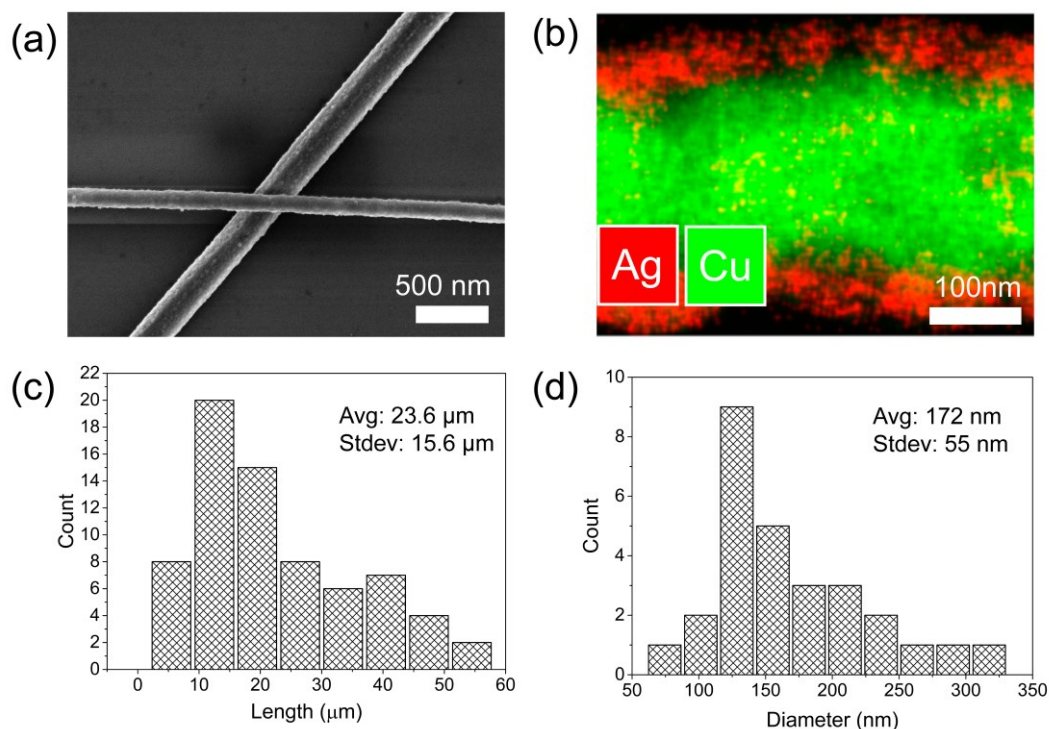


FIGURE 3.4. Characterisation of Cu@Ag nanowires. (a) SEM image of Cu@Ag core-shell nanowires. (b) TEM-EDX mapping of Cu@Ag nanowires taken from Stewart et al.^[24] (c) and (d) represent distributions of the average length and diameter of Cu@Ag nanowires respectively, statistics were assembled from SEM and TEM imaging.

Cu nanowires were synthesized as outlined in the previous section (3.2.2). A sample of Cu nanowires in PVP/DEHA storage solution is taken, and 1 M ascorbic acid is added. The solution is then stirred rapidly for 3 mins, AgNO₃ is added, and the solution is left stirring for a further 2-3 mins. The Cu@Ag nanowire solution is then briefly vortexed to prevent aggregation.^[24] Cu@Ag wires were received in the same PVP/DEHA storage solution as the Cu nanowires, and because of this, the procedure detailed previously (section 3.2.2) was used to disperse the wires in IPA. Afterwards, the nanowires were characterised using SEM and TEM imaging, a sample of which can be found in Figure 3.4(a)-(b). The core-shell structure of the wires was confirmed by TEM analysis carried out by Dr Eoin McCarthy. From TEM, the Ag shell was found to be 5-10 nm thick. TEM energy dispersive x-ray spectroscopy (TEM-EDX) mapping seen in Figure 3.4(b) was performed at North Carolina State University.^[24] SEM and TEM were used to measure length and diameter statistics. The nanowires have an average length of $23.6 \pm 15.6 \mu\text{m}$, and an average diameter of $172 \pm 55 \text{ nm}$ yielding an average aspect ratio of 137.

3.2.4 Contacting Single Wires and Junctions

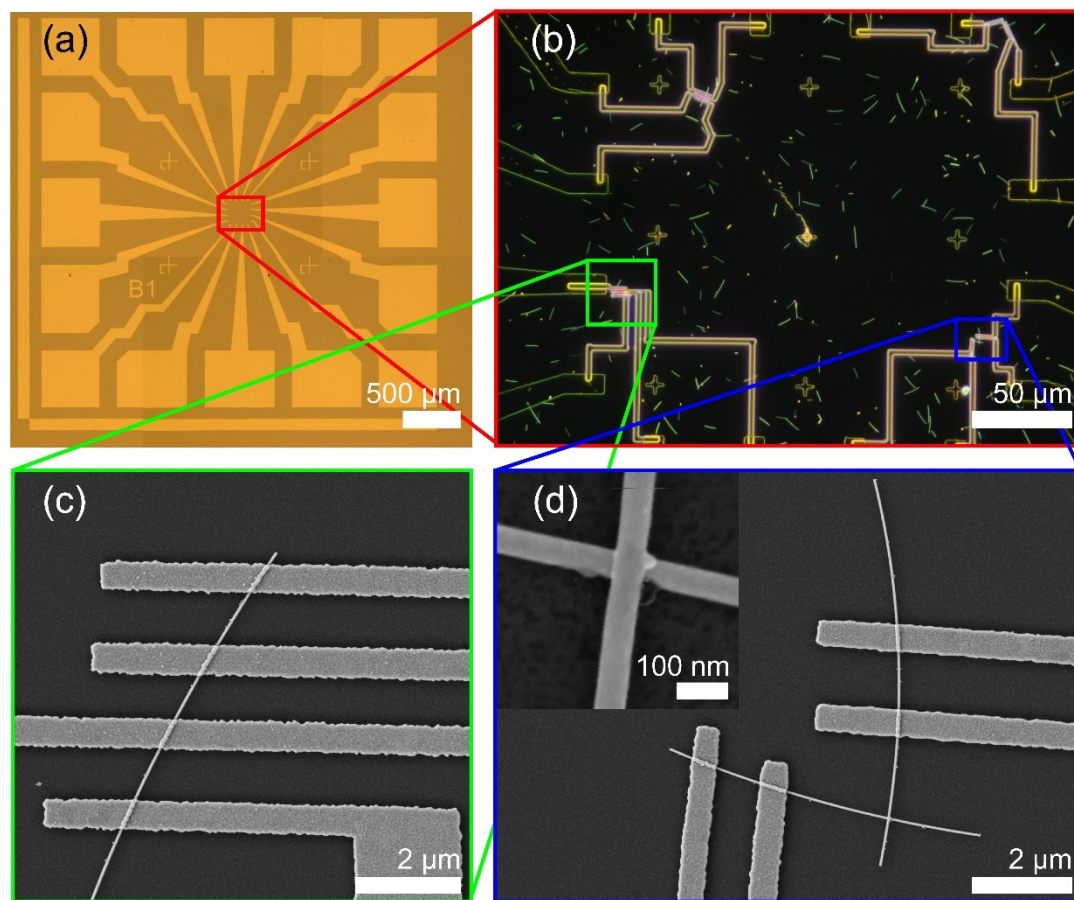


FIGURE 3.5. Optical (a-b) and SEM (c-d) images of single Ag nanowire and nanowire junction devices with four Ag metal contacts fabricated by EBL.

As detailed in chapter 2, mix-and-match lithography, a combination of UV lithography and EBL is used to allow the contacting of nanoscale objects efficiently. To fabricate electrical contacts to a single wire and crossed wires, Si wafers were first diced into 2.2 x 2.2 cm chips. These substrates were patterned using UV lithography and subsequently metallised with Ti-Au (5 nm - 25 nm). Dilute solutions (concentrations varied for each wire type, but was typically on the order of tens of $\mu\text{g} / \text{mL}$) of the nanowire IPA dispersion was drawn into a μL pipette set to 5 μL . A small meniscus was allowed to form at the end of the pipette tip, which was carefully touched onto the centre of each device area and allowed to evaporate in a fume hood. This approach was found to be more successful in concentrating the nanowires in the middle of the usable area and less wasteful than drop-coating the entire substrate with a solution. The sample was inspected under an optical microscope, and the deposition process

was repeated until a sufficient number of isolated wires and crossed junctions had been formed. Nanowires could be removed from the substrate if repeated deposition produced unsatisfactory results by sonication in IPA (37 kHz, 580 W, 60 s). Once potential candidates were located, electrical contacts were drawn, exposed and metallised as outlined in chapter 2. To ensure a good electrical connection to the nanowire the thickness of the evaporated metal layer was set to approximately one and a half times the average diameter of the nanowire. Ag nanowires were contacted with Ag electrodes. Cu nanowires were contacted with Ag electrodes, and Cu-Ag nanowires were contacted with Al electrodes, so that in each case mobile (Ag, Cu) ions could migrate through polymeric or oxide layers and form good conducting pathways. Figure 3.5 shows a macro to nano view of a contacted single nanowire and nanowire junction. The large pads seen in the optical image presented in Figure 3.5(a) are required for contacting by electrical probes. The dark-field optical image in Figure 3.5(b) shows four nanowire samples contacted by EBL in the central area of the electrode array with the smaller and brighter EBL contacts extending and meeting with the UV defined electrodes. Figure 3.5(c) and (d) show a highly-magnified SEM image of a single Ag nanowire contacted with four electrodes, and two overlapping Ag nanowires contacted with a pair of electrodes either side of the junction respectively. Four contacts are required to allow 4-probe measurements in both cases. The inset of Figure 3.5(d) shows a magnified view of the junction.

3.3 DC Electrical Measurements: Single Wires and Junctions

The motivation to perform single wire and junction measurements has already been described, as have the fabrication steps necessary to contact the nanowires for electrical contact. In the following section, the results of the direct current (DC) electrical measurements on Ag, Cu and Cu@Ag nanowires are presented.

3.3.1 Ag Nanowires

As explained in section 3.2.1, the widely-used polyol synthesis method for Ag nanowires results in a thin PVP coating on the surface of the nanowire. This PVP layer presents a barrier to conduction and must be broken down to establish an ohmic contact. In work by Bellew et al., this was achieved by annealing the sample under N₂

flow at 200 °C for 2 hrs in a tube furnace before contacting.^[1] Such annealing steps are commonly used to improve the sheet resistance of Ag nanowire networks.^[4, 7, 9, 13] Electrical activation and breakdown of this polymeric coating also allows for tunable conductivity in Ag and Ni nanowire networks.^[32] The strengthening of individual junctions and co-opting of additional pathways is a self-selective process in which the network attempts to minimise energy and power.^[32, 33] This work will focus on the electroforming method for generating ohmic, highly conducting contacts. To compensate for the material resistance in R_{jxn} measurements, and for use in nanowire network simulations, measurements were performed on single Ag nanowires contacted with four electrodes to determine the material resistivity (ρ) (Figure 3.6(a)). The schematic above the SEM image shows the electrical set up for the 4-probe measurement. As discussed in chapter 2, a current is sourced between the outermost electrodes (source HI and source LO), and the voltage drop is sensed across the innermost electrodes (sense HI and sense LO). During the experiment, the electrical responses of electrodes 1, 2 and 3 are measured relative to electrode 4 which is at a grounded potential. The PVP coating can prevent the wires from being conducting in the pristine state. Electroforming is then required; this involves sourcing an increasing voltage and allowing the capacitive breakdown of the dielectric at the junction to occur. The current allowed to flow through the device under testing is set by a predefined current compliance limit. The current limit prevents permanent damage to the device, and can also be used to control the conductance of the low resistance state to a point.^[34] To form the lowest resistance connection at each contact a current compliance limit of 1 mA was used. A I-V curve of a pristine connection can be seen in Figure 3.6(b), dielectric breakdown occurs in this sample at a forming voltage (V_{form}) of 800 mV. Post electroforming the 2-probe resistance is 524 Ω . This process is repeated for all connections to ensure a stable, low-resistance ohmic contact. The electroforming process is an irreversible resistive switch. It is suspected that the PVP in the Ag/PVP/Ag layer is permanently modified due to redox reactions and Joule heating effects which form a stable connection at the junction.

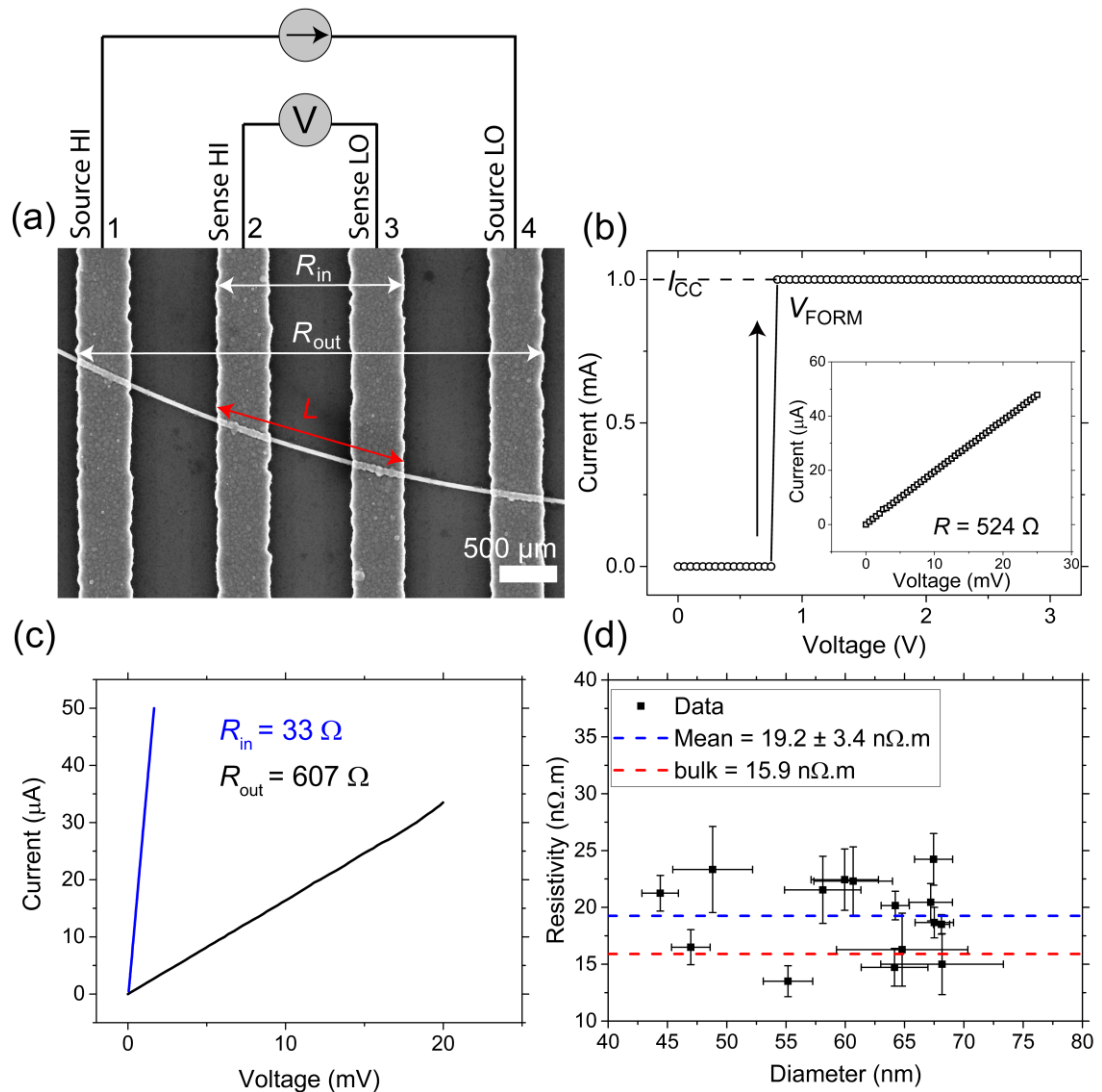


FIGURE 3.6. ρ measurements of individual Ag nanowires. (a) SEM image of a single Ag nanowire contacted with Ag electrodes in a 4-point configuration for calculating the ρ . R_{out} and R_{in} define the outer 2-point resistance, and the 4-point inner resistance which measures the voltage drop across the device length L (red arrow). (b) 2-probe electroforming of a connection to an Ag nanowire at a compliance current of 1 mA, inset is an I-V curve measuring a resistance of 524 Ω . (c) I-V plot illustrating the difference between the resistance of the outer and inner electrodes. (d) Measured ρ for 15 individual nanowires of varying diameter. $\langle\rho_{Ag}\rangle$ was found to be 19.2 ± 3.4 n $\Omega\cdot$ m.

A 4-probe measurement is then performed. Over the course of 100 steps, the current is increased to 50 μ A. Subtracting the voltage measured in sense LO (electrode 3) from sense HI (electrode 2) and plotting this against the sourced current, the I-V characteristics between the inner electrodes can be found (blue curve in Figure 3.6(c)). After application of Ohms law, this method presents two resistance values, R_{out} , which

is the resistance between the outer electrodes, and R_{in} which is the resistance between the inner electrodes. As explained in chapter 2, the 4-probe technique causes the measured resistance across the inner electrodes to be equal to the actual resistance across the device. The ρ can be calculated using equation (2-1), where the length of the channel L is measured from the outside edges of the inner electrodes (red arrow) as recommended by Kolesnik et al.^[35] The diameter was measured eight times along the wire (used to generate diameter error bars) from high-resolution SEM images, and an average value obtained. Figure 3.6(d) shows the results for fifteen individual nanowire samples. The average resistivity for Ag nanowires, $\langle\rho_{Ag}\rangle$ was found to be $19.2 \pm 3.4 \text{ n}\Omega\cdot\text{m}$, slightly above that of bulk Ag ($15.9 \text{ n}\Omega\cdot\text{m}$). No visible dependence of the ρ on the nanowire diameter could be found, though it should be noted that as the diameter of a metal nanowire becomes small relative to the mean free path ($\sim 40 \text{ nm}$ in bulk silver) of the incident electron the electrical resistivity has been shown to increase.^[7, 35, 36] The measured $\langle\rho_{Ag}\rangle$ was used to calculate and compensate for the resistance of the nanowire segments in nanowire junction measurements.

R_{jxn} was calculated for ten samples using the same 4-probe measurement technique as the nanowire ρ measurements. The schematic of the outer circuit measuring the 2-probe resistance R_{out} and the 4-probe inner resistance R_{in} can be seen in Figure 3.7(b). Contributions to R_{in} include the resistances ($R1$ and $R2$) of the nanowire segments (of length $L1$ and $L2$) leading to the junction and the R_{jxn} . Using $\langle\rho_{Ag}\rangle$, the average diameter of the nanowire from SEM and the nanowire lengths ($L1$ and $L2$), resistance contributions for each wire $R1$ and $R2$ may be removed. The junction resistance can be calculated by $R_{jxn} = R_{in} - R1 - R2$.

The results of these calculations are included with twenty-two additional junctions and can be seen in the distribution of R_{jxn} found in Figure 3.7(c), taken from Bellew et al.^[11] Most noticeable is the range of R_{jxn} values, from a few ohms to hundreds of ohms. Interestingly there appears to be no correlation between the junctions which were thermally processed, and nanowire junctions which were electroformed, junctions representing all three processing methods can be found spread across the distribution. Apart from the few outliers, most R_{jxn} values are found below 50Ω , with a strong peak at 11Ω which corresponds to the median value of the distribution.

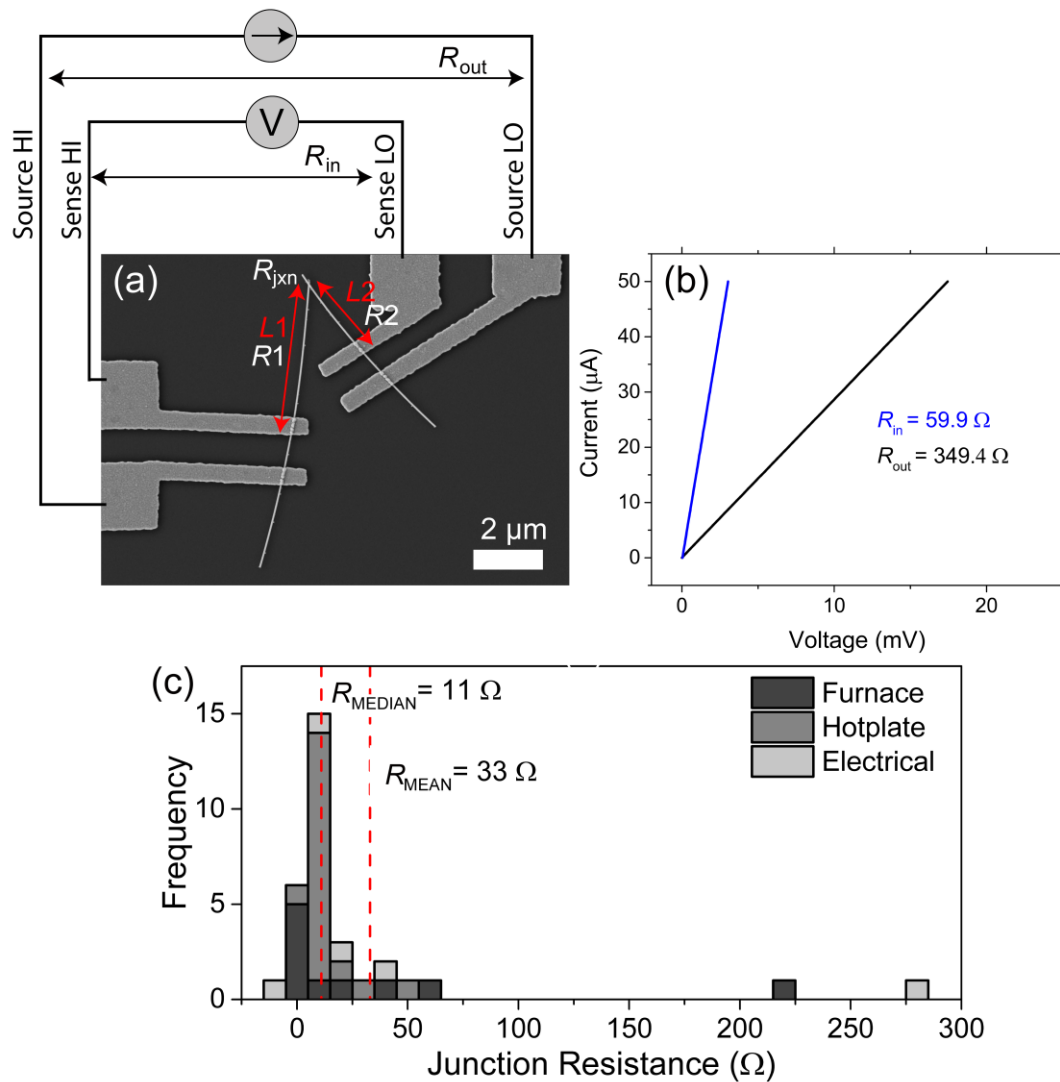


FIGURE 3.7. Ag nanowire R_{jxn} measurement. (a) SEM image of an Ag nanowire junction and schematic illustration of the 4-probe measurement. Current is driven between the outer two electrodes (source HI and source LO), the voltage drop is sensed across the inner electrodes (sense HI and sense LO). The contributions of $R1$ and $R2$ may be calculated using $L1$ and $L2$ and removed from R_{in} , giving an accurate value of R_{jxn} . (b) I-V curve of the inner and outer electrode responses showing the difference between R_{in} and R_{out} . (c) Resistance measurements on 32 Ag nanowire junctions after furnace, hotplate and electroforming of the junction. Dashed red lines indicate the median and mean values of 11 and 33 Ω respectively.^[11]

The morphology of measured Ag nanowire junctions was inspected in SEM post-measurement, a selection of images of this can be seen in Figure 3.8.^[15] It was noticed that furnace annealing resulted in a fused nanowire junction (Figure 3.8(a)), while hot plate and electroformed junctions kept their structure (Figure 3.8(b-c)). What is surprising is the observation that junctions which are not fused together exhibit similarly low R_{jxn} . This is an important result as it implies the welding together of the

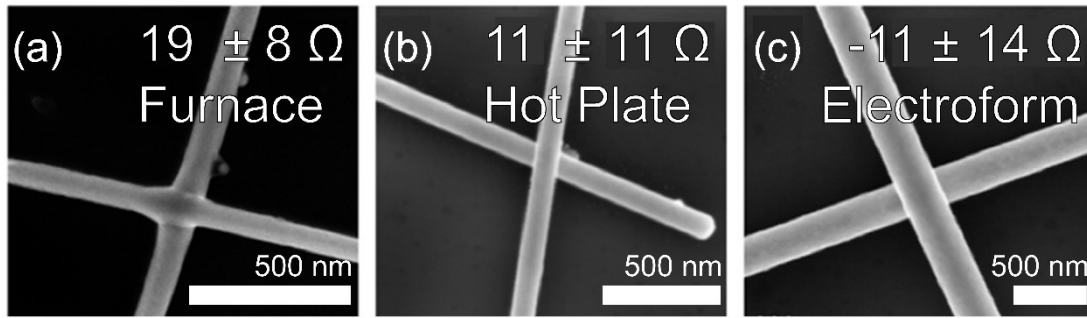


FIGURE 3.8. SEM images of Ag nanowire junctions processed by furnace annealing (a), hot plate annealing (b), and electroforming (c). Welding can be seen on the furnace annealed sample, yet all three processes yield comparably low R_{jxn} .^[15]

junction has little influence over the resulting R_{jxn} . The welding of nanowire junctions has been previously reported and is a common occurrence after annealing procedures.^[11, 37] After the work by Bellew et al.^[1] direct measurement of Ag R_{jxn} values for annealed samples were reported, and agreed with our findings, exhibiting values of $25.2 \pm 1.9 \Omega$. In the same study, Selzer et al. performed direct measurements of Ag junctions which had not been annealed. For these results, R_{jxn} values of $529 \pm 239 \Omega$ were obtained.^[14] No details on the electrical measurement procedure were given in the manuscript regarding electroforming of non-annealed junctions. It is assumed that the high values presented are nanowire junctions which can yet be optimised to a lower limit by a more aggressive electroforming procedure.

The results presented in this section have important implications for the optimisation of Ag nanowire network materials. It should be clear that R_{jxn} for Ag nanowires prior to our report has been overestimated.^[1] Simulations which do not incorporate the inner wire resistance and provide a junction dominated approach (JDA) are not representative of systems where the inter and intra-wire contributions are comparable. The outliers in the distribution also have important implications in determining the ultimate limit of Ag nanowire networks. High resistance junctions have been shown to exist regardless of an annealing process and will have significant consequences for the electrical properties of sparse networks, which have the highest optical transmittance and are most desirable for transparent conductor applications. The results in this section (ρ_{Ag} and R_{jxn}) will be used in chapter 4 for a computational model that investigates the potential of Ag nanowire networks for specific applications, compares their performances and predicts the conductivity limits.

3.3.2 Cu Nanowires

As mentioned in the motivation for this chapter, other metallic nanowire networks have been proposed as transparent conductors. As an alternative to Ag nanowires, it could be strategic to consider cheaper metals.^[7] Among these potential materials, Cu presents as a promising alternative. Cu is 100 times less expensive than Ag, 1000 times more abundant, and considering bulk values, Cu is only 6 % less conductive than Ag ($\rho_{\text{Cu}} = 1.68 \times 10^{-8} \Omega \cdot \text{m}$, $\rho_{\text{Ag}} = 1.58 \times 10^{-8} \Omega \cdot \text{m}$).^[38] Replacing Ag nanowires with Cu nanowires should in principle offer similar performances at a much-reduced cost. There is, however, an issue with Cu nanowire networks; they are electrically insulating after printing due to the formation of copper oxides on the surfaces of the nanowires and must undergo annealing treatments. The study of Cu for metallic nanowire networks is much less developed than that of Ag nanowires. No literature exists on the possible R_{jxn} values for this material, though transparent conducting films with electrical and optical performances approaching that of Ag nanowire networks have been reported.^[38] In this section, the electrical properties of Cu nanowires and electroformed Cu nanowire junctions will be investigated.

Cu nanowires were electrically contacted using the same methods described previously. Figure 3.3(e) shows the diameter dependent native oxide which forms on the surface of the wire. Due to the insulating nature of this oxide shell, and the electrochemically active Cu core when a pair of electrodes are put in contact with a single wire, and a sufficiently high voltage applied, resistive switching can occur. The mechanism of electrochemical resistive switching is explained in detail in chapter 1 but will be briefly presented again. Cu is widely used as an oxidizable (soluble) electrode in many metal-electrolyte-metal (MEM), or metal-insulator-metal (MIM) thin-film devices.^[39] Applying a positive voltage to the oxidizable electrode leads to the dissolution of the metal and the deposition of a metallic filament at the opposite electrode, which then grows back towards the anode, and ultimately bridges the two electrodes at a voltage (V_{SET}), defining a low-resistance ON state (LRS). The resistance of the LRS can be set by limiting the compliance current.

When the compliance current is removed, and sufficient current (I_{RESET}) is driven through the nanoscale filaments in the LRS, Joule heating causes a thermal dissolution of the filament, and the conducting bridge is disconnected, defining a high-

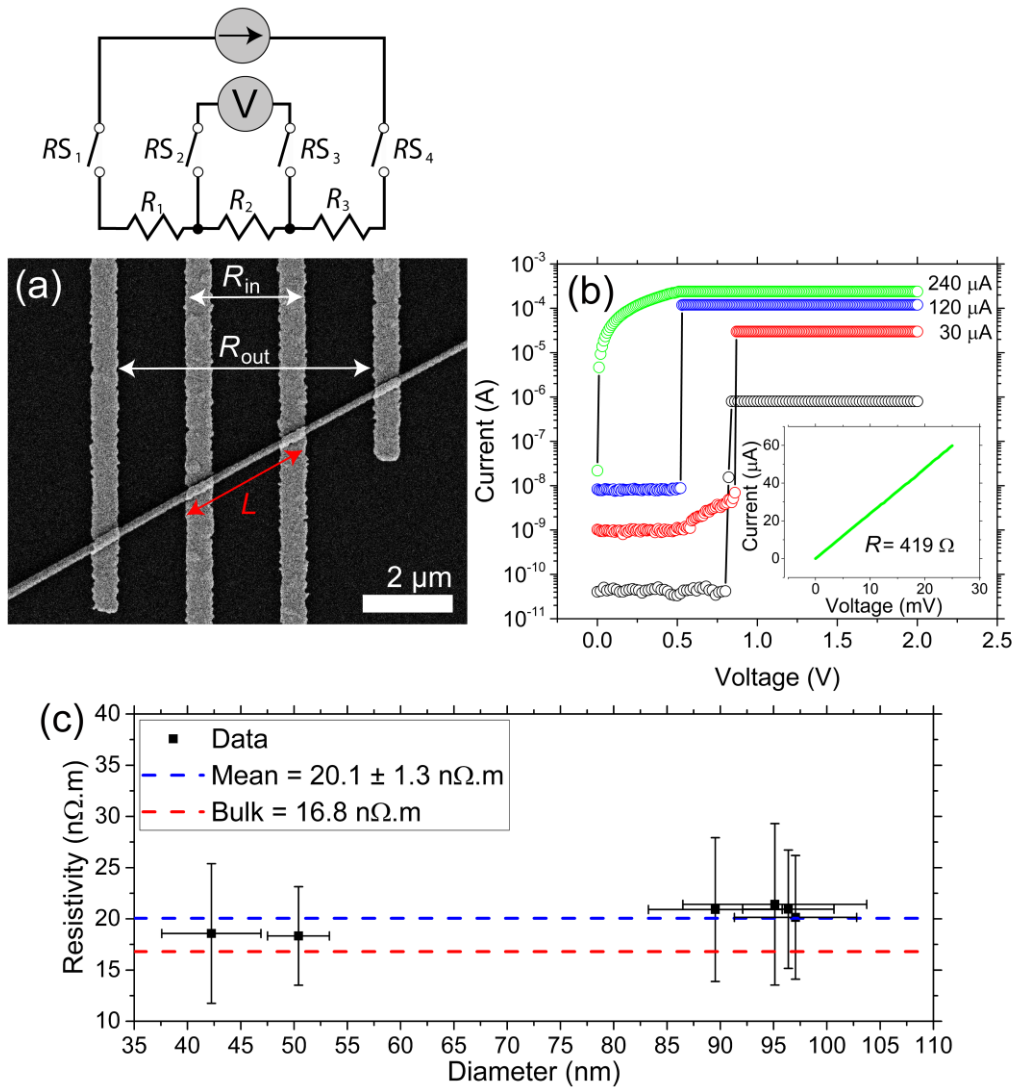


FIGURE 3.9. Electroforming for ohmic conduction in a single Cu nanowire. (a) SEM image of a single Cu nanowire contacted with 4 electrodes for ρ measurements. Above the SEM image is a schematic of the equivalent circuit for a pristine Cu nanowire. (b) I-V curve showing the electroforming process by increasing compliance current, the inset curve shows the low resistance (419 Ω) ohmic response after electroforming. (c) Measured ρ for 6 individual nanowires of varying diameter. $\langle \rho_{Cu} \rangle$ was found to be 20.1 ± 1.3 n Ω .m, with no diameter dependence of the ρ observed.

resistance OFF state (HRS). In nanowire form, copper oxide and cuprous oxide hetero-junctions have been established from as-grown CuO nanowires and have demonstrated non-volatile random-access memory and memristive effects.^[40] The resistive switching behaviours of oxide coated Cu nanowires were not fully characterised in this work as they are beyond the scope of this study but are planned for future work.

As contacted Cu nanowires are insulating, the equivalent circuit of the four switchable contacts is shown in Figure 3.9(a); each contact forms a MIM structure capable of undergoing resistive switching. Establishing a stable low-resistance ohmic contact between the EBL-defined electrodes and the Cu core requires electroforming the connections. Figure 3.9(b) shows an I-V plot where voltage sweeps are performed at increasing compliance currents and the LRS is not retained after the SET event, this is known as threshold switching. After 120 μA compliance current the sample demonstrated a stable low-resistance ($\sim 400 \Omega$) ohmic response, wires were typically stressed to a few 100 μAs as they tended to switch into a HRS at $I_{\text{RESET}} \sim 1 \text{ mA}$.

After each pair of electrodes had been fully electroformed to a LRS, the resistance of the nanowire could be measured using the 4-probe method. Measurement of the length and diameter of the device by high-resolution SEM allowed for the ρ_{Cu} of the nanowire could be obtained. The presence of the native oxide was removed from the measured diameter of the nanowire during the calculations. The actual value of the oxide could not be measured for each sample, however, the linear dependence of the oxide thickness on the diameter of the nanowire as shown in Figure 3.3(e) allowed for a reasonable estimate to be made for each sample. The ρ of 6 samples was obtained, and these are plotted in Figure 3.9(c). $\langle \rho_{\text{Cu}} \rangle = 20.1 \pm 1.3 \text{ n}\Omega \cdot \text{m}$ which is plotted as the red dashed line. The bulk ρ_{Cu} is shown as the blue dashed line at a value of $16.8 \text{ n}\Omega \cdot \text{m}$. Compared to the $\langle \rho \rangle$ for Ag nanowires, this represents a decrease in conductivity of only 4 %.

Establishing the nanowire ρ is crucial for accurately calculating the R_{jxn} . As for single wire measurements on Cu nanowires, an electroforming procedure was run between each of the contacts (electrodes 1-2, and 3-4) to the wire either side of the junction, and then to the junction itself (Figure 3.10(a)). Bringing the junction into a LRS involves creating a conductive filament through both copper oxide shells (Figure 3.10(b)). Thus, the voltages required to SET the device are higher than for a single wire. The electroforming process is carried out similarly to the activation of the electrical contacts on a single Cu nanowire. The voltage is increased until a SET event occurs and the current flow across the device reaches a limiting compliance current (1 mA in this case), through this process, the device is taken from the pristine HRS to a LRS (Figure 3.10(c)). The inset schematic illustrates the conductive filament, which

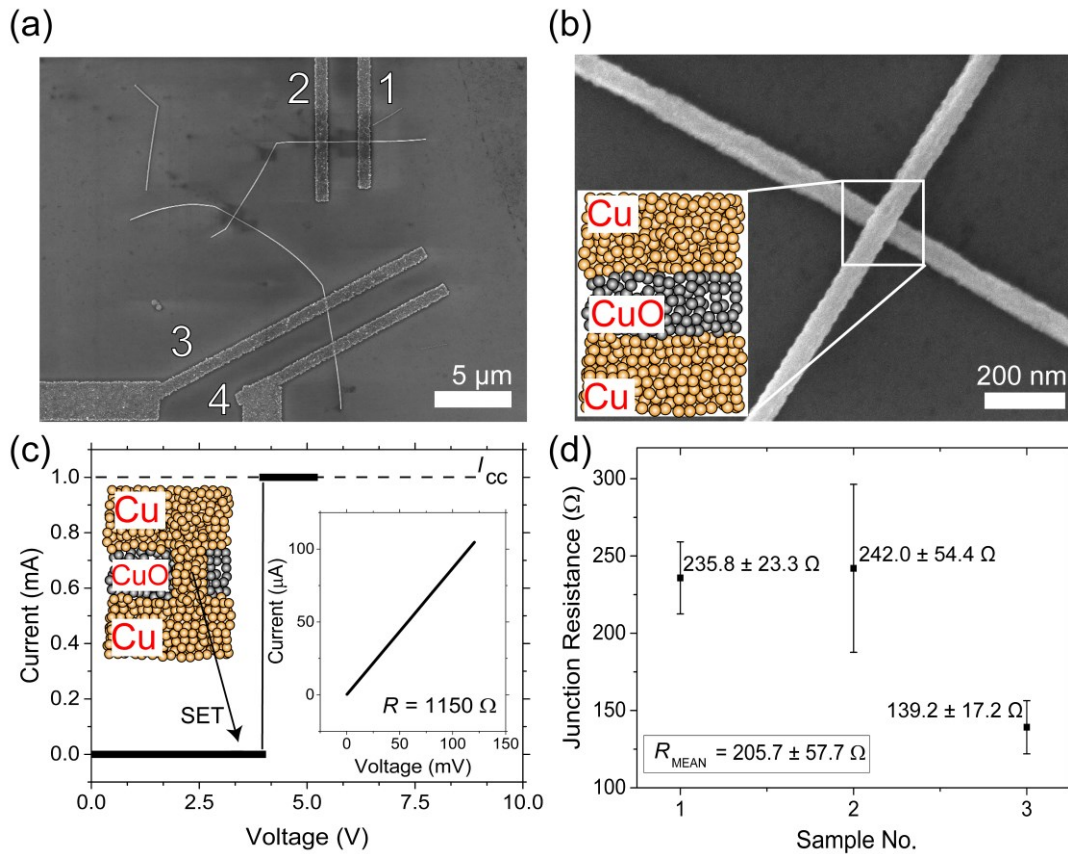


FIGURE 3.10. Cu nanowire R_{jxn} measurement. (a) SEM image of a Cu nanowire junction contacted with four electrodes for 4-probe measurement. (b) Magnified SEM of the nanowire junction, the inset schematic illustrates the metal-insulator-metal structure of the junction in the pristine, non-conductive state. (c) Electroforming I-V curve for the nanowire junction, with a compliance current of 1 mA, the inset graph shows the resistance of a 2-probe measurement after this electroforming with a resistance of 1.15 kΩ. The top left inset schematic depicts the Cu conductive bridge formed through the oxide. (d) Measurements on three individual junctions yield $\langle R_{jxn} \rangle = 205.7 \Omega$.

bridges the two metallic nanowire cores. After a stable electrical connection is made for all the EBL-defined contacts and the junction, a 4-probe measurement of the crossed nanowire structure can be performed.

Removing the resistance contributions from the nanowire lengths up to the junction involves the same calculation as described for Ag nanowire junctions but with one difference. The oxide thickness is removed from the measured diameter of the nanowire as it does not contribute to the electrical conduction along the length of the wire. The graph found in Figure 3.10(d) shows the R_{jxn} measurements for three individual nanowire junctions. $\langle R_{jxn} \rangle$ was calculated to be $205.7 \pm 57.7 \Omega$, significantly higher than the median value of Ag. This larger value is to be expected for

electroformed Cu junctions, given that there is a conductive filament bridging the two oxide shells. Attempts to remove the oxide shell were unsuccessful, (glacial acetic acid and citric acid were used on devices post measurement and imaging). Acid treatments may have removed the oxide briefly, but after drying a rougher oxide had grown and the electrical properties of the wires were even worse. These challenges in measuring the R_{jxn} of Cu nanowires could account for the absence of literature values to date. Extra R_{jxn} measurements after annealing had been planned, however the stock batch of Cu nanowires had oxidised with no way to revitalise them chemically. A second batch of Cu nanowires was received from the Wiley group. However, these nanowires had much worse electrical characteristics. They are significantly larger in diameter with a thicker native oxide and a tapered ‘bone-like’ morphology.

3.3.3 Cu@Ag Nanowires

As previously discussed, the coating of Cu nanowires with 5–10 nm of Ag has been undertaken to make Cu nanowire networks a more attractive alternative to Ag nanowire networks and ultimately ITO. This strategy has been reported to make the nanowire networks conducting after printing and to prevent Cu nanowire oxidation. Resulting networks exhibited optoelectronic properties similar to Ag nanowires networks with similar aspect ratios.^[24] While network performances are ultimately the most important aspect, these cannot be fully optimised without understanding what is happening at a junction level. In this section, the electrical properties of single and crossed Cu@Ag wires are investigated.

As with all the other metallic nanowire platforms described, measurements were carried out to determine the nanowire material ρ . Single Cu@Ag wires were electrically contacted using the methods described previously (Figure 3.11(a)). Samples were conducting as contacted, with a 2-probe resistance of 2.6 k Ω shown in Figure 3.11(c) as the black trace in the I-V curve labelled (1). To reduce this resistance, large currents were driven through the device to further improve the connection as per the red curve (2), after 270 μ A the current level through the device begins to fall and eventually goes toward equipment noise levels. A subsequent sweep (green curve) labelled (3) caused the device to switch to a LRS at 2.6 V and 400 μ A compliance current dramatically improving the 2-point resistance compared to the previously measured values. The green curve goes backwards as the experiment was measuring

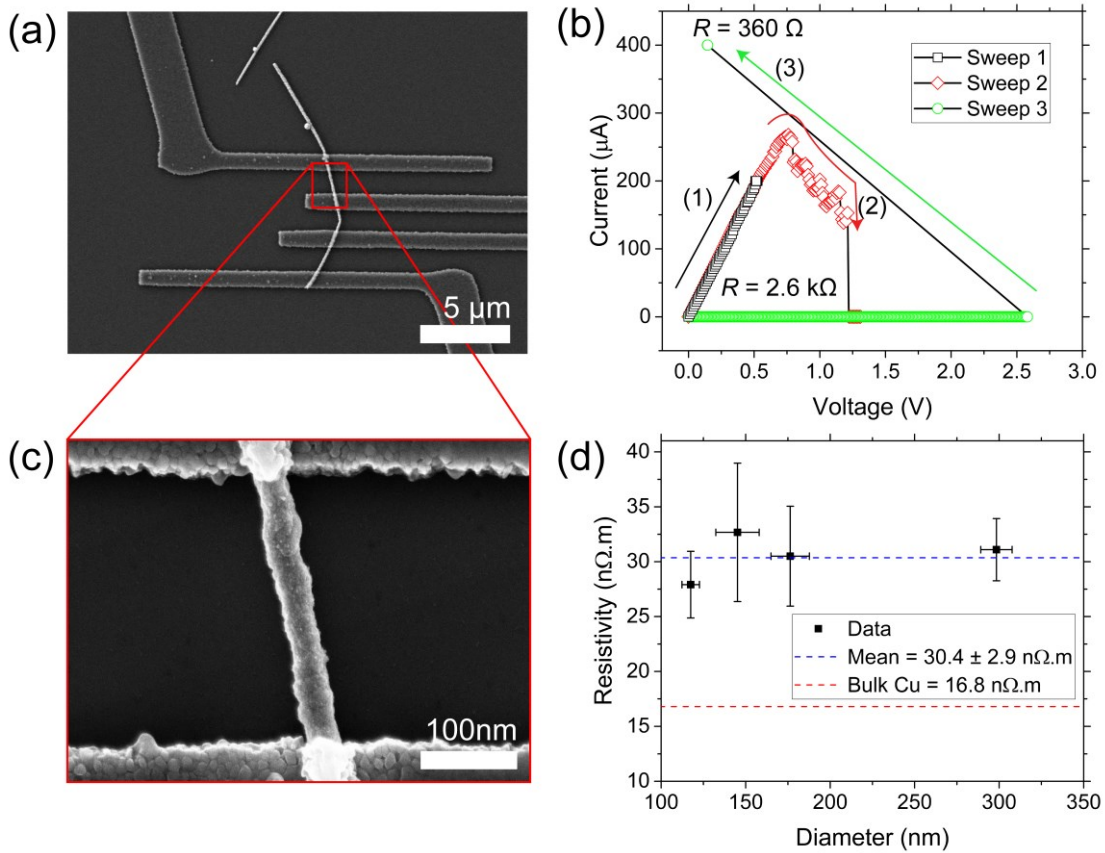


FIGURE 3.11. 4-probe measurement of a Cu@Ag nanowire. (a) SEM image of a Cu@Ag nanowire contacted with four EBL-defined Al electrodes. (b) Electrical resistive switching characteristics of the nanowire between two contacts. An initial ohmic response seen in (1) with a 2-probe resistance of 2.6 kΩ. After a high current sweep (2) the device shows a reduced current response and then no current flow. (3) A subsequent voltage sweep causes the device to switch to a LRS (360 Ω) at 2.6 V shown by the green trace which records the measured voltage (3). (c) Magnified, high resolution SEM image of the region in the red box showing the nanowire electrode interface post electrical measurement. (d) ρ measurements for four individual Cu@Ag nanowire samples, with the bulk ρ_{Cu} shown by the dashed red line, and $\langle\rho_{Cu@Ag}\rangle$ shown by the blue dashed line as 30.4 ± 2.9 nΩ·m.

the actual voltage through the device and not the programmed voltage. That is, when the system reached the compliance limit, it switches to a constant current source supplying only the voltage needed to maintain this level, in this case, 144 mV resulting in a resistance of 360 Ω. A high-resolution magnified image of the red square can be seen in Figure 3.11(c). This shows the interface between the wire and the metal electrode and the morphology of the wire post electrical measurement, which looks to be unaffected by the large current levels and resistive switching.

Using SEM images and the 4-probe data the ρ of four nanowires was calculated, the results are plotted in Figure 3.11(d). The bulk value of Cu is shown as the red dashed line for reference, $\langle\rho_{\text{Cu@Ag}}\rangle = 30.4 \pm 2.9 \text{ n}\Omega\cdot\text{m}$ (blue dashed line). No obvious dependence of the ρ on the nanowire diameter was observed. This is an important result; it shows that by encapsulating the Cu nanowire in Ag, its resilience to oxidation may be greatly improved, but the conductive properties of the wire might degrade. The increased ρ is most likely caused by the thin Ag shell and increased surface roughness which could cause increased scattering.^[36] Increased ρ has implications for the ultimate conductivity of large-scale Cu@Ag nanowire networks which cannot compete with the conduction properties of Ag or Cu nanowires.

The most important aspect to consider when optimising a nanowire network are the junctions. Crossed wire samples were fabricated for 4-probe measurement as previously described, a SEM image of one of these Cu@Ag nanowire junctions can be seen in Figure 3.12(a). As with single Cu@Ag wires, each pair of electrodes on the wire segments and across the nanowire junction was electroformed to at least 400 μA . This allowed for low-resistance ohmic connections between all electrodes in the 4-probe configuration. Figure 3.12(b) shows the 2- and 4- probe electrical response with the inner electrode sensing a resistance of 384 Ω (blue trace), and the outer resistance of 546 Ω (black line). After electrical measurement, the junctions were inspected using high-resolution SEM to determine the lengths of the wire segments from the outer edge of the contact closest to the junction to the overlapping wires and the diameter of the two wires. Using this information and $\langle\rho_{\text{Cu@Ag}}\rangle$, the contributions of the two segments leading to the junction was removed. This resulted in R_{jxn} values of 366.9 Ω and 481.7 Ω (Figure 3.12(c-d)) respectively which are higher than was previously measured for bare Cu junctions. What is interesting to note is the difference in the appearance of the two junctions, the junction with the higher resistance appears to be fused, while the junction measuring 366.9 Ω does not. This result is similar to the Ag nanowire junctions which displayed morphological differences between annealed and non-annealed samples but correlated poorly with low R_{jxn} . These results are relevant in the context of understanding the electrical properties of core-shell interfacial systems.

Protecting the Cu wires from oxidation has consequences on the electrical properties, and thus a balance must be struck between the desired application and the

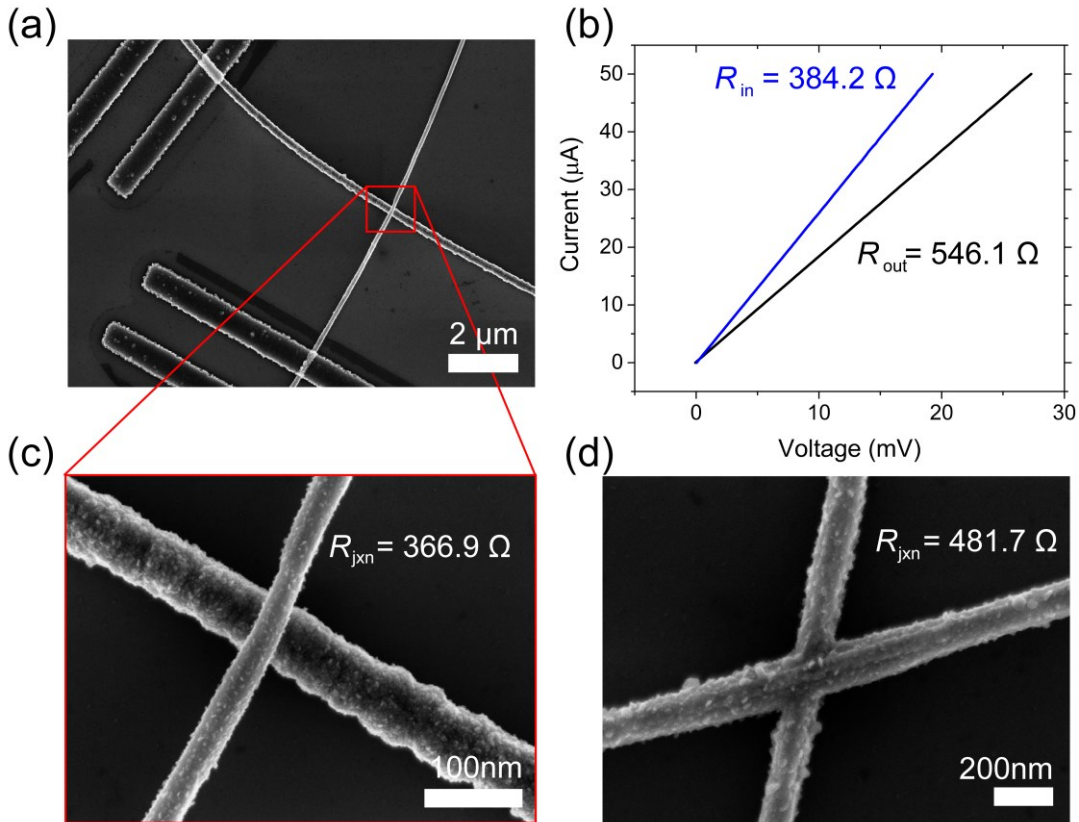


FIGURE 3.12. Cu@Ag nanowire R_{jxn} measurement. (a) SEM image of a Cu@Ag nanowire contacted with two electrodes either side of the junction. (b) After electroforming procedure, the R_{in} and R_{out} (2-point and 4-point) electrical characteristics were taken. (c) Magnified image of the junction pictured in (a) after electrical measurement, R_{jxn} value of 366.9 Ω was extracted for this sample. (d) SEM image of another Cu@Ag nanowire junction with a calculated R_{jxn} of 481.7 Ω . The junction appears to be fused by the Joule heating caused during the electroforming procedure.

most suitable material. These are the first individual nanowire and junction level measurements of this Cu@Ag system and has revealed some interesting single wire resistive switching and electrical conduction behaviours which could be lost in a network level measurement where the network chooses the most conducting pathways.

3.3.4 Ni Nanowires

The values for ρ and R_{jxn} of Ni nanowires are used from the PhD thesis of Dr Bellew.^[15] These values were used as they are readily available for the comparison and simulation of metallic nanowire network systems. Ni nanowires are passivated with a native oxide similar to Cu nanowires. The resistive switching of NiO coated Ni nanowires has been extensively reported in the literature.^[41-45] While Ni nanowires networks are not strongly considered as transparent conducting materials due to their template-based

synthesis and robust native oxide; they could serve a niche purpose in touch sensors, or programmable materials.^[32, 46]

Similar methods were used to determine these values as has been described for all previous nanowires. From three single wire experiments, $\langle\rho_{\text{Ni}}\rangle$ was found to be $62 \pm 19 \text{ n}\Omega\cdot\text{m}$, slightly lower than bulk Ni ($69 \text{ n}\Omega\cdot\text{m}$), but within the limits of experimental error. 4-probe electrical measurements of six Ni nanowire junctions yielded $\langle R_{\text{jxn}}\rangle = 750 \pm 529 \Omega$. These measured values are larger than a similar 2-probe measurement made by Cagli et al. where a R_{jxn} of 265Ω across a Ni/NiO core-shell nanowire junction was reported.^[43] The discrepancy in R_{jxn} was not clear, however, a compliance current of only $10 \mu\text{A}$ was used to electroform the junctions, which may not have been sufficient current to form the best connection possible.

3.3.5 Summary of Nanowire Electrical Measurements.

The physical lengths, diameters, aspect ratio, R_{jxn} and ρ for all systems presented so far in this chapter are summarised in Table 3.2. The R_{jxn} for Ag nanowires published by our group^[1] was corroborated shortly after the publication of Selzer et al.^[14]

TABLE 3.2. Summary of the metallic nanowire systems characterised in this study both in physical terms and electrical performances.

wire type	length (μm)	diameter (nm)	L/D	$\langle R_{\text{jxn}}\rangle$ (Ω)	$\langle\rho\rangle$ ($\text{n}\Omega\cdot\text{m}$)
Ag	6.7 ± 1.8	42 ± 12	159	11	19.26 ± 3.39
Cu	20.2 ± 12.5	84.7 ± 18.7	238	205.7	20.1 ± 1.31
Cu@Ag	23 ± 15	172.6 ± 55.7	133	424	30.4 ± 2.8
Ni	10.6 ± 6.7	81.4 ± 6.9	130	705	62 ± 19

Junction-level measurements on Cu and Cu@Ag nanowires are presented as the first of their kind, giving an important insight into designing new nanowire architectures for transparent conductor applications. Single Ni nanowire measurements were used from the thesis of Dr Bellew^[15] and should be considered as a comparative material with intriguing electrical behaviours, but in reality, it is a material which does not hold much interest in the transparent conductor arena at present. It is evident from the above table that Ag has the greatest potential for highly conductive nanowire networks. These results will be used in the development of a computational model which can determine the ultimate performance limits of Ag

nanowire networks through a one-to-one comparison with experimentally measured nanowire networks. Then, to quantitatively compare the metallic nanowire types presented in this chapter, the data obtained on single metallic nanowires will be used in the versatile computational model, which simulates the electrical properties of metallic nanowire networks factoring contributions from the material and junction resistance. These results will be presented in chapter 4.

3.4 Conclusions

This chapter has presented results on the characterisation of ρ and R_{jxn} of metallic nanowire systems. This includes work published in the most comprehensive study on the fundamental electrical properties of single Ag nanowires to date. The distribution of R_{jxn} , having an average of 33 Ω and median of 11 Ω shows that both electrical activation and thermal annealing can form low resistance junctions with morphological changes induced by annealing providing no benefit in R_{jxn} values. The electrical properties of electroformed Cu nanowires and nanowire junctions were also measured. This nanowire system has been reported to have optoelectronic performances which rival Ag nanowire networks but suffers from the formation of native oxides making R_{jxn} measurements difficult. Cu nanowires were found to exhibit an average resistance of 205 Ω . Cu nanowire systems with Ag shells were also investigated. Cu@Ag nanowires solve the native oxide formation issue and are observed to be conductive as deposited. They manifest interesting electrical behaviours which may not be evident in network scale measurements. ρ values were much higher than either the Cu or Ag system, and R_{jxn} measurements showed values over twice that of Cu nanowire junctions with an average resistance of 424 Ω . The performance of Ni nanowire systems was also investigated, and they have the largest ρ and R_{jxn} of all the systems studied in this work. While unsuitable for high-performance transparent conductor technologies, Ni nanowires could be viable for transparent programmable materials due to their resistive switching properties. These results represent a step towards the development of a rigorous computational model and a materials-by-design approach for nanowire networks, investigating the fundamental material properties of individual nanowires to chase the limits of performance of a collective network.

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4

THE ULTIMATE CONDUCTIVITY OF METALLIC NANOWIRE NETWORKS

In chapter 3, we established that metallic nanowires can exist with a variety of growth-dependent, natural or engineered surface coatings. These coatings dictate the electrical behaviour of the nanowire when contacted and electrically interrogated. We aim to investigate the potential of these individual nanowires as a collective in a functional nanowire network material and ultimately design nanowires which are endowed with new behaviours. The work presented in this chapter combines the 4-probe electrical measurements on single Ag nanowires, crossed nanowire junctions and isolated nanowire networks with a novel approach to network simulation; this work is based on an ab initio model derived from fundamental material properties, electrical equations and optical performances based on Mie scattering of light by small particles. Using the *resistivity* (ρ) and the *junction resistance* (R_{jxn}) data presented in the last chapter for Cu and Cu@Ag nanowires along with a collaboratively developed computational model, a tool will be demonstrated which can determine the ultimate conductivity and predict the optoelectronic performances of nanowire networks. Aspects of the work presented in this chapter have been published in *ACS Nano*, *Nanoscale* and *Physical Chemistry Chemical Physics*.^[1-3]

4.1 Motivation

As technology becomes further embedded into our everyday life, the demands for flexible transparent conducting materials grows year on year. As discussed in chapter 1, conventional transparent conducting oxides (TCOs) are made of very brittle, rare-earth materials, typically tin-doped indium oxide (ITO) or fluorine-doped tin oxide (FTO). The finite supply of rare-earth minerals means the materials which they are based on are becoming increasingly expensive and are inherently incapable of keeping up with market demands for flexible thin-films.^[4, 5] For these reasons, researchers have shown a huge interest in metallic nanowire networks as alternatives to ITO.^[6]

4.1.1 Metallic Nanowire Networks as Transparent Conductors.

Networks of metallic nanowires have the potential to deliver next generation devices reliant on flexible transparent conductors by matching the electrical and optical requirements set by conventional materials (ITO/FTO). Many other potential applications have also been proposed for these new materials, including: transparent thin-film heaters,^[7, 8] electromagnetic interference and static discharge shielding,^[9] emergent programmable and tunable memories,^[10, 11] stretchable radio frequency (RF) antenna,^[12] and polymer light-emitting diodes (PLEDs).^[13] For each of these applications, different electrical and optical performances will be required. For example, displays require high optical transmittance ($T > 90\%$) and low sheet resistances (R_s) ($\sim 10 \Omega/\square$), while touch screens require similarly high transmittances, but can allow for higher sheet resistances ($\sim 500 \Omega/\square$).^[14] Specific applications will have other requirements, depending on which material property is of most importance. These include high transparency or conductivity, stability at high temperatures or when subject to large electrical currents, mechanical or chemical durability, diffusive optical properties may also be desirable (either for practical or aesthetic purposes, for example, in solar cells or privacy glass^[15, 16]) or low-cost. Exploring individual materials for each application would require an enormous scientific effort. A more efficient system would predict the electrical and optical properties of a network using a computational model based on real world physical measurements and suggest materials specifically tailored to the required application.

4.2 Nanowire Network Fabrication

In this section, the fabrication of isolated Ag nanowire networks by a selective area spray deposition technique is presented. The construction of spatially confined and isolated Ag nanowire networks allowed for a precise electrical measurement of the network sheet resistance. Furthermore, it facilitated the wire-by-wire digitisation of these networks into a computational model, which makes a direct comparison between the performances of physical and simulated samples.

4.2.1 Nanowire Network Fabrication

Native or chemically attached surface layers in the form of surfactants, polymers, molecules and oxides prevent aggregation and stabilize nanomaterials in solution. These can be exploited for selectivity, as demonstrated in the work of Widenkvist et al. where the covalent functionalisation of carbon nanotubes (CNTs) allowed for surface-specific targeted adsorption.^[17] Drop casting and spin-coating of nanomaterials into electron-beam lithography (EBL) defined windows has also resulted in the controlled placement of small clusters of quantum dots.^[18] However, a more general technique is required to pattern a range of solution based nanomaterials ranging from nanoparticles to nanowires.

To pattern nanowire networks and other nanomaterial structures, a selective area spray deposition (SASD) technique was developed. SASD was pioneered by Dr Bell in his work on the resistive switching in networks of Ni nanowires.^[19] In his thesis, the SASD technique was used to pattern Ni nanowire networks of various sizes. SASD utilises two techniques previously introduced, spray deposition and EBL. EBL is used to precisely define the shape in the polymeric resist which creates a mask and allows spray deposition for patterning the nanomaterial in that area. When the deposition method was used to pattern Ag nanowire networks a gathering effect was observed. The polyvinylpyrrolidone (PVP) coated nanowires were observed to readily gather inside the EBL exposed openings leaving few nanowires on the poly(methylmethacrylate) (PMMA) surface. The PVP coated nanomaterial displayed an affinity for the SiO₂ substrate which was not previously reported for the oxide coated Ni nanowires. The absence of selectivity was reproduced using Cu nanowires, which also possess a native oxide on the surface of the nanowire.

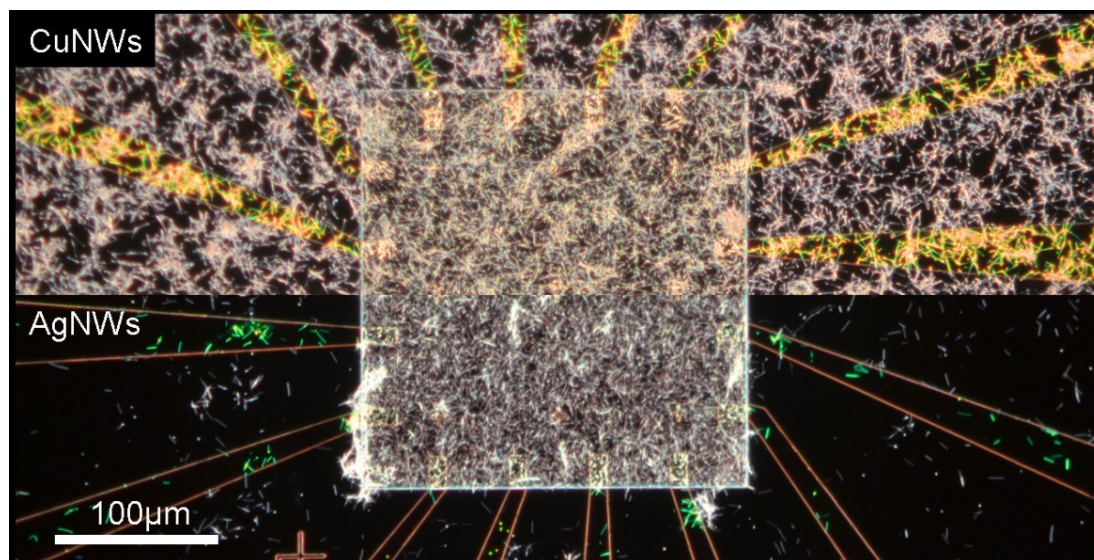


FIGURE 4.1. A composite dark-field optical image of CuO coated Cu nanowires (top) and PVP coated Ag nanowires (bottom) sprayed into a $120 \mu\text{m}^2$ EBL defined area which exposes the pre-patterned SiO_2 substrate.

A striking comparison between Cu and Ag nanowires is given in the composite image displayed in Figure 4.1. The top-half of the image contains a large amount of spray deposited Cu nanowires homogeneously distributed on both the resist surface and the exposed SiO_2 substrate. The bottom-half of the picture illustrates the gathering effect observed when PVP coated Ag nanowires are sprayed under the same conditions with both nanowire systems dispersed in IPA based solutions.

The reason for the gathering effect was investigated by characterising the interactions of a single nanowire on the two surfaces. For this, atomic force microscopy (AFM) measurements were performed in collaboration with Dr Shaun Mills on PMMA-coated, and bare SiO_2 substrates spray deposited with Ag and Cu nanowires. The results are summarised in Figure 4.2. Ag nanowires which were spray deposited onto bare SiO_2 substrates were found to be strongly adhered to the surface and fractured (Figure 4.2(b)) when pushed with an AFM tip in the direction described by the red arrow in Figure 4.2(a). When the same experiment was performed on Cu nanowires which had been spray deposited on bare SiO_2 the nanowire moved under the force of the AFM tip indicating it adhered weakly to the surface (Figure 4.2(c) and (d)). The same weak adherence was observed for both Ag and Cu nanowires which were spray deposited on PMMA (Figure 4.2(e) to (h)). The corresponding lateral force curves concerning the wire displacement for each of the nanowire manipulations are

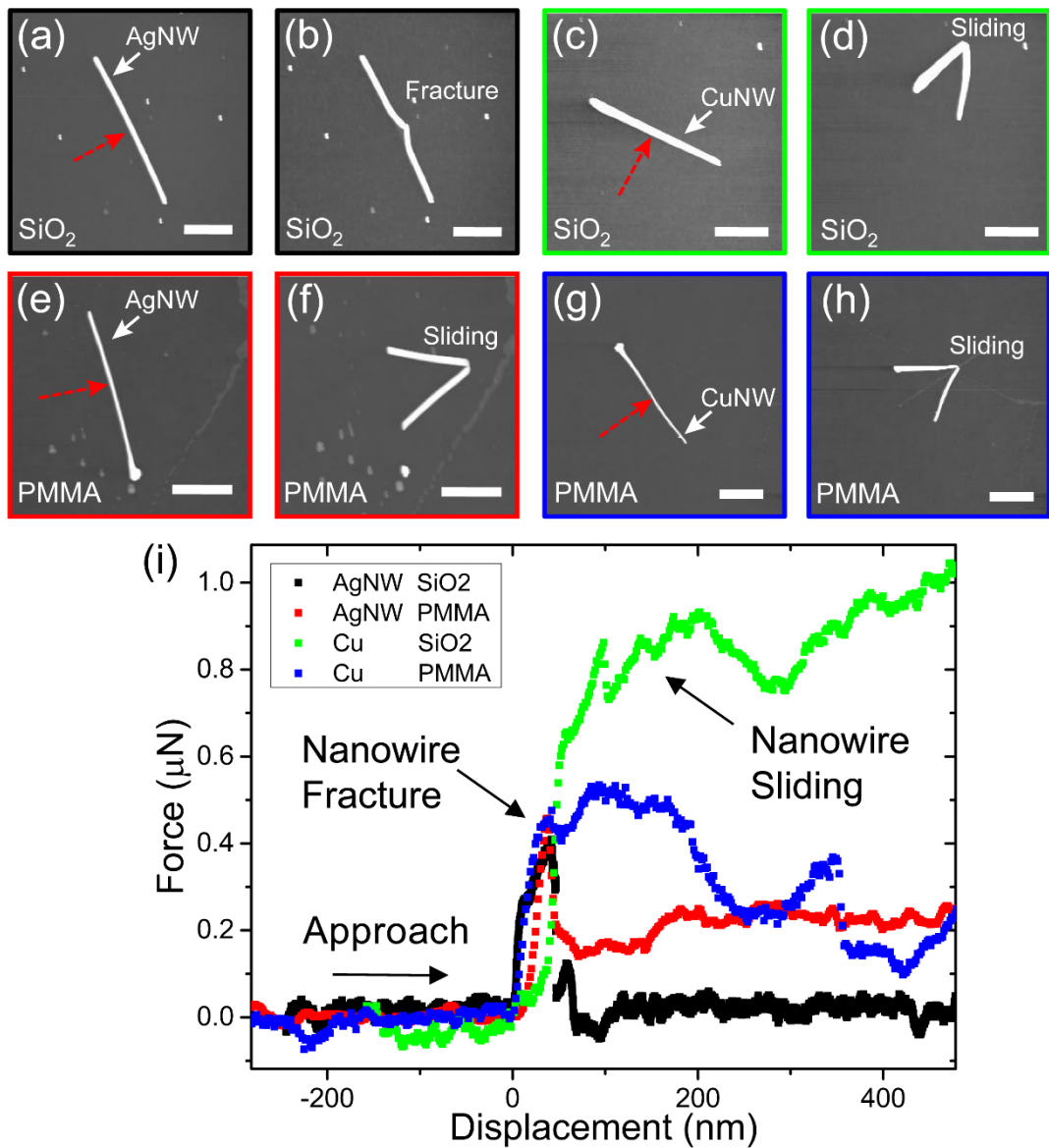


FIGURE 4.2. (a) – (h) Atomic force microscope (AFM) images of Ag and Cu nanowires on SiO₂ and PMMA before and after manipulation with an AFM tip. The AFM tip loading paths are defined by the red arrows. Images (a), (c), (e), (g) show wires before manipulation with the corresponding images after manipulation given in (b), (d), (f), (h) respectively. (i) The lateral force with respect to wire displacement for each of the nanowire manipulations. All scale bars represent 2 μm.

given in Figure 4.2(i). The enhanced adhesion of the Ag nanowires to the SiO₂ substrate is further explored in the thesis of Dr Mills, as it leads to a residual stress in solvent deposited Ag nanowires.^[20] The proposed reason for the strong adhesion to the SiO₂ substrate is believed to be a polymer swelling effect; the PVP can swell in the IPA solution and become more compliant to the surface, enhancing the contact area and the strength of the Van der Waals forces.^[20] It is argued that if the effect was only

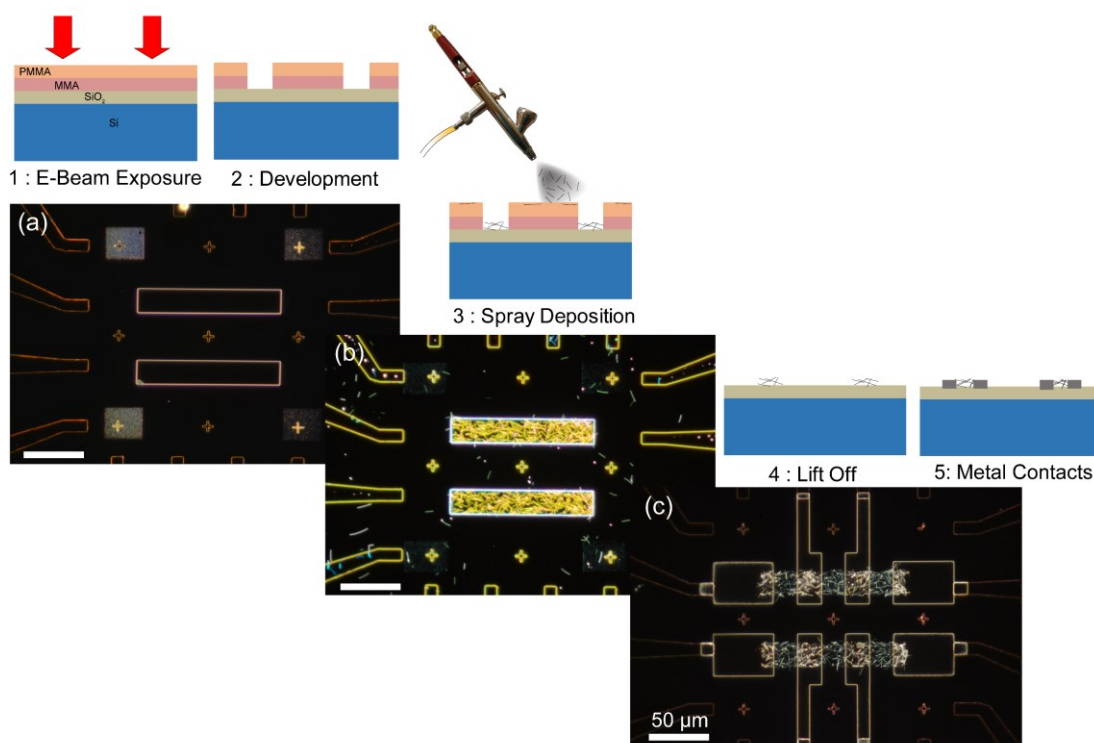


FIGURE 4.3. Overview of the fabrication procedure for isolated nanowire networks. (a) PMMA/MMA is spin coated onto SiO_2 substrate, with windows opened in the resist through EBL. (b) Ag nanowires spray are then deposited onto the chip. (c) Lift-off procedure to remove resist and excess nanowires, Ag contacting electrodes are defined by EBL. All images are dark-field optical images.

surface energy driven, oxide-coated Cu nanowires should strongly adhere to the PMMA surface, which they do not. When sprayed with a high N_2 backing pressure (50 psi) the nanowires in the IPA dispersion are mobile on the surface, in the case of Ag nanowires, this allows the capture of the nanowires once they land on or migrate into the exposed SiO_2 region on the substrate, causing the observed selectivity.

Figure 4.3 illustrates the complete SASD technique, a MMA and PMMA resist is spin-coated onto pre-patterned substrates. Figure 4.3(a) shows how following the EBL exposure of a $120 \mu\text{m} \times 30 \mu\text{m}$ rectangular shape and development the bare SiO_2 is exposed. The nanomaterial can then be spray deposited onto the surface using methods described in chapter 2. Figure 4.3(b) shows Ag nanowires gathered inside the two rectangular windows. Network density can be controlled by the concentration of the nanowire solution, and the amount of solution sprayed. In Figure 4.3(c) excess nanowires and EBL resist is removed using an acetone lift-off. Further EBL procedures can be performed to define electrical contacts, as shown in Figure 4.3(d).

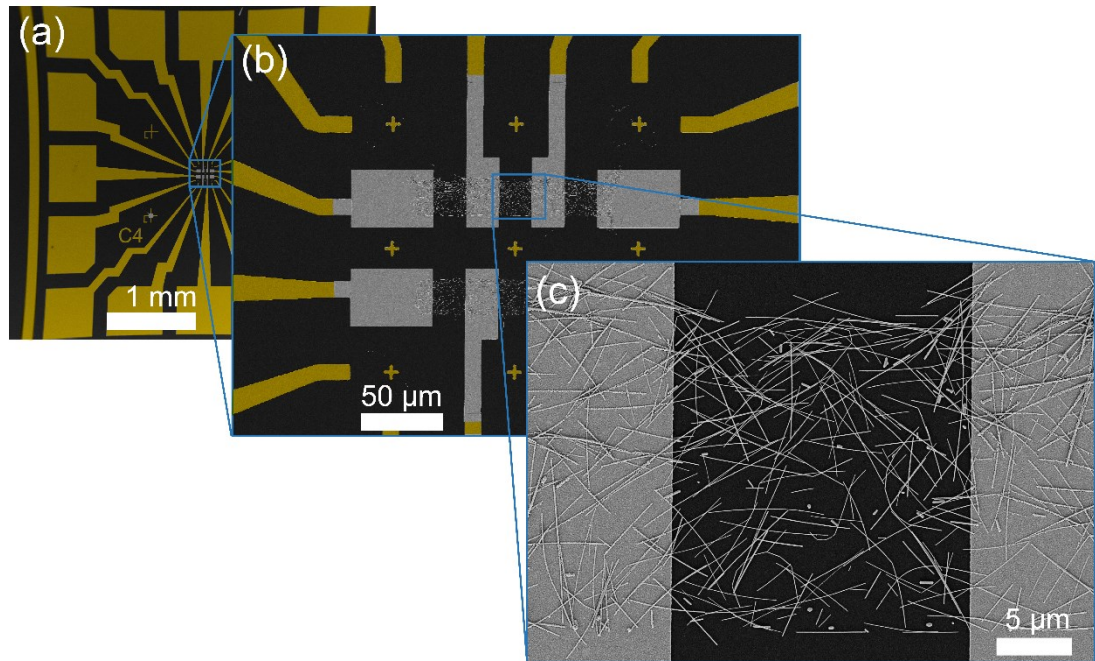


FIGURE 4.4. False coloured SEM images of an isolated Ag nanowire network at increasing magnification. (a) Au false coloured UV defined electrodes of the ‘cryomask’ design. (b) Magnification of the inner working area showing the grey Ag electrodes contacting the Ag nanowire network. (c) 20 x 20 μm Ag nanowire network between Ag contacts.

For convenience, the same UV-defined electrode pattern was used as for the fabrication of single wire and junction samples. The first EBL step involved exposure and development of a 120 x 20 μm rectangular window, which will define the area of nanowire deposition. Ag nanowires at a concentration of 25 $\mu\text{g}/\text{mL}$ were spray deposited onto the surface and frequently inspected using an optical microscope until the desired density was achieved. Excess nanowires on the EBL resist surface are removed using an acetone lift-off step. A second EBL step defines the Ag electrical contacts to the network; these can be seen in Figure 4.4(b) as the grey electrodes making a connection to the Au false-coloured UV defined contacts. Further magnification shows the fine detail of the nanowire network, which is confined and isolated, allowing for careful electrical measurement and one-to-one mapping and simulation. The electrical measurement and simulation of nanowire networks will be discussed in section 4.3 and 4.4 respectively.

4.3 DC Electrical Measurements: Nanowire Networks

To accurately compare the nanowire network simulations, isolated nanowire networks of $20 \times 20 \mu\text{m}$ were fabricated and electrically measured to allow for the first one-for-one comparison between physical and simulated nanowire networks. This section will focus on the DC electrical measurements of these networks and the comparison between electrical and thermal activation of small isolated Ag nanowire networks.

4.3.1 Electrical Network Activation

It has been previously established that PVP coated Ag nanowires are non-conducting in the pristine unprocessed state; a variety of processing methods can be used to create junctions with low electrical resistance. The interest in studying electrically activated networks is threefold. Firstly, it is important to benchmark electrical activation against traditional annealing steps as the electrical activation process is much quicker and far less energy intensive. Secondly, the study of the emergent and evolutionary behaviour that results from the interconnectedness of a network and distribution of electrical stresses is relevant for large distributed systems such as the internet-of-things (IOT) and neural networks; electroforming allows for a self-selective connectivity, decentralisation of information, and energy minimization to be investigated at a fundamental level. Finally, it acts as a real-world benchmark to survey the validity of computational models developed to account for the inter- and intra- wire resistances.

For every sample, each section of the network between adjacent electrodes was electrically stressed (Figure 4.5(a)). The electroforming procedure was carried out by applying multiple 0-5 V dual sweeps (0 to 5 V, 5 V to 0 V) and stressing the network at increasing compliance current up to the mA range as shown in Figure 4.5(b). For the particular network shown, electrical breakdown occurred at 4.2 V and a compliance current of 0.5 mA was used. After activation, the device was in an ohmic, highly conductive state (illustrated by the inset graph which shows a 2-probe resistance of 146Ω) due to the irreversible breakdown of the many insulating junctions chosen to form the conductive pathway between the electrodes. A further I-V sweep which was performed with no current compliance limit can be seen in Figure 4.5(c), this is to illustrate the effectiveness of the 0.5 mA electroforming procedure. The network has an ohmic response until 6.5 mA of current is reached, and then the current response

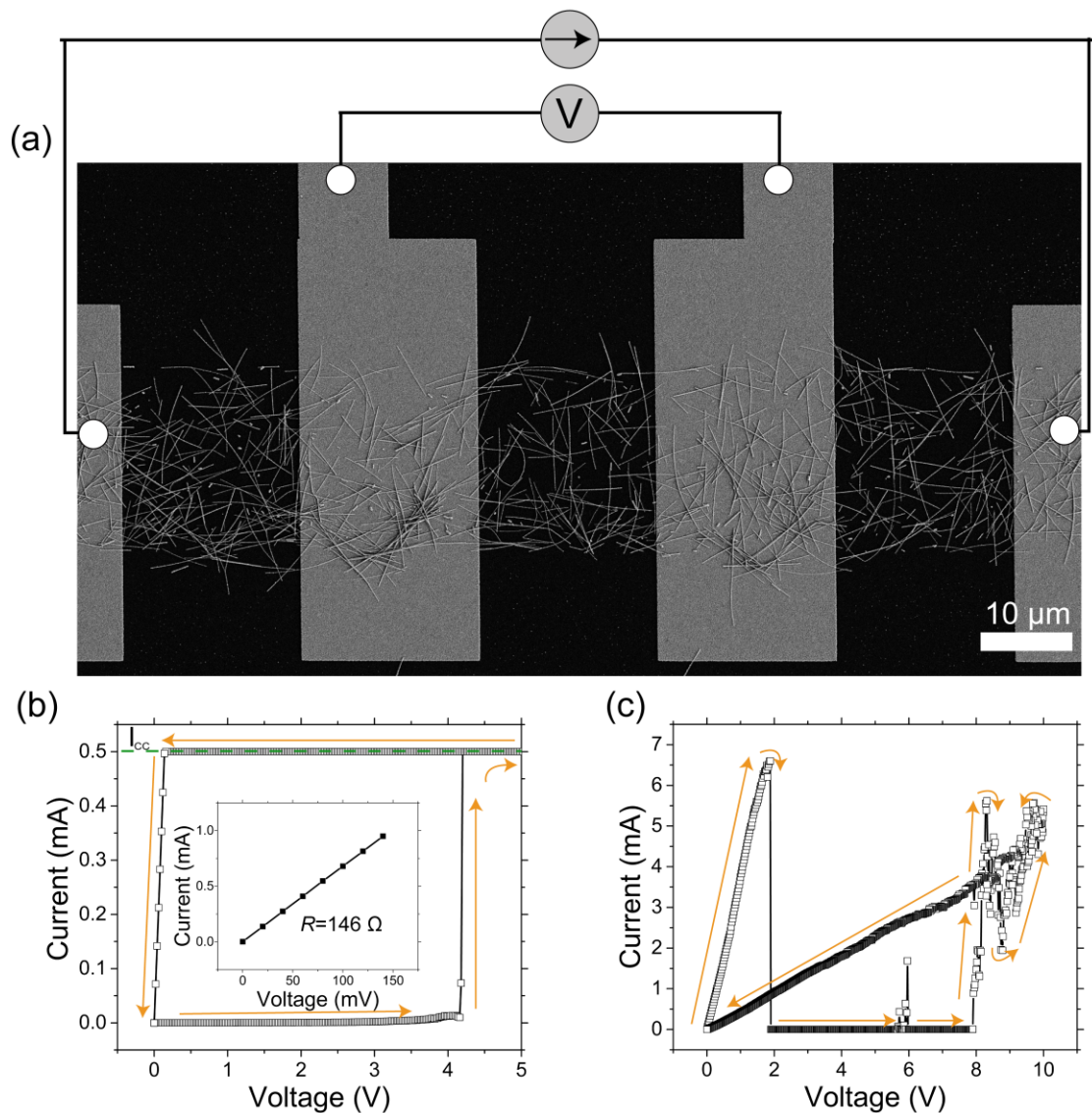


FIGURE 4.5. The electrical measurement of a Ag nanowire network. (a) SEM image of a $20 \times 20 \mu\text{m}$ isolated nanowire network contacted with four electrodes. A schematic of the 4-probe electrical arrangement is also shown. (b) Initial electrical activation of the nanowire network between two electrodes. The network shows no significant current flow until electrical breakdown of a pathway occurs at 4.2 V ; the system then reaches current compliance set at 0.5 mA . The inset curve shows the low-resistance response after electroforming reading 146Ω . (c) Electrical breakdown of the network when it is stressed far beyond the initial forming current. After breakdown, redundant pathways can become activated, though the resistance is significantly higher than before.

breaks down. As previously reported Ag nanowire networks can recover from the failure of the primary low-resistance pathway by re-routing the conduction through alternative connections.^[21] This is shown by the secondary activation at 8 V and higher resistance of the return trace. After electrical activation, the sheet resistance was measured using the 4-probe method. As before, a current is sourced across the outer

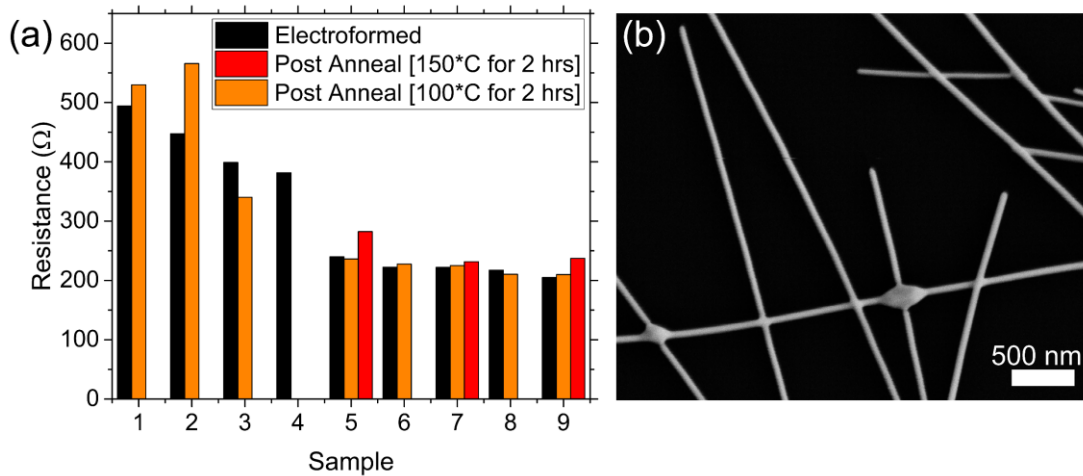


FIGURE 4.6 Results of electroforming and annealing study. (a) 2-probe resistance values for nine $20 \times 20 \mu\text{m}$ isolated nanowire networks as electroformed to a compliance current of 1 mA (black bars), after a 2 hour anneal at 100°C (orange bars), and after an extra 2 hours annealing at 150°C (red bars). (b) SEM image of a section of the nanowire network after annealing. The junctions of the nanowire network are visually melted and fused together.

two electrodes and the voltage drop measured across the inner two electrodes. The negligible sense current across the inner electrodes removes the contact resistance from the measurement, due to the square geometry of the network its sheet resistance value is obtained. Thirty Ag nanowire network samples were measured in this way with distinct wire densities ranging from 0.16 to 0.58 nanowires per μm^2 . These experimental results fed a computational model elaborated in our group that will be discussed in detail in section 4.4.^[2]

To validate the effectiveness of electroforming, isolated nanowire networks were electroformed and then subsequently annealed. Nine $20 \times 20 \mu\text{m}$ isolated Ag nanowire networks were electroformed to a current compliance limit of 1 mA and subsequently annealed in a tube furnace at 100°C , and then at 150°C under Ar flow for 2 hrs at each temperature, with 2-probe electrical measurements taken after each annealing step. The results can be seen in the bar chart in Figure 4.6(a). Electroformed resistances for each of the nine samples are shown in black. The electrical responses taken after the 100°C anneal can be seen in orange. Except for samples 3, 5 and 8, the networks showed a slightly higher resistance after annealing; this could be a result of the melting of crucial low-diameter wires within the network or increased ρ caused by necking at the melted junctions. This logic can be extended to the networks which became completely disconnected after the anneal step. Small isolated nanowire

networks prove to be very sensitive to the destruction of a few critical junctions with even mild annealing steps causing the resistance to increase or for the network to become disconnected. The samples were inspected under SEM where the melting of nearly all junctions was observed (Figure 4.6(b)).

These results show that for small isolated nanowire networks the procedure of electroforming is adequate to optimise the conductivity of the network. For larger nanowire networks (mm to cm scale), electroforming may not produce the lowest attainable sheet resistances.^[6] To benchmark the conduction limit of metallic nanowire networks, computational simulations were employed.

4.4 Simulations of Metallic Nanowire Networks

As described in chapter 1, numerous approaches have been reported in the literature towards a better understanding or means of predicting the properties of nanowire networks. Many of these approaches involve the use of Monte-Carlo methods where ensembles of random networks are seeded and evaluated in order to develop statistical averaging of the results which are then fit to experimental data of similar densities.^[22] In many of these approaches, the inner wire resistance is not considered, and the junctions are assumed to dominate the sheet resistance of the network (Figure 4.7(a)). This is known as the junction-dominated assumption (JDA) and can only be considered valid when the R_{jxn} is significantly larger than the skeletal resistances (material resistance) of the network. This is the case, for instance, of networks made of single CNTs in which the R_{jxn} can reach 98 k Ω s.^[23] The incorporation of the inner wire resistance contribution in our model is referred to as the multi-nodal representation (MNR), this adds extra complexity to the simulations which will be discussed shortly. The MNR description accounts for the finite material resistance of the wires (Figure 4.7(b)) and makes the model more powerful and versatile as it can describe many wire systems of distinct material characteristics. A drawback to this approach is that it requires many more computational resources; memory and processor demands are much higher due to the large number of voltage nodes used to segment the wires. To reduce memory usage and computation time, our group has also obtained a closed form expression – derived from an effective medium theory – which relates the sheet

resistance of the network with numerous characteristic parameters such as wire density, R_{jxn} , the nanowire ρ , the electrode size and separation.^[3]

The network characteristic resistances and SEM images were used by our collaborators in the Theory and Modelling Group lead by Prof. Mauro Ferreira. The SEM images were digitised, and the pixel information was converted into Cartesian coordinates which marked the position of all N number of wires in the network. In the JDA approach, each wire is represented as a node and the whole network is mapped into a voltage grid system comprising of N nodes, in the JDA approach the spatial location of these nodes is unimportant. Overlapping wires are represented as connected resistors which emulate the R_{jxn} (Figure 4.7(a)), this builds a connectivity profile of the network which creates the resistance matrix (\hat{M}_R) which is solved by Kirchoff's circuit equation in the form $\hat{M}_R \hat{U} = \hat{I}$, where the vectors \hat{U} and \hat{I} are the potential at each wire and the current injected/drained from the circuit, respectively.^[24] The R_s is calculated by evaluating $R_s = I / (U_L - U_R)$ where $U_{L/R}$ represents the electric potential on the left/right electrode. The matrix of \hat{M}_R holds the values assigned for each R_{jxn} which are assumed to be homogeneous throughout the network.

The JDA approach is an overly simplistic reduction which could be considered applicable where the resistance of the junctions are far higher than the wire segments, essentially, JDA assumes ballistic transport of charge carriers from junction to junction. A more rigorous approach is required to include the contribution of the inner-wire resistance (R_{in}) of the segments between the junctions.

To include the resistance component of the nanowire segments, each connection point in all wires must be assigned a node, the total number of nodes thus increases from N to $2N_c$ where N_c is the number of interwire connections in the network. This inclusion creates the MNR mapping scheme of the network which is topologically different to the JDA approach. In the MNR representation the positions of the nodes is very important, if two nodes hold the same coordinates (x,y), they describe an interwire connection with value R_{jxn} . Nodes which are nearest neighbours and lie on the same wire are considered inner-wire segments and assigned the appropriate resistance value depending on their separation.

Figure 4.7(c) shows a SEM image of a Ag nanowire network containing approximately 303 wires with a density of 0.68 nanowires per μm^2 . The physical

network was digitised by hand using an interactive canvas widget which allowed the start and end points of each wire in the network to be specified. The outcome of this shows a graph (Figure 4.7(d), replicating the physical network) composed of vertices (junction points) marked with black dots, and edges (wire segments) linking neighbouring junctions in red with isolated wires coloured green where junctions are segments. A chart of the neighbouring node pairs is determined using an adapted breadth-first search^[25] algorithm which inspects the network and results in a resistance matrix \widehat{M}_R which can then be solved to obtain the R_s of the sample.^[2]

The first outcome of the simulations is to provide the network sheet resistance as a function of the average junction resistance $\langle R_{jxn} \rangle$ for both JDA and MNR modalities to compare both methods.^[2] This can be seen in Figure 4.7(e-f). As expected, the sheet resistance grows linearly with R_{jxn} . The experimentally measured sheet resistance for the particular network is shown as the horizontal red dashed line indicating a value of $84.42 \Omega/\square$. At this value of sheet resistance, JDA predicts $\langle R_{jxn} \rangle = 65 \Omega$ whereas MNR obtains $\langle R_{jxn} \rangle = 27 \Omega$ at least when dispersion in R_{jxn} (σ) is neglected.

The incorporation of internal wire resistances within the MNR model shifts $\langle R_{jxn} \rangle$ values downwards with respect to the JDA results, which were overestimating the contribution of the junctions. This shift is due to the contribution of the Ag nanowire skeletal resistance which is neglected in the JDA. This provides information on the ultimate performance limit of the nanowire network assuming the most ideal situation in which all $\langle R_{jxn} \rangle \rightarrow 0$, which in this case is about $50 \Omega/\square$. Adding a level of dispersion (σ) to the standard distribution of R_{jxn} induces a deviation from the linear dependency of R_{sheet} vs $\langle R_{jxn} \rangle$. This disorder could account for the natural distribution of junction resistances which play a role in the determination overall sheet resistance. A small dispersion, between 20 and 30Ω would be necessary to bring the $\langle R_{jxn} \rangle$ closer to the measured median value of 11Ω . With no dispersion necessary to align the simulated $\langle R_{jxn} \rangle$ with the experimentally measured $\langle R_{jxn} \rangle$ of 33Ω .

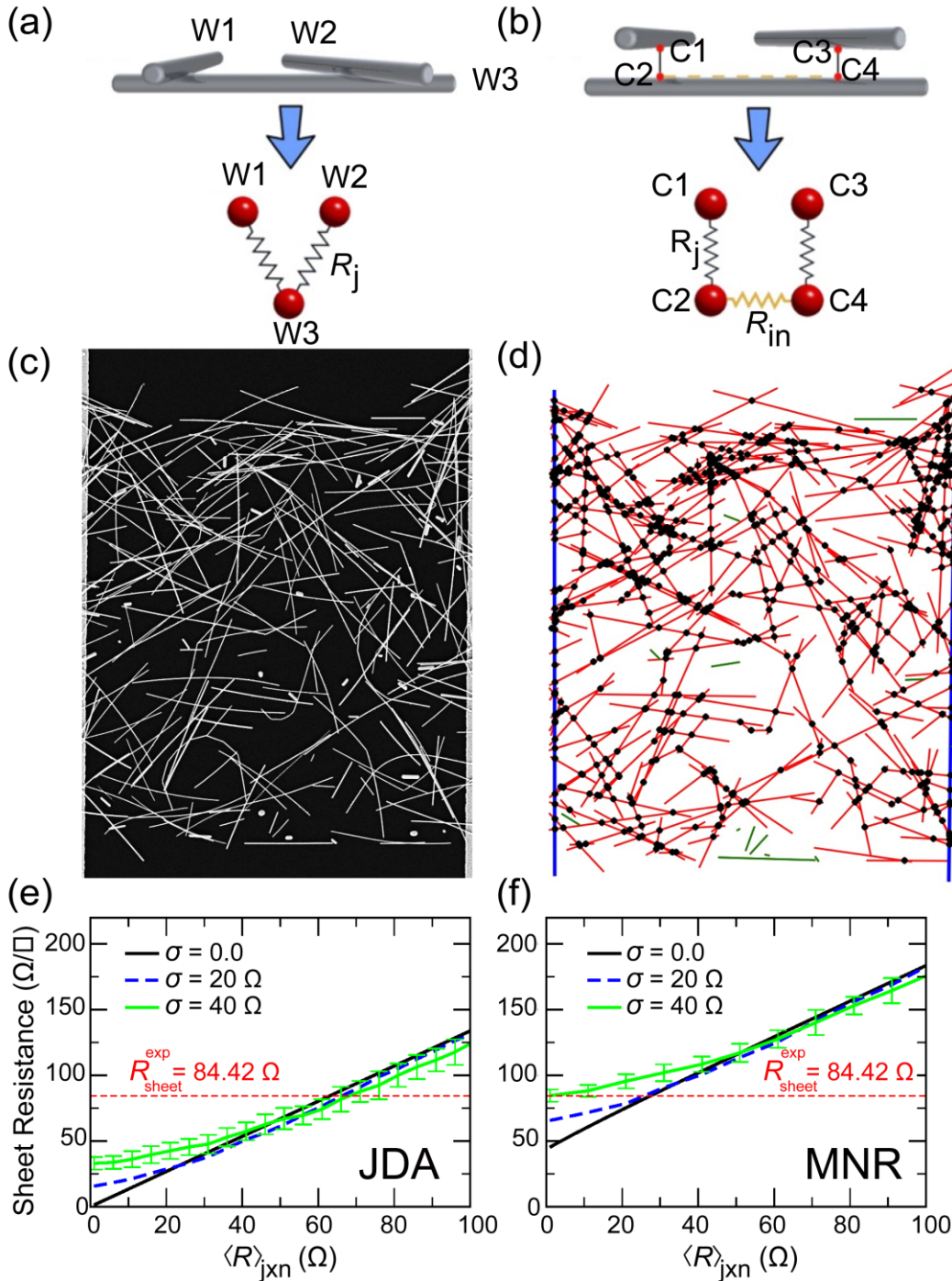


FIGURE 4.7. Nodal mapping schemes (a) JDA and (b) MNR models. (c) SEM image of an Ag nanowire network that was computationally mapped shown in (d). Junctions are displayed as black dots with connected wire segments shown in red, and disconnected wires appear as green. The electrodes are denoted by the blue vertical lines. (e) – (f) Sheet resistance versus $\langle R_{jxn} \rangle$ analysis performed on the above network using the JDA approach (e) and MNR approach (f). The black solid lines correspond to the cases of a homogeneous network with all junctions having the same resistance. Additional curves were obtained considering a heterogeneous nanowire network in which $\langle R_{jxn} \rangle$ follows a Gaussian distribution of mean value $\langle R_{jxn} \rangle$ and standard deviation σ .^[2]

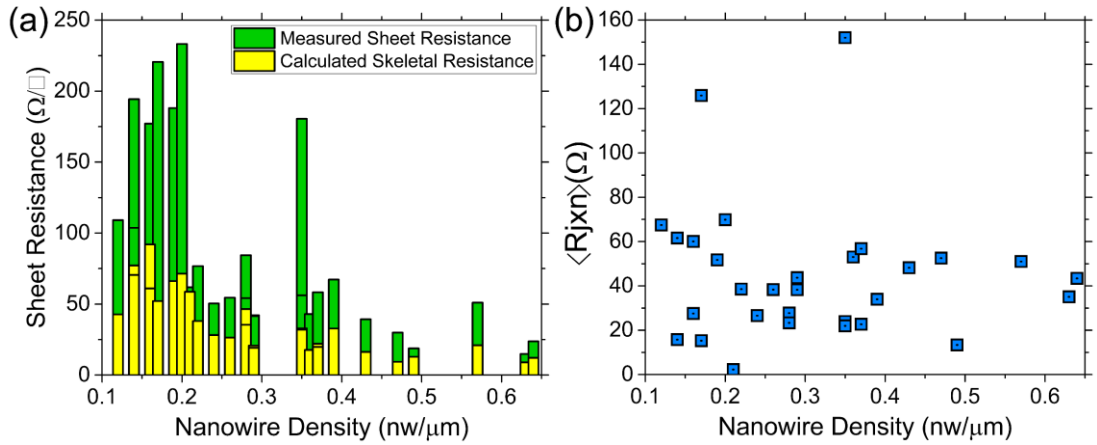


FIGURE 4.8. (a) Measured (green) and calculated (yellow, from MNR model) sheet resistance of thirty $20 \times 20 \mu\text{m}$ Ag nanowire networks for network densities ranging from 0.1 nanowire/ μm^2 . (b) Average junction resistance calculated for the thirty distinct networks with respect to the nanowire density.

The output of the model allowed each of the thirty nanowire network samples to be analysed with respect to the calculated skeletal resistance, measured sheet resistance and their optimum conductivity.^[2] Noteworthy is the fact that on average $49 \pm 16 \%$ of the overall sheet resistance could be attributed to the skeletal resistance of the network (material resistance) when analysed by the MNR model. The contribution of the calculated skeletal resistance with respect to the measured sheet resistance and the nanowire network density can be seen in Figure 4.8(a). For the thirty nanowire networks a $\langle R_{jxn} \rangle$ could be calculated by aligning the experimental and calculated sheet resistance.

For the majority of cases $\langle R_{jxn} \rangle$ was below 80Ω and agrees reasonably well with the experimentally measured average R_{jxn} of 33Ω . The $\langle R_{jxn} \rangle$ represents a distribution of junction resistances which account for naturally highly resistive outlier junctions which were reported in chapter 3. Ultimately the MNR approach is a powerful tool with the ability to establish how much potential for optimisation a network has. Moreover, it allows for the relative contributions of the junction and the wire material to be compared. Through these simulations we uncover that the resistance provided by the material of the network is as important as the R_{jxn} for high performance Ag nanowire networks.

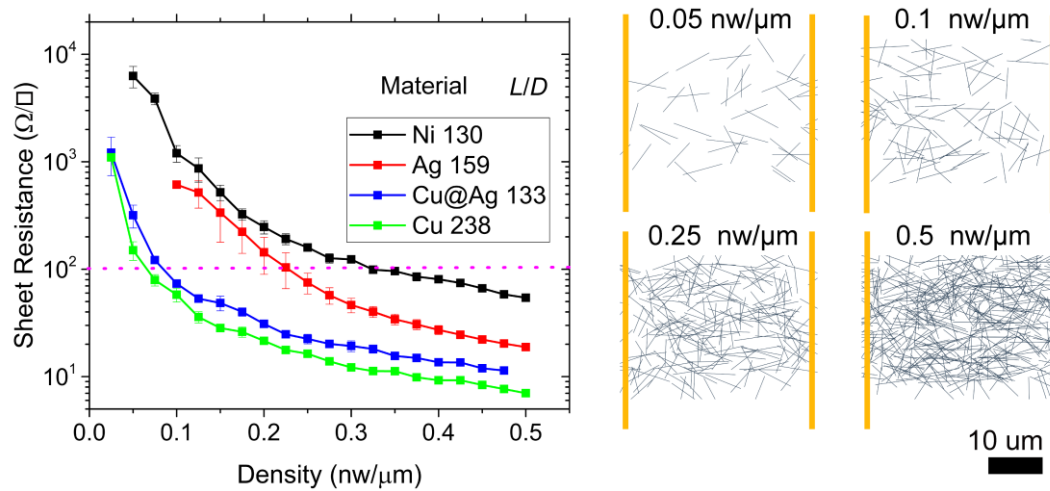


FIGURE 4.9. MNR nanowire network simulations of the experimentally measured metallic nanowire systems from chapter 3, the industry specified limit of $100 \Omega/\square$ is marked by the magenta dotted line. Visual examples of 0.05, 0.1, 0.25 and 0.5 nanowires/ μm densities for Ag nanowires with a $30 \mu\text{m}$ separation between the electrodes is shown to the right of the main plot.

To benchmark the potential of the materials investigated in chapter 3 for transparent conductor applications, MNR simulations were used to calculate the sheet resistance at various densities. The results in Figure 4.9 show the sheet resistance (R_s) values for Ni, Ag, Cu@Ag and Cu nanowire networks as a function of the density of the network measured as the average number of nanowires per μm^2 . Visual representations of 0.05, 0.1, 0.25 and 0.5 $\text{nw}/\mu\text{m}$ densities for Ag nanowires ($6.7 \mu\text{m}$ in length, 42 nm in diameter) are pictured beside the main plot. The comparative simulation of metallic nanowire networks of $30 \mu\text{m}^2$ size takes the inner wire resistance into account and uses experimentally measured values of R_{jxn} . Length and diameter values are drawn from those presented in chapter 3. As expected, low-density networks which are the most optically transparent, display the highest sheet resistance as there are fewer parallel pathways and a larger number of junctions in series connecting the electrodes. To fully describe the optoelectrical properties of the simulated networks, the wire density value must be related to the optical transmittance.

For transparent conductor applications, various sheet resistance targets must be met, appropriate to the desired application. Previous works have modelled the optical performance of nanowire networks using various methods as discussed in chapter 1. One method involves reducing the nanowire network to an approximate film thickness and calculating the transmittance in a similar method to that used for continuous thin-

films.^[26, 27] Optimising the sheet resistance and transmission values simultaneously requires increasing the aspect ratio of the nanowire, this effect cannot be accounted for by the thin-film method.^[28] Fundamentally, increasing the length of the nanowire has a huge effect on the onset of percolation as the critical number density of sticks required for percolation (N_c) is given as $L^2/5.637$.^[29] A method proposed by Bergin et al.^[28] involves relating density to transmittance by experimentally measuring and fitting data to produce a diameter and wavelength-dependent fitting parameter which can predict the transmittance of a nanowire film.^[22] The term AF is the area fraction of the substrate covered by the nanowires. Which is simply the density (N) of the nanowires multiplied by the length (L) and diameter (D) of the nanowires.^[28]

$$AF = N \times L \times D \quad (4-1)$$

The transmittance can then be calculated with the following equation,

$$\%T = 1 - a_1 100AF \quad (4-2)$$

The fitting parameter a_1 was reported to be 0.87 for 40 nm diameter Ag nanowires.^[28]

As described in section 1.2.3 , the Mie light scattering approach can be used to predict the optical transmittance of a metallic nanowire network by^[30],

$$\%T = e^{AF \times Q_{ext}} \quad (4-3)$$

Where Q_{ext} represents the amount of light blocked by a single nanowire according to its extinction cross-section and is essentially the ratio of the amount of light scattered and absorbed by a nanowire relative to its geometric cross-section.^[31] Values for Q_{ext} were calculated from the far-field solution of MatScat.^[32, 33] MatScat is a MATLAB package which contains an implementation of electromagnetic scattering by cylinders based on Mie theory; the physical solution for which is taken from the book by Bohren and Huffman^[34] and detailed in section 1.2.3 . The calculation of Q_{ext} requires only the diameter of the nanowire and the optical constants for Ag ($n = 0.13936$, $k = 3.5604$, $\lambda = 546$ nm)^[35] and Cu ($n = 1.0344$, $k = 2.57984$, $\lambda = 546$ nm).^[35]

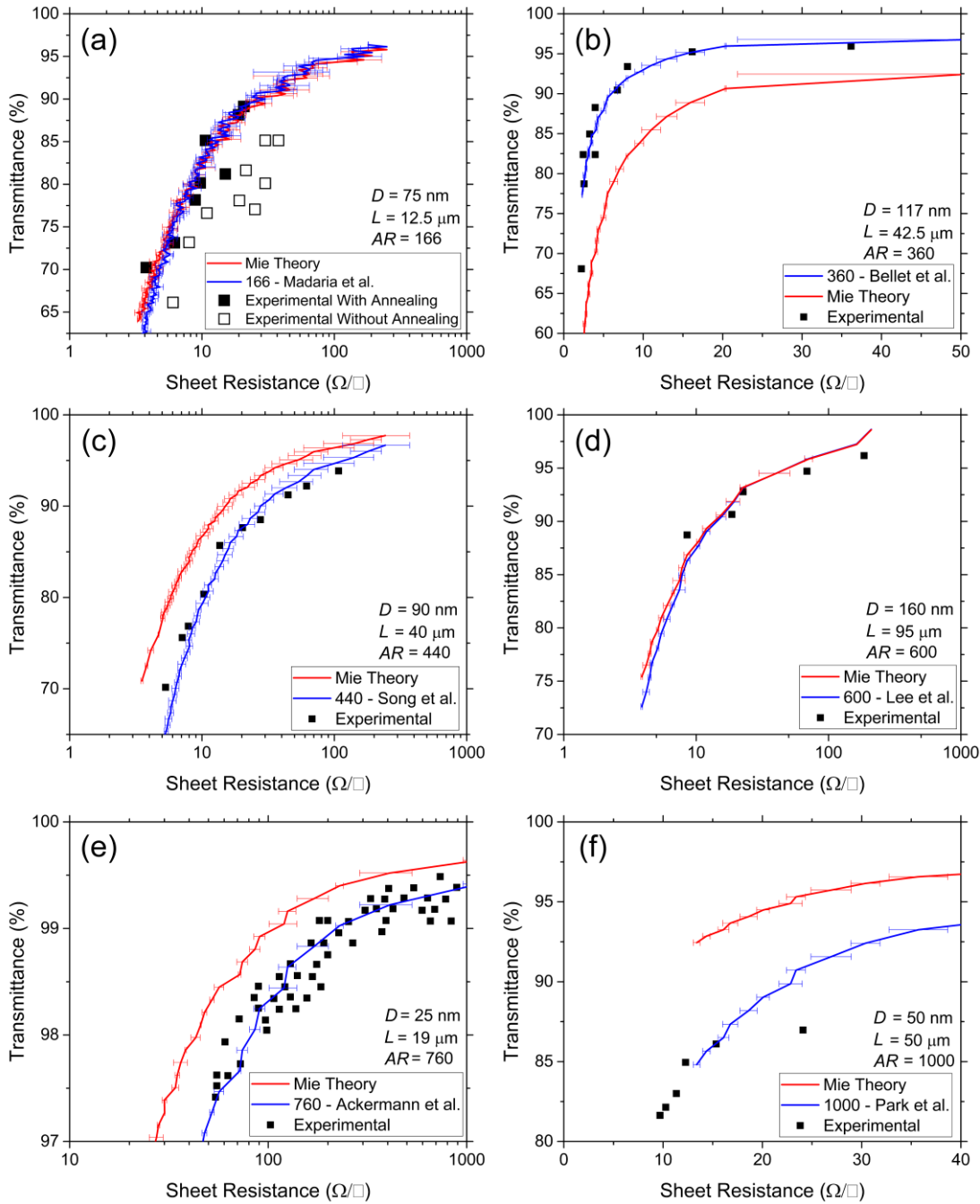


FIGURE 4.10. MNR simulations of metallic nanowire networks for various literature inspired aspect ratios. (a)–(f) Black squares indicate reported experimental data for nanowire networks of aspect ratio: (a) 166^[36] (white squares indicate experimental data without the 20 min 200 °C annealing step) (b) 360^[6] (c) 440^[37] (d) 600^[38] (e) 760^[39] (f) 1000.^[40] In each case the red curve represents the sheet resistance values as computed by the MNR model with treatment of the network density to a transmittance by Mie theory (Eqn (4-3)). The blue curve is a fit to the experimental data by the linear method of converting density to transmittance outlined in Eqn (4-2).

Figure 4.10 displays the results of MNR simulations (network size >2 times nanowire L , 3 sample averages, densities dependent on the aspect ratio; simulations ran from the percolation threshold to the limit of the machine memory) of literature inspired nanowires of aspect ratios ranging from 166 to 1000. Networks composed of these nanowires were simulated with the MNR method using ρ and R_{jxn} data experimentally measured in chapter 3. The black squares represent the experimental data reported in the literature for each case. The blue curve in Figure 4.10(a-f) is a fit to the experimental data by the linear method presented in Eqn (4-2); where the fitting parameter a_1 was set to agree as closely as possible to the experimental data to investigate whether a correlation exists between the fitting factor and the aspect ratio or diameter of the nanowires in the network. Indeed, no correlation between the required fitting factor and either the aspect ratio or diameter of the nanowires was observed, making a prediction of the performance of nanowire systems by this method impossible, and requiring the experimental characterisation of each individual system separately. The red plot in each panel (a-f) are the results of the conversion of the density (output by the MNR simulation) of the network to a transmittance value by Mie theory (Eqn (4-3)). This first principles approach predicts the optical transmittance of the nanowire networks remarkably well in all cases considering the information used to describe the network. Under estimations (5-10 %) of the transmittance occur for networks in Figure 4.10(b), with an aspect ratio of 360 where the minimum electrical resistance for these samples was measured during a thermal ramp at ~ 250 °C, which could represent an optimised thermal treatment and may account for the excellent performance.^[6] For networks of aspect ratios ranging from 600–760 the MNR simulations treated by the Mie method agree within a few percentage to the experimental data, allowing for an accurate prediction of these networks by first principles simulation, an important result for the development of a materials-by-design approach to metallic nanowire networks. For extremely high aspect ratio systems, the agreement between the Mie treated MNR data and the experimental data breaks down. It is also difficult to simulate these ultra-high aspect ratio systems as the increase in network size causes a large amount of additional junctions which increases memory and processor use. These results show the predictive strength of the Mie treated MNR data for Ag nanowire networks.

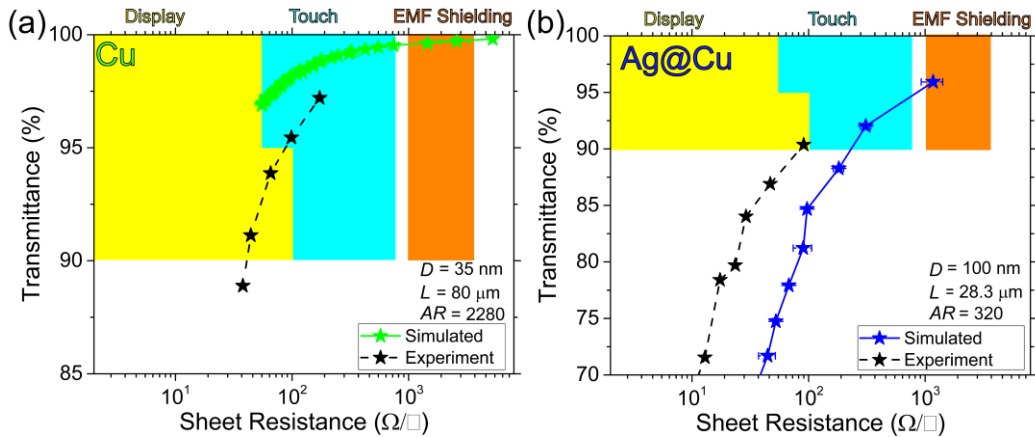


FIGURE 4.11. (a-b) Simulated transmission vs sheet resistance plot for Cu and Cu@Ag nanowire networks using the MNR and Mie approach. Regions of the plot are coloured corresponding to their transparent conductor application specifications, yellow is for display applications, blue for touch, and orange for EMF shielding. In each plot MNR simulation data is shown as a coloured star, experimental data from the published works appears as the black star and dashed line for for Cu ($L/D = 2280$ ^[41]) and Cu@Ag ($L/D = 320$ ^[42]).

A similar method was used to computationally predict the optoelectronic performances of Cu and Cu@Ag nanowire networks. Networks composed of these nanowires were simulated with the MNR method and Mie theory. The results of the MNR simulations and comparison with nanowire network data of the same aspect ratio from literature reports are presented in Figure 4.11. The green stars displayed in Figure 4.11(a) represent the average transmittance versus sheet resistance from 10 MNR simulations of Cu nanowires (200 μm distance between the electrodes, $\rho = 20.1 \text{ n}\Omega\text{m}^{-1}$ and $R_{\text{jxn}} = 205.7 \Omega$) with an aspect ratio of 2280 ($D = 35 \text{ nm}$, $L = 80 \mu\text{m}$).^[41] The black stars represent the experimental data reported in the manuscript above. The MNR density to transmittance conversion by the Mie method does not agree well with the reported experimental data. This could be due to the Cu oxide coating of the nanowires which is not considered in this iteration of the Mie treatment, the MNR simulations also only consider a single aspect ratio and perfectly rigid rods; the flexibility of such ultra-high aspect ratio systems and a large dispersion in wire lengths could contribute to the overestimation of this model, further work is certainly needed to account for these variations. Cu@Ag nanowire networks were also simulated using the MNR model (60 μm distance between the electrodes, $\rho = 30.4 \text{ n}\Omega\text{m}^{-1}$ and $R_{\text{jxn}} = 424 \Omega$) with an aspect ratio of 320 ($D = 100 \text{ nm}$, $L = 28.3 \mu\text{m}$).^[40] Experimental data taken from reported works are plotted as solid black stars in Figure 4.11(b), with the

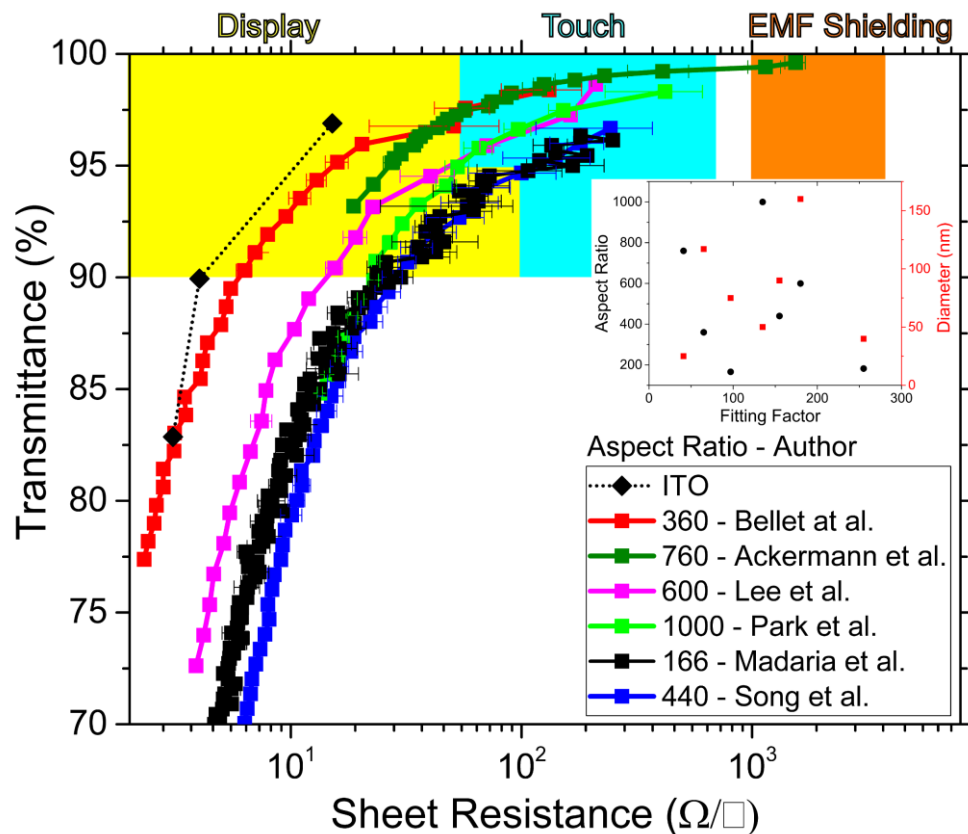


FIGURE 4.12. A combined plot of the simulated transmission vs sheet resistance values for Ag nanowire networks simulated by the MNR model and fit by the linear method, and ITO. Regions of the plot are coloured corresponding to their transparent conductor application specifications, yellow is for display applications, blue for touch, and orange for electromotive force (EMF) shielding. The inset graph shows the lack of correlation between the aspect ratio and diameter on the fitting factor used in each case.

MNR simulations plotted as the blue stars. The simulated data follows the same trend as the experimental results, however the model predicts much lower optoelectronic performance.

Figure 4.12 displays a combined graph of all the literature inspired simulations by the MNR and fit by the linear method to compare all the Ag nanowire network systems. The results show Ag nanowires at an aspect ratio of 360 achieving optoelectronic values very close to the performance of ITO (represented by the black diamonds and dotted line) for display applications.^[43] These results demonstrate that in practise, higher aspect ratios do not translate to higher optoelectronic performances. This disparity could be due to a number of factors; the poly-disperse distributions of nanowire lengths and diameters in high-aspect ratio systems, increased curvature of high-aspect ratio nanowires resulting in a network composed of objects behaving more

like flexible filaments than rigid rods,^[41] or the optimised thermal treatment used in the processing the 360 aspect ratio network.^[6] The lack of correlation between the fitting factor used to translate the density to transmittance makes it impossible to describe a predictive model based on this method. The Mie theory approach currently represents the best way to predict the performance ab initio.

Modelling metallic nanowire networks can be used to screen materials and systems highlighting that they are inherently suitable, or unsuitable for certain applications, though all the Ag nanowire systems investigated are capable of reaching the industry specified performances for display, touch and EMF shielding. The MNR model allows for a material-by-design approach, by adjusting the aspect ratio, and material specific electrical properties it is possible for metallic nanowire networks to be designed for specific applications. Further work is necessary to fully optimize the post-processing conditions to realise the highest performing films and determine a coated cylinder solution of the Mie model for material systems which are currently poorly described such as Cu and Cu@Ag. Once these aspects are considered, the computational simulations can aid with material design. This is critical as some nanowire systems may be inherently better suited for certain applications over others, either due to their electrical and optical performances, stability in certain conditions, or price.

4.5 Conclusions

This chapter has presented methods for fabricating isolated Ag nanowire networks, topographical replicas of these networks were made in a virtual space by digitising the coordinates of each nanowire to simulate the networks electrical properties more accurately. A multi-nodal representation method was employed which not only accounted for the junction resistance component of the sheet resistance but also determined the ‘skeletal’ material resistance of the network, which represents an ultimate performance limit for the network. By varying the average R_{jxn} and aligning the simulated sheet resistance with the experimentally measured sheet resistance, a good agreement of the R_{jxn} values measured in chapter 3 for Ag nanowires was achieved. The deconvolution of material and junction resistance allows for a deeper

analysis of the network to be performed; it also allows the model to be flexible to materials other than Ag.

Using the MNR model and the electrical properties measured in chapter 3; Ag, Cu and Cu@Ag nanowire networks were simulated with aspect ratios inspired by the literature values. To relate the density to an optical transmittance and enable to comparison of simulated and experimental results, an optical model based on Mie light scattering was utilised to calculate the optical transmittance of the metallic nanowire networks with respect to their geometrical aspect ratio and area coverage. This first principles approach which depends on Ohm's law, Kirchhoff's system of equations, experimentally measured resistivity and junction resistance values. Simulated nanowire networks accurately matched the literature reported networks over a range of Ag nanowire aspect ratios. It was also shown that there was no correlation between a linear fitting factor required to unite experimental and simulated data across a range of literature reported data.

The results of this work show that simulation of metallic nanowire networks is a viable approach for exploring the potential applications of a range of materials and guiding the synthesis of systems for specific needs. Metallic nanowire networks are well suited as replacements for ITO in a wide variety of transparent conducting applications. These results represent a step towards a materials-by-design approach for transparent conductor applications using metallic nanowire networks.

4.6 References

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5

THE MEMRISTIVE BEHAVIOURS OF TiO₂ NANOWIRES

In Chapter 4, the fundamental material properties and potential of metallic nanowire systems for transparent conductor applications were investigated. The focus of this chapter is semiconducting nanowires. Specifically, we look to exploit the rich electrochemistry and reactivity of TiO₂ nanowires, a material which has been the subject of much research since it was shown to possess memristive responses. The chapter will begin with a brief motivation of memristive systems followed by device fabrication methods. The results of this chapter show that TiO₂ nanowires display a memristive behaviour, which can be programmed to result in multiple memory levels. Furthermore, single TiO₂ nanowires display a unique time-correlated response to heterogeneous stimuli. These qualities make TiO₂ nanowires a prime candidate for smart-sensors and neuromorphic type devices. My original contribution to knowledge in this chapter is the investigation of the forming voltage and scaling of the current response of a single nanowire with respect to the channel length. The effect of Ag electrodes on the resistive switching behaviours, the continued development of single TiO₂ nanowires as a multi memory system with 6 and 11 level memory states demonstrated, and the characterisation of time-correlated voltage and optical stimuli for which part of the work presented has been published in the journal *Advanced Electronic Materials*.^[1]

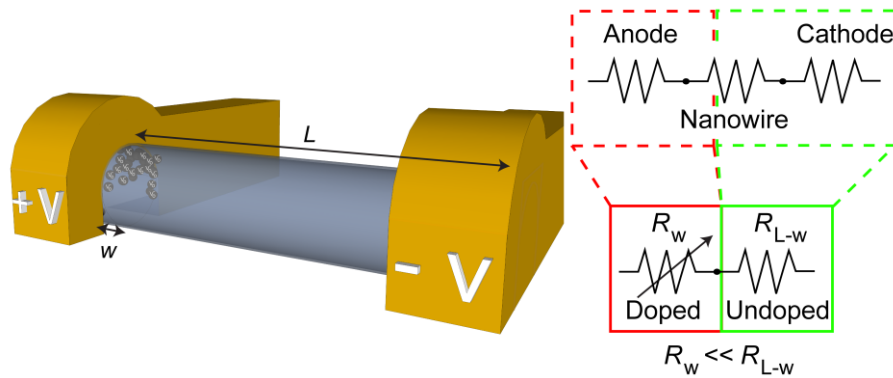


FIGURE 5.1. A schematic of the typical nanowire device structure used in this work, a single TiO₂ nanowire contacted with two Au electrodes. The two regions within the device are described by a variable resistor which accounts for the very limited doped region (shown as the black spheres at the nanowire/electrode interface), which has a much lower resistance relative to the undoped region. As the nanowire is electrically stressed, the width of the doped region increases or decreases depending on the polarity of the bias applied. This creates a dynamic response to the applied bias.

5.1 Motivation

TiO₂ has been the focus of much research since it was shown by Strukov et al.^[2] to display the qualities of the proposed fourth fundamental circuit element, the memristor^[3] (short for memory resistor). As discussed in chapter 1, the memristor is a simple two-terminal element which has many interesting and valuable properties. The most desirable quality being the nonlinear relationship that the memristance (M) provides between charge (q) and magnetic flux (Φ). This results in a two-terminal non-volatile cell well suited for high-density memory applications. The signature of a memristive system is a pinched hysteretic I-V response which displays a continuum of resistance states rather than a binary behaviour. This inherently makes a memristor suitable for reconfigurable logic operations.^[4] Memristors are regarded as a promising solution for physically emulating biological synapses and facilitating hardware implementations of neuromorphic computing.^[5] Memristive devices also have the potential for breakthroughs in memory, logic and sensing applications.^[4] The approach used to realise devices with memristive behaviour is typically a metal-oxide-metal structure which displays a hysteretic current-voltage response due to the action of charged mobile dopants within the active (oxide) layer.^[6-8] In the literature, the majority of memristive systems are constructed from planar cross-bar style memory cells, where the nanoscale-film of active material is sandwiched between two metal electrodes.^[9]

In this work, a memristive system is constructed by contacting a semiconducting TiO₂ nanowire with two metal electrodes as seen in Figure 5.1. Three elements comprise the resistance of the two-terminal nanowire device, the Schottky barriers which form at the two metal/semiconductor interfaces and the nanowire between them. This configuration can be described by a coupled variable-resistor model. The variable-resistor arises from the dependence on the concentration of dopants in the region around the anode (which is a function of the total history of the applied voltage), and the undoped region of the nanowire plus the cathode. The conduction mechanism of TiO₂ nanowires will be provided later in the chapter.

5.2 Fabrication of TiO₂ Nanowire Devices

TiO₂ nanowires were purchased from EMFUTUR,^[10] as 50 nm in diameter and 5-10 μm in length. TEM and selected-area electron diffraction (SAED) patterns display the uniform single crystalline anatase phase of the TiO₂ nanowires used in this work (Figure 5.3).^[11] Nanowires were received as a dry white powder; to disperse the wires in solution approximately 15 mg of powder was added to 10 ml of IPA. The solution was shaken by hand for (5-10 mins) followed by sonication at 37 kHz and 80 kHz (580 W) for 2 mins each. UV lithography was used to pre-pattern the Si substrate with electrical contacts in the ‘Cryomask’ pattern. The large electrical contacts consisted of thermally evaporated Ti-Au to a thickness of 5 and 25 nm respectively. The electrical contacting procedure is shown in Figure 5.2. The nanowire IPA dispersion was dropcast onto the pre-patterned Si substrate; suitable wires were located by optical microscopy, such as the wire highlighted by the yellow oval in Figure 5.2(a). Electrical contacts were drawn to the nanowire in the Raith software using the image overlay method described in chapter 2 (Figure 5.2(b)). For Au contacted devices the contacts were exposed using EBL and metallised with Au-Al or Au-Ni contacts to a thickness of 30 and 100 nm for both processes respectively, for Ag contacted devices Ag-Ni to a thickness of 100-100 nm was used. The false coloured SEM image in Figure 5.2(c) and (d) shows a single TiO₂ nanowire contacted with multiple Au-Ni electrodes. Au was chosen as the primary layer to contact the nanowire with a less precious metal chosen to ensure good electrical connection around the wire. A further discussion of the choice of electrode metal will be presented in section 5.5

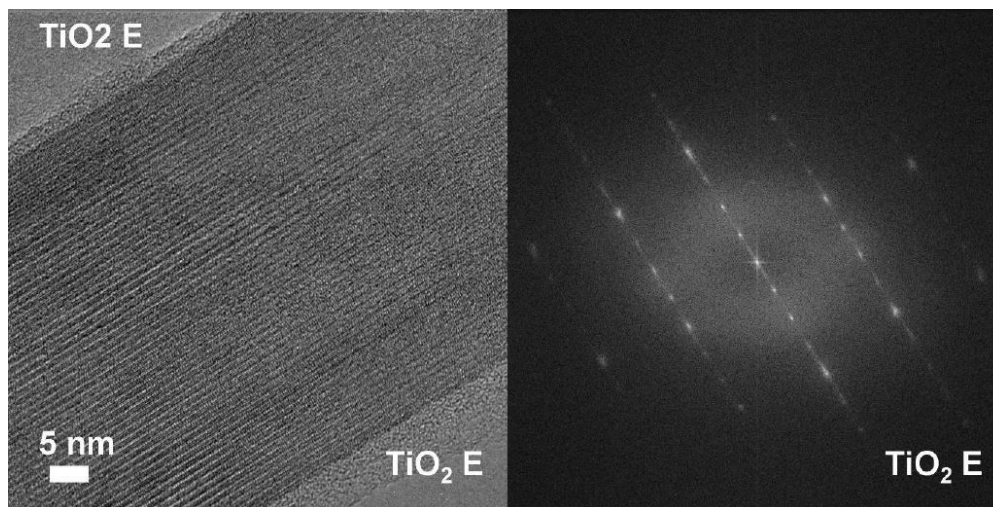


FIGURE 5.3. TEM and FFT images of TiO₂ nanowires purchased from EMFUTUR. The crystalline nature of the nanowires was observed under HR-TEM and confirmed using diffraction. [11]

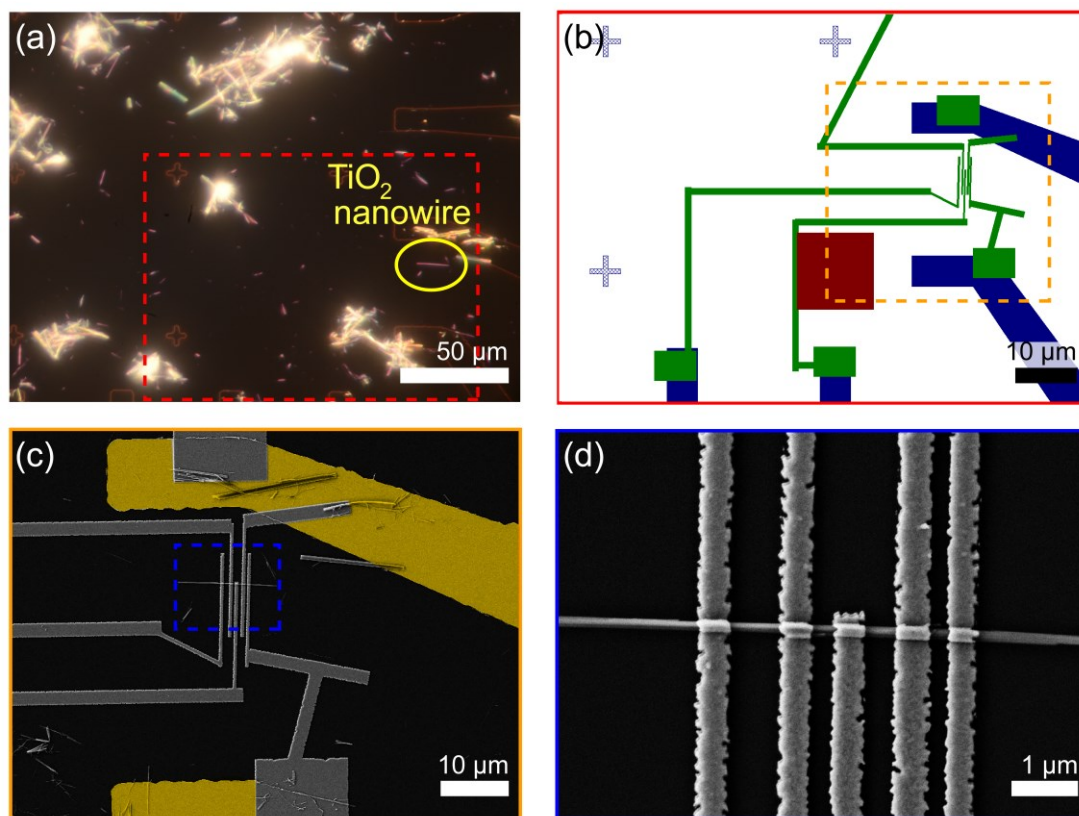


FIGURE 5.2. Electrical contacting of single TiO₂ nanowires. (a) Optical image of nanowires dropcast onto the surface of pre-patterned Si substrates, suitable candidates are located using optical microscopy. (b) Screen capture of EBL designs drawn to the chosen nanowire in the Raith computer aided drawing software. (c) False coloured SEM image after exposure, development and metallisation of the EBL defined contacts. (d) Close-up of the region bounded by the dashed blue box in (c) with five electrical contacts made to the nanowire.

5.3 Electrical Measurements

2-probe electrical measurements were performed on the single nanowire devices using the Keithley 4200-SCS parameter analyser described in chapter 2. Electrical measurements were typically conducted at a rate of 0.25 V/s unless otherwise specified. This section will describe the dynamic memristive responses of TiO₂ single nanowire devices with Au contacts.

5.3.1 Dynamic Current Response of Two Terminal TiO₂ Nanowires

The high resistivity of TiO₂ nanowires makes realisation of TiO₂ nanowire networks impractical with extremely large voltages (>50 V) required to drive a small current response (nA).^[11] The focus of this work will be on single wire behaviour. Each device tested in this work consisted of a single crystal anatase phase TiO₂ nanowire contacted with EBL defined electrodes. In comparison to thin-film memory cells, the nanowire device is simpler in its construction; thin-film memory cells typically require one metal patterning step for the bottom electrodes, a TiO₂ deposition step, which usually includes an oxygen deficient interface and a second metal patterning step for the top electrodes.^[12-14] The oxygen deficient TiO₂ is necessary to create an asymmetry in the device. Due to the symmetric construction of the nanowire devices, asymmetry was introduced through an electrical forming step.

In the pristine state, the nanowire device is a poor conductor, with typical resistances of $\sim 10^{12} \Omega$, this can be seen in the I-V response shown by the orange curve in Figure 5.4(a) the current onset occurs at 9 V and only a small hysteretic loop peaking at 11 nA. ReRAM cells often need an electroforming step (short: forming) step before their first write/read operation. The forming step involves priming the device and ensures a more reproducible response. The forming step is of particular importance in memristive systems where the history dependence of the device plays a major role in the subsequent electrical response. For TiO₂ nanowires, the forming step involves holding a +10 V bias for a long time to saturate the current response of the system (typically 1000 s). The I-V response post electroforming is shown by the grey curve of Figure 5.4(a), immediately noticeable is the increased current response at 10 V (~ 40 nA), the decrease of the current onset - which now occurs at sub 2 V, and the reduction of the resistance to $\sim 10^8 \Omega$. The magnitude of the hold voltage has a profound effect

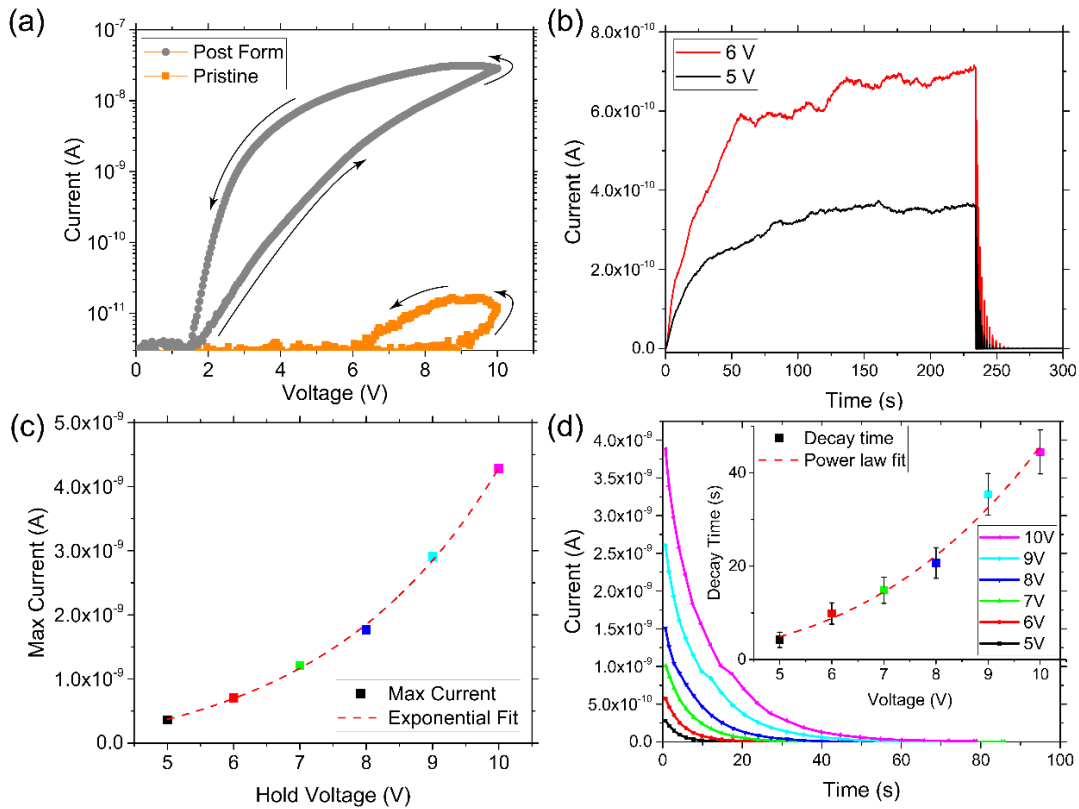


FIGURE 5.4. The electrical forming of Au contacted TiO₂ nanowires with 1 μm between the electrodes. (a) The current response of the nanowire in a pristine state (orange trace), and after a 1000 s forming step at +10 V (grey curve). The device is over 3 orders of magnitude more conductive after forming has been applied. (b) The current response over time for a constant 5 V (black) and 6 V (red) hold for 230 s followed by 250 ms interrogation pulses at the same voltage every 3 s to measure the current decay. (c) The maximum current response from the experiment described in (b) plotted against the hold voltage, the maximum current scales exponentially with the hold voltage. (d) Rescaled plot of the pulsed interrogated after the steady voltage hold, the decay time was calculated as the time taken for the measured current to reach 100 pA, the inset plot shows a power law fit to the decay time when plotted against the magnitude of the voltage pulse.

on the maximum steady state current; this is shown in Figure 5.4(b) by the black and red curves indicating a 5 V and 6 V hold respectively. The current decay was measured using 250 ms pulses of the same voltage magnitude every 3 s; this was repeated in 1 V increments from 5 to 10 V. The maximum current measured during the voltage hold is plotted in Figure 5.4(c) and shows an exponential relationship between the hold voltage and maximum current. The measurement of the current decay over time revealed that increasing the voltage magnitude of the pulse allowed the retention time to be lengthened. The charge delivered during the 250 ms pulse every 3 s was not enough to keep the current stable even at a 10 V pulse, due to the fast relaxation of the

system. The inset of Figure 5.4(d), shows that increasing the pulse magnitude slows the decay of the system, which is well described by a power law relationship. The electroforming step temporarily changes the properties of the nanowire and electrode interface, though they relax back to its original level if the device is not sufficiently stimulated.

Without the electroforming step, the device can increase in conductance with every voltage sweep. Figure 5.5(a) shows 15 successive 0 to + 10 V sweeps, with each sweep the conductance of the device increases. Figure 5.5(b) shows that the maximum current of each sweep fits a power law description. Eventually the conductance will saturate, which is the purpose of the more efficient forming step. In the pristine state, the device is malleable, the electrical stimuli applied to the device sets the history for subsequent experiments. The increase in conductivity caused by the movement of charge in one direction can be reversed by operating the device with an opposing voltage bias as shown in Figure 5.5(b), this is prototypical memristor behaviour as described in Leon Chua's seminal paper in 1971.^[3] The conductance of the element depends on the complete history of the memristor current, TiO₂ single wires behave quite predictably, increasing in conductance (to a point) upon repeated application of a voltage stimulus. The evolving current response can be observed with repeated sweeps in the positive, or negative direction (Figure 5.5(c)). This behaviour will be exploited in section 5.4.2 by programming arbitrary digital levels onto the analogue response of the device demonstrating the ability of a single TiO₂ nanowire to hold multiple memory levels. A functionality first reported for single TiO₂ nanowires by our group.^[15]

As shown above, the single nanowire device is a relatively simple platform for investigating fundamental memristive phenomena. Parallels can be made with conventional planar, two-terminal thin-film devices except for the massive difference in the thickness of the TiO₂ layer. Thin-film devices typically have oxide layers less than 100 nm in thickness; this results in the mobile charged dopants created at one electrode to gather at the counter electrode and potentially form sub-oxide phases, this will be further discussed in section 5.4.3 . The nanowire device structure has some advantages and disadvantages when compared to thin-film cells; it effectively separates the device into two electrode regions which can be treated independently.

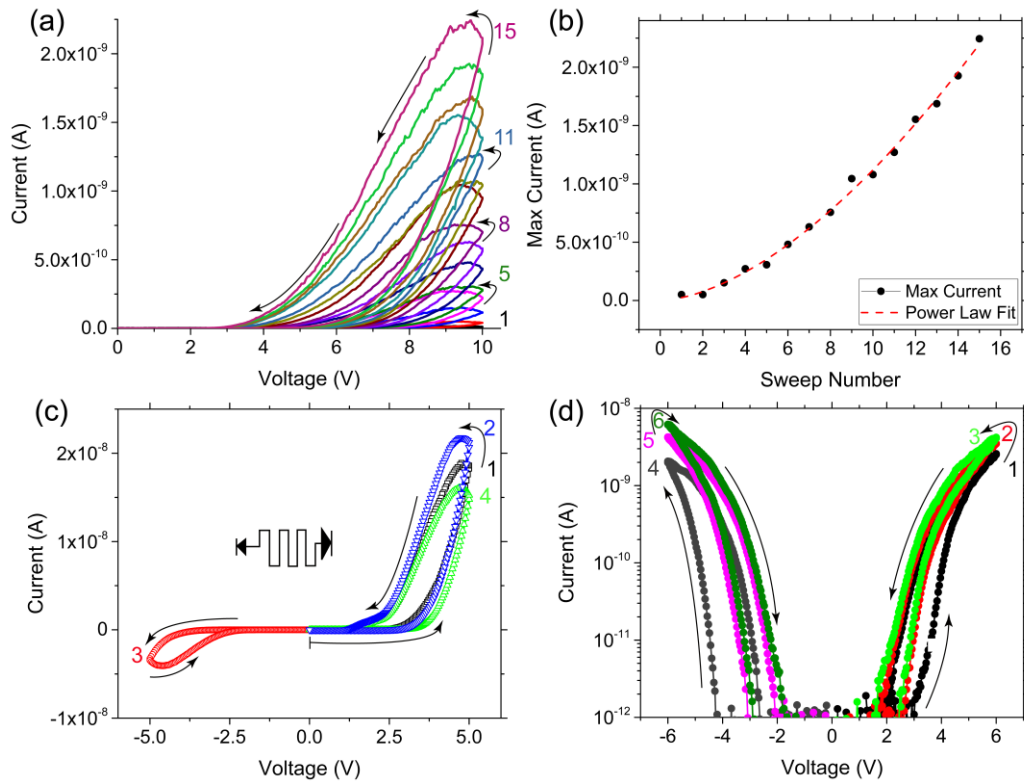


FIGURE 5.5. (a) The evolution of the current response of the nanowire to 15 consecutive positive sweeps performed directly after each other. (b) The increase in peak current is shown from (a) and follows a power law trend, this was performed on a pristine device. (c) The increase in conduction at one polarity can be decreased using opposite polarity input, sweep 2 showed in an increased response to sweep 1, however sweep 3 caused sweep 4 to be less than sweep 1. (d) Evolving current response can be seen in both directions, in positive bias, conductivity grows with each successive sweep, in the negative direction the current also grows with successive sweeps.

This allows for evolutionary behaviour of the device, but also causes the quick decay of the resistance state. The gap between the electrodes needs to be precisely controlled in the lithography step as it is directly related to the magnitude of the current response as illustrated in Figure 5.6. Devices with multiple electrodes were fabricated with separations between the electrodes ranging from 4 μm to 0.5 μm , as shown in the SEM image in Figure 5.6(a). A magnified, annotated SEM image of a second device indicates the range of electrode separations possible (Figure 5.6(b)). During the experiment, the electroforming procedure (+10 V hold, 1000 s) was applied to different electrode combinations. The electroforming curves in Figure 5.6(c) show that reducing the distance between the electrodes results in an increased current response, which scales exponentially with the channel length. The exponential scaling is shown

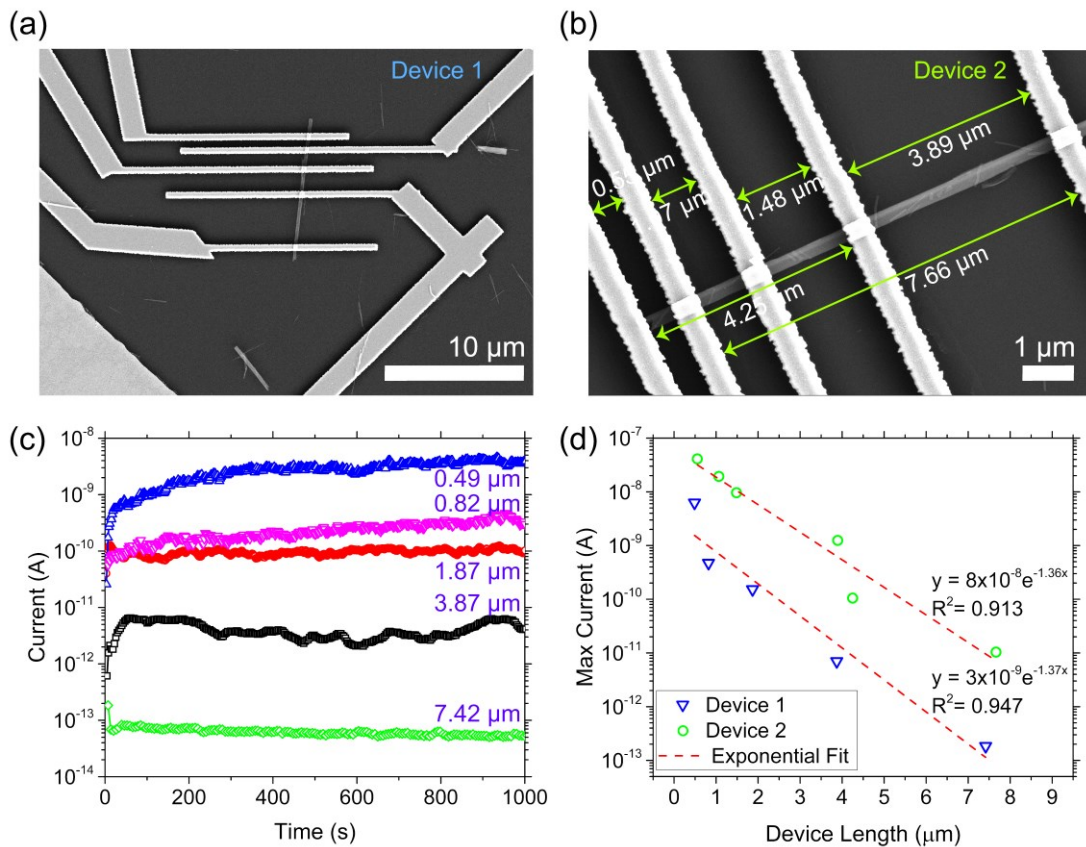


FIGURE 5.6. The current response of TiO_2 nanowires with multiple electrodes. (a) SEM image of a TiO_2 nanowire ‘device 1’ contacted with five Au electrodes. (b) SEM image of ‘device 2’ with device lengths annotated. (c) Electroforming of TiO_2 nanowire devices using a constant +10 V hold and monitoring the current response for 1000 s at various electrode separations. (d) Maximum current of each forming step vs electrode separation. An exponential fit is applied to both data sets with good agreement.

for two measured devices in Figure 5.6(d). The exponential scaling of the device conductance with length motivates short-channel devices where lower voltage operation could be exploited. The channel length affects the max current, but no difference in the device behaviour was observed for separations of 500 nm between the electrodes. The precise lithography necessary for sub 500 nm channel lengths is challenging, and the difficulty is compounded by the use of a noble metal at the nanowire interface, which prevents the use of an adhesion layer (for reasons discussed later in the chapter); this makes lift-off very difficult drastically reducing device yields.

5.4 Memristive Behaviour and Learning

Memristive systems are complicated and difficult to characterise, the hysteretic nature of the device and history dependent response requires that a protocol is established to ensure repeatable and reproducible results. This is the role of the electroforming step, to set a saturated current response from which the device may be operated. In the next subsection the control of the continuum resistance response is demonstrated with multiple memory levels which are defined through the application of positive and negative voltage pulses for single TiO₂ nanowires contacted with Au electrodes.

5.4.1 Introduction

Increased storage density is a constant goal in the development of new memory technologies. Scaling of individual memory bits requires overcoming certain fabrication and eventually physical limitations. Multilevel storage is another effective way to increase the storage density. Much research has been carried out on the possibility of multilevel storage for many kinds of memory including RRAM^[16] and phase change random-access memory (PRAM).^[17] Multilevel storage requires that the device can hold and distinguish between more than two resistance states. In RRAM this has been achieved through the use of external compliance values to limit the compliance current.^[16] While these results suggest multilevel feasibility, it is a cumbersome implementation which requires additional circuitry and current compliance selectors. Our group has previously demonstrated that a single TiO₂ nanowire can operate at six distinct memory levels using a combination of 2.5 s positive and negative voltage pulses.^[15] In this section, six-level memory is demonstrated with lower operating voltages and shorter pulse durations than previously reported. The feasibility of eleven-level memory is also explored.

5.4.2 Multilevel Memory

The key to the operation of the multilevel memory in TiO₂ nanowires is the control over the continuum of resistance states that exist in the memristive system. As previously discussed, the memristor is an element which evolves its resistance depending on the history of current flow. A single positive voltage pulse can augment the device to a lower resistance state, with a negative voltage pulse returning the device to its original resistance level. Through the use of multiple positive pulses, it is

possible to define arbitrary resistance levels demonstrating multiple memory operations, the ability to reset, or step back the resistance of the forward channel by applying a reverse bias pulse is not available or has not been demonstrated in a conventional two-terminal thin-film memristor to date.^[15]

Figure 5.7(a) shows the current response to a pulsing segment involving five set pulses (+4 V) and one reset pulse (-4 V) with a pulse duration of 100 ms. The status of the multilevel memory level can be read by the application of a sub threshold pulse sufficient to produce a measurable current but not capable of modifying the resistance of the device. Figure 5.7(b) is a plot of the relative value of the current level as a fraction of the highest current level. This allows the separation of the resistance levels to be seen; the six-level memory arises from the five defined resistance states and the single off state. The evolution of the current response can be considered in the first 15 pulse sets as the relative levels increases to a saturated state. Beyond this, well-defined memory levels are observed with the relative separation between these levels remaining unchanged. It is possible to change the number of memory levels by altering the voltage pulse height or width before the reset pulse. Figure 5.7(c) shows that by increasing the voltage pulse to +5 V and the pulse width to 130 ms, eleven-level memory operation can be demonstrated. The relative value of each level shows separation, but the saturation of all levels is not readily achieved. These results build upon the work previously reported by our group^[15] and demonstrates a significant reduction in power and increase of speed. In the original work, six-level memory was demonstrated using 2.5 s pulse widths and pulse heights of +/- 7.5 V for set/reset pulses. Decreasing the separation between the electrodes from 2 μm to 1 μm has resulted in 19 times increase in speed and a 1.8 times decrease in operating voltages. By altering the pulse height and width, eleven-level memory is demonstrated. The operation of such multilevel memory devices would require the development of algorithms to specifically tailor pulse heights and widths for maximum fidelity and precise control of the memory levels. Another challenge for the operation of these devices includes determining a read voltage which does not perturb the memory level. Each memory level is also not stable for an indefinite amount of time (less than a 30 seconds) due to thermodynamic instability and resistance drift as previously shown.

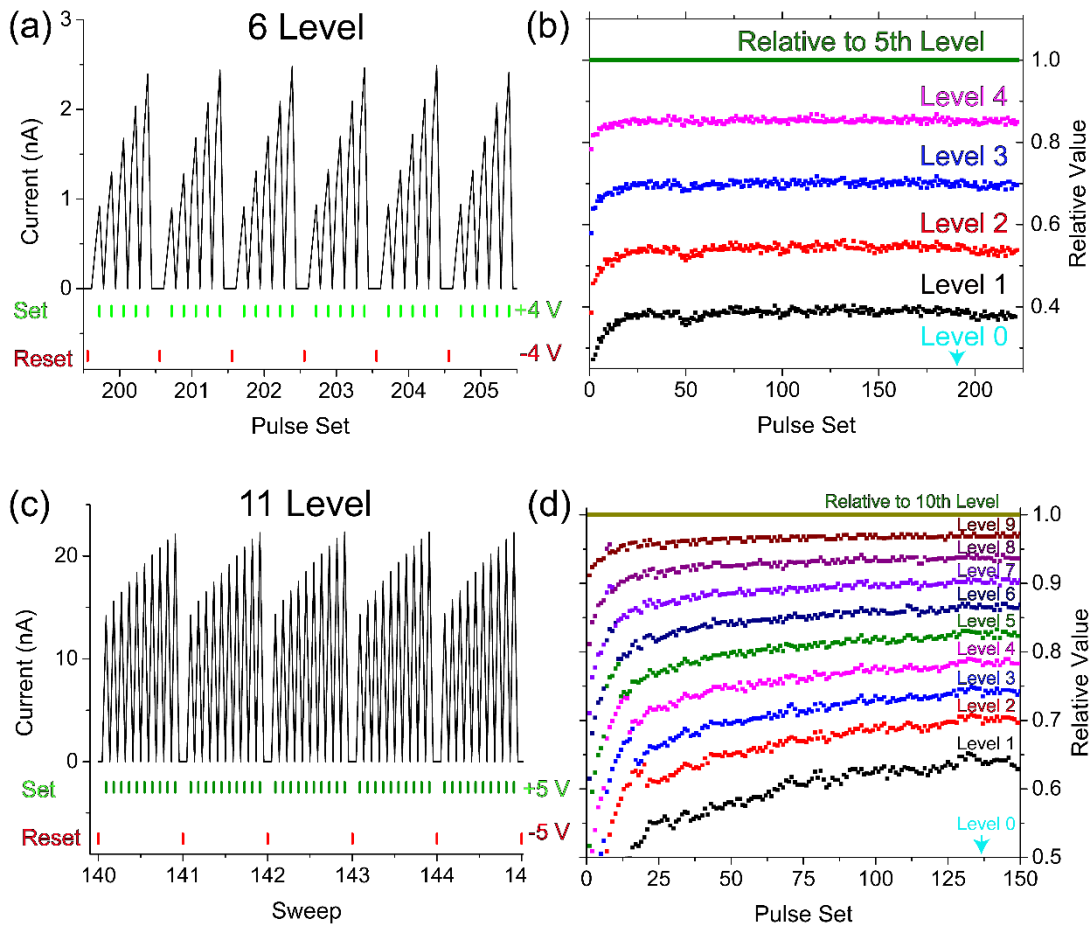
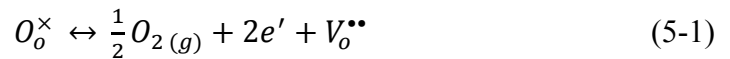


FIGURE 5.7. The programming of multiple memory levels in a two-terminal TiO₂ nanowire with 1 μm separation between electrical contacts. (a) The conductance level can be incrementally increased using five successive 100 ms pulse at a bias level of 4 V, the -4 V pulse resets the device and returns the memory level to the baseline. (b) The ratio between the current response between each pulse allows the arbitrary definition of digital memory to the analogue system. (c) With ten applications of a 130 ms +5 V eleven-level memory can be demonstrated. (d) The fidelity between levels is decreased. Level zero is defined as the zero-relative value state, which is not shown on the plots.

In the current form, such a device is unsuitable for non-volatile memory applications. However, the controllable change in resistance levels and short-term retention of multiple memory levels could be useful in hardware implementations of neuromorphic inspired systems, where through the continued application of certain stimuli the response is strengthened, and specific behaviours are encouraged. After a discussion on the conduction mechanism itself, this will be the inspiration for the next section, where single TiO₂ nanowires are interrogated with a combination of voltage and optical stimuli.

5.4.3 Conduction Mechanism

The single wire structure is a unique way of exploring the memristive properties when compared to two-terminal thin-film devices. The relatively large separation between the contacts allows for the rich memristive response. The resistance changes at or around the interface are presumed to control the electrical behaviours as it is unlikely that a conducting filament can bridge the two electrodes. The mechanism of resistive switching and memristance has been widely debated in the literature.^[18] Here we propose an ionic and Schottky barrier dominated mechanism due to the observed operation of the Au contacted single crystalline anatase phase TiO₂ nanowires. The 5.1 eV work function of the Au electrodes form a Schottky barrier with the wide bandgap TiO₂ nanowire; this initial state is shown schematically in Figure 5.8(a). The single crystal anatase phase TiO₂ wire has few defect generated carriers to screen the Schottky barrier and the band bending reflects the Schottky barrier height (ϕ). The low-doped metal-semiconductor contact is initially blocking or rectifying,^[19] which explains the low-conductivity and large voltages required for current rectification in pristine devices. On the application of a positive bias oxidation of lattice oxygen O_o^x can form positively charged oxygen vacancies V_o^{••} by the following reaction,^[15, 20]



It has been well established that oxygen vacancies readily form at the interface between TiO₂ and positively biased noble metal contacts.^[6, 19-21] Along with the creation of oxygen vacancies Ti interstitials could also be present. Oxygen vacancies act like n-type dopants with shallow donor states below the conduction band of TiO₂. The generation of n-type dopants transforms the interface of the wide bandgap semiconductor into a more electrically conductive doped semiconductor.^[22] Not only does the production of the oxygen vacancies transfer two free electrons into the conduction band, the shallow traps that are generated shifts the Fermi energy closer to the bottom of the TiO₂ conduction band. The overall effect of this is to reduce the Schottky barrier height and width in the developed state shown schematically in Figure 5.8(b). The movement of positively charged oxygen vacancies created at the anode

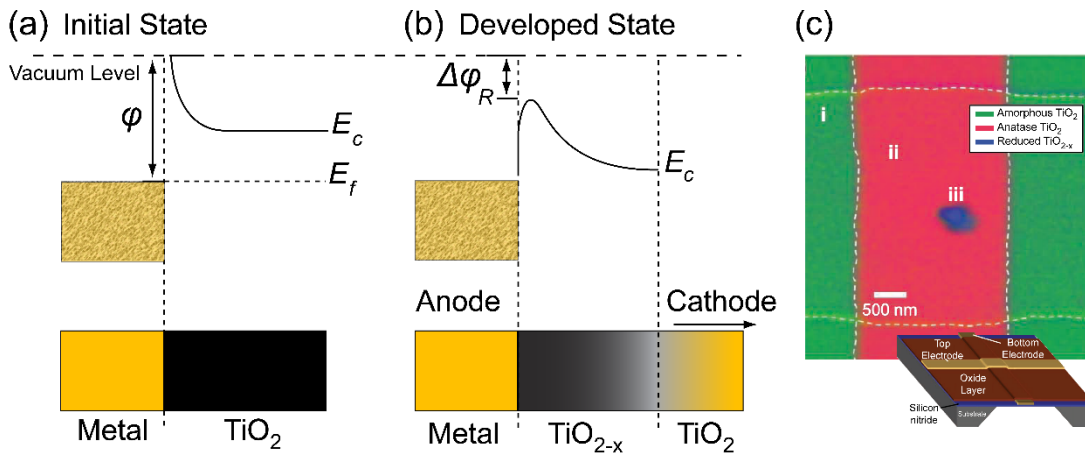


FIGURE 5.8. Energy band alignment of and Au contacted TiO₂ nanowire in the initial and electrically developed state. (a) A Schottky barrier with height ϕ forms at the metal semiconductor interface. (b) During electrical stressing, a population of oxygen vacancies are formed acting as n-type dopants and transforming the wide bandgap oxide to a more electrically conductive oxide at the interface, this lowers the Schottky barrier height by $\Delta\phi_R$ increasing charge injection and the conductance of the device. The positively charge vacancies can drift toward the cathode, allowing for the dynamic behaviour. Image adapted from Curtis et al.^[15] (c) Chemical and structural mapping of three phases of titanium oxide. The colour of each pixel is derived from Ti L_{2,3} x-ray absorption spectrum, from Strachan et al.^[26]

will naturally drift towards the cathode. A critical concentration of oxygen vacancies can create auto-doped phases which are metallically conducting for TiO_(2-x) for $x > 1.5$.^[18] The formation of Ti_nO_{2n-1} regions have been observed and postulated as the conducting channel inside TiO₂ ReRAM devices.^[23-25] Using spatially-resolved x-ray absorption spectroscopy Strachan et al. could observe a 200 x 300 nm region of a stoichiometrically reduced sub-oxide, or the equivalently mixed valence composition of Ti⁺³ and Ti⁺⁴ within a region of anatase phase TiO₂ (Figure 5.8(c)).^[26] Within this region, a strongly diffracting single crystal of Ti₄O₇ with a diameter of less than 100 nm was observed. Ti₄O₇ is a homologous series of stable reduced TiO₂ phases which are commonly known as Magnéli phases and possess a metallic conductivity at room temperature.^[26] In TiO₂ nanowires, the formation of these phases could occur at the interface where the concentration of oxygen vacancies are quite high, or other regions along the wire as the Magnéli phases are more thermodynamically stable than a distribution of vacancies spread throughout the material.^[27]

The saturation of the current response during the electroforming step (c.f Figure 5.6(c)) likely represents a balance between the rate of vacancy generation at the

anodic electrode and the rate of vacancy drift towards the cathode. As shown, the devices are highly dependent on the voltage bias polarity, reversing the polarity has the effect of increasing the measured resistance. The application of a short negative pulse to a positively formed device causes the reverse of reaction (5-1) annihilating the oxygen vacancies near the contact region, and creating a depletion region at the electron injecting interface.

5.4.4 Correlated Voltage and Light Stimuli

So far, the method used for interrogating and characterising the memristive TiO_2 system has been through DC voltage experiments. Apart from the huge interest in TiO_2 as a memristive system, TiO_2 is an important photocatalytic material. TiO_2 is the most investigated single-crystalline system in the surface science of metal oxides. It exists as two main polymorphs, anatase and rutile, each with different properties and photocatalytic properties.^[28] Generally, anatase is more active than rutile; this is believed to be due to the bulk transport of excitons to the surface, it has been shown that the charge carriers excited deeper in the bulk contribute to the surface reactions in anatase form.^[29] With a band gap of 3.0 eV (413 nm) for the rutile phase and 3.2 eV (387 nm) for the anatase phase, TiO_2 is considered a wide indirect band gap semiconductor.^[30]

TiO_2 nanowire devices were fabricated with Au contacts as described in section 5.2, wires were electroformed at +10 V for 1000 s before electrical measurement. UV radiation of a single nanowire device was performed using the laser set up described in section 2.4.2. To briefly recap the setup, a 405 nm wavelength 4.5 mW (0.5 mW at the wire) laser was integrated into the optical turret of the Karl Suss PM-8 probe table. The laser could be focused to a 470-490 nm full width half maximum spot size and the exposure of the beam onto the sample was controlled using a mechanical shutter operated by a trigger from the Keithley 4200-SCS.

During optical experiments, a steady 2 V potential was held across the device so that a photo induced current response could be measured, voltage pulses were applied on top of this. Figure 5.9 shows the importance of simultaneity in the voltage and optical stimulus, using an alternating pulse train of voltage (0.75 V) and optical stimuli, our group has shown that for 20 s and 5 s gap between the two inputs only a weak augmentation of the device conductance was observed(Figure 5.9(a) and (b)).

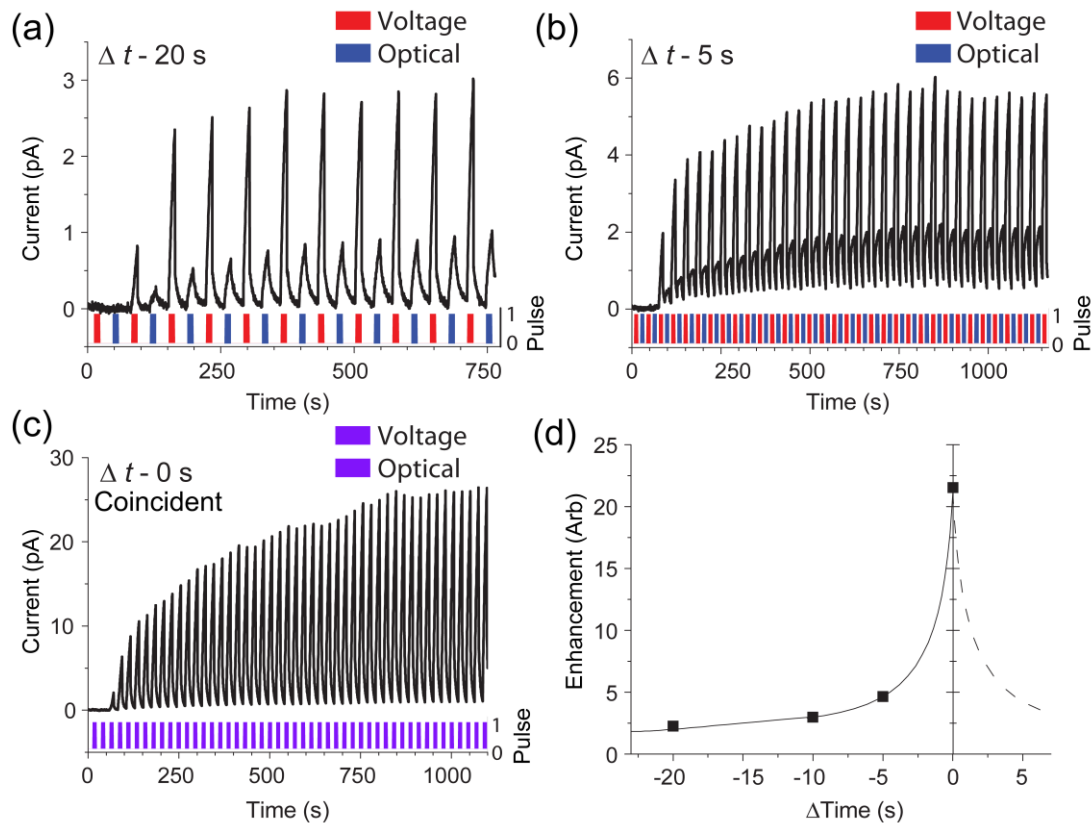


FIGURE 5.9. The simultaneity of the optical and voltage pulse is critical to the observed enhancement. A 2 V holding bias was applied throughout all experiments, voltage (red, 0.75 V) and optical (blue) pulses were separated by (a) 20, (b) 5 and (c) 0 s, for which the device shows maximum augmentation and an increase in conductivity for each of the 50 pulses. (d) A graph illustrating the pseudo-plasticity strengthening analogous to STDP as the separation between optical and voltage pulses is decreased. Figure adapted from O’Kelly et al.^[1]

When the two pulses (optical and voltage) are coincident on the nanowire, a huge nonlinear response in the current is recorded. Moreover the conductance of the device evolves with each coincident pulse for over 50 pulses (Figure 5.9(c)). The enhancement of the current response with respect to the separation between the two heterogeneous stimuli can be seen in Figure 5.9(d). The time correlated enhancement and strengthening response is particularly interesting and bears some similarities to spike-timing-dependent-plasticity (STDP), a biological process which adjusts the strengths of the connections between neurons in the brain based on the relative timing of particular neurons input and output nerve impulses (spikes).^[31] Unlike biological systems, no inhibition is observed when the order of the heterogeneous stimuli is reversed. The potentiation and depression due to homogeneous voltage pulses was shown earlier in this chapter for single TiO₂ nanowires, and allowed the operation of

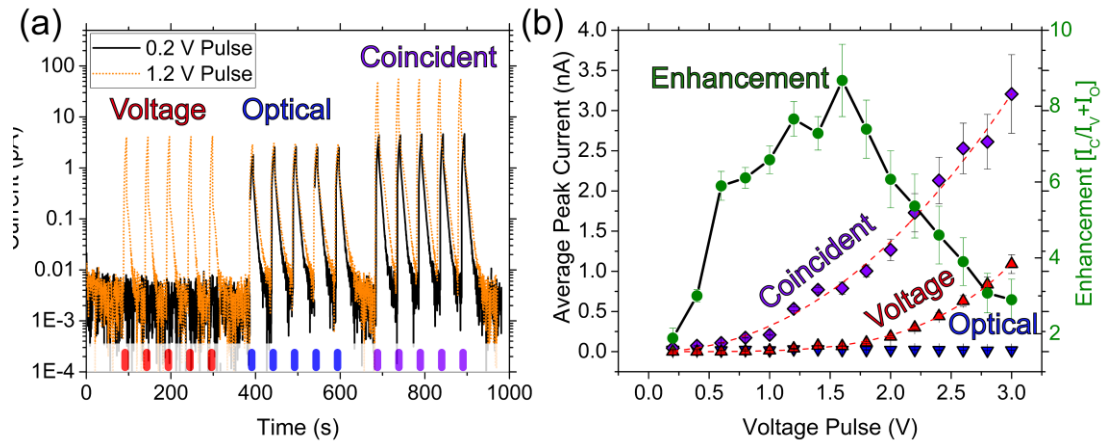


FIGURE 5.10. (a) Current response from five separate heterogeneous voltage and optical pulses followed by five coincident (coupled voltage and optical pulses). A 2 V hold was applied throughout the experiment, the graph shows two different voltage pulse levels, 0.2 V in black and 1.2 V in orange. The magnitude of the current response for the coincident stimuli is far larger than the sum of the individual optical and voltage responses. (b) The enhancement of the coincident response with respect to an increasing voltage pulse. The average peak current taken from the five pulses is plotted on the left vertical axis, and shows how optical response remains the same, but voltage and coincident responses increase at a power law rate. The enhancement, which is the response of the average coincident pulses divided by the summed average of the separate pulses shows a peak enhancement of 8.6 at 1.6 V.

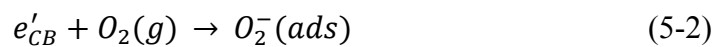
multilevel memory. The STDP phenomenon has also been previously reported for homogeneous voltage impulses in memristors.^[5, 23, 32]

It was observed that the enhancement of the correlated response could be increased by carefully choosing the magnitude of the voltage pulse stimulus. An experiment designed to maximise the enhancement of the coincident pulse is shown in Figure 5.10. Five separate voltage and optical stimuli were followed by five coincident pulses. The magnitude of the voltage pulse was varied from 0.2 to 3 V in 0.2 V increments. A complete I-t plot for 0.2 V and 1.2 V voltage pulses can be seen in Figure 5.10(a), a constant hold of 2 V was applied to the system and the pulse width was 7 s with 44 s between. Figure 5.10(b) shows the average peak current of the separate heterogeneous response as well as the enhancement of the correlated pulse. The nonlinear enhancement factor represented by the green circles was calculated by dividing the coincident current response (purple diamonds) by the sum of the separate voltage (red triangles) and optical (inverted blue triangles) pulses. Once again it is clear that the dual stimuli elicit a current response which is greater than the linear combination of the two individual pulses. The enhancement reaches a peak value of

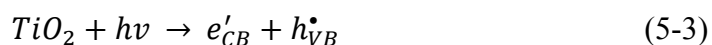
8.6 at 1.6 V, after this, the enhancement factor sharply decreases. The optical response remains stable throughout the experiment indicating good control of the laser light onto the wire. As the voltage pulse magnitude increases the current response from the separate voltage pulses also increases and reduces the effective enhancement factor. The larger voltage pulses evidently alter the conductivity of the device. The data shown is typical of the three devices measured where peak enhancement factors varied between four and eight, with voltages required to reach this augmentation ranging from 0.8 V to 1.6 V. The errors are taken from the standard deviation of the five pulses and propagated to the enhancement factor.

The action of stepping the voltage is expected to produce a small set of excess carriers at the anode. Similarly, application of UV light is thought to generate an additional set of carriers by charge separation (photogenerated electrons and holes) and oxygen vacancy generation. The charge carriers created when the coincident voltage and UV stimulus is applied are not equal to the addition of the two separate stimuli. The mechanism for the enhancement can be understood from the electrical conduction mechanism previously outlined in section 5.4.3 and the known properties of how the TiO₂ material interacts with light.^[1]

As already discussed, when TiO₂ is put in contact with Au, a Schottky barrier is formed as in Figure 5.11(a). In this configuration, a depletion region of width W_d forms. During electrical forming oxygen vacancies are generated at the TiO₂ Au interface by reaction (5-1). Figure 5.11(b) shows O₂ gas in the ambient reacting with electrons in the conduction band and resulting in the adsorption of O₂⁻ species by^[33]



The scavenging reaction has the effect of reducing the conductivity. When light falls upon a semiconductor with energy above the band gap, an electron-hole pair (exciton) will form. The photogeneration of excitons in TiO₂ follows the typical semiconductor response and is given by the following,^[33]



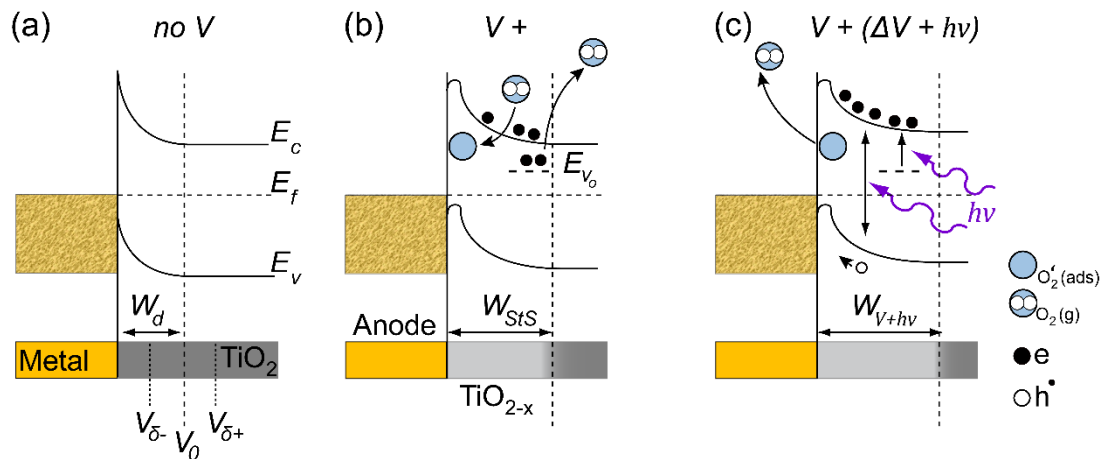


FIGURE 5.11. Schematic energy band diagrams of the Au/TiO₂ interface at: (a) No voltage bias, the depletion width W_d is defined by carriers available to screen the Schottky barrier these lose or gain electrons in response to an electric field. (b) On application of a positive bias oxygen vacancies are introduced at the metal semiconductor interface, oxygen vacancies cause shallow traps and alter the Schottky barrier height. Oxygen can also adsorb at the TiO₂ metal interface, scavenge electrons from the conduction band and further augment the barrier height. (c) Photogenerated holes may combine with and release adsorbed oxygen, increase the population of oxygen vacancies and augment conduction. Adapted from O'Kelly et al.^[1]

In general, if the photon energy is sufficient to excite an electron from the valence band to the conduction band a free electron and a free hole are generated, which can respond to the influence of electric fields present within the material. Photogenerated holes are driven upward by band bending where they are captured by the adsorbed O₂⁻ species liberating neutral O₂. The O₂ remains trapped at the Au-TiO₂ interface where it can recombine with photogenerated electrons via reaction (5-2).^[1] Repeated coincident stimuli causes a build-up of the amount of photogenerated carriers which results in the increasing current response described in Figure 5.9(c). The augmentation which is provided by the optical stimulus is short-lived and does not permanently modify the conductivity of the device. The lifetime of the associated memory effect could be prolonged by covering the device in a polymer capping layer which serves to limit the recombination of the carriers with atmospheric oxygen. The decay of the photocurrent can be extended even further by operation in vacuum.^[1, 34]

5.5 Effect of One or More Ag Electrodes

The effect of the electrode metal contacting the nanowire was investigated in the thesis of Dr O’Kelly; it was observed that Ti contacts showed visible signs of degradation or bubbling under the contact during electrical testing; while Pd electrodes had poor adhesion to the SiO₂ causing low device yields.^[11] The liberation of lattice oxygen has been shown to damage planar thin-film cells and has also been observed in 60 μm long Pt-TiO₂-Pt devices using only a 4 V bias.^[6] The fact that bubbling has not been observed for Au contacted nanowire devices has been explained by Dr O’Kelly, who suggested that the novel geometry and transverse orientation let nanowire devices ‘breathe’ by allowing the evolved oxygen gas to escape the interface. The bubbling of the Ti electrodes is ascribed to the oxidation and oxygen capture by the Ti electrodes from the TiO₂ wire underneath. Due to this reactivity, he suggested that noble metals are used, in particular pure Au contacts (80 nm) were utilised for all device fabrication.^[11] In this work, the electrical behaviour of Ag electrodes was investigated.

Ag is considered an oxidizable (soluble) or active electrode in electrochemical metallisation memories (ECM). In ECM thin-film cells TiO₂ is readily used as the insulating medium in the construction of two-terminal resistive switching, metal-insulator-metal (MIM) devices.^[35-37] So far the electrical behaviours of single crystalline TiO₂ nanowires contacted by Ag electrodes have not been reported. Presented below are the typical electrical behaviours of devices contacted with a combination of Ag-Ag, Au-Au, and Ag-Au electrodes, using the methods described previously.

In the pristine condition, the current response of the device was larger than that typically observed with Au-Au contacted nanowires, with a current response of 53 nA ($1 \times 10^8 \Omega$ resistance) observed during the first sweep shown by the black trace in Figure 5.12(a). The current response was augmented with subsequent positive voltage sweeps illustrated by the red and blue curve indicating sweeps 2 and 3 respectively and could be decreased by sourcing a negative voltage as shown by with the magenta trace of sweep 4 in the graph. The higher initial current responses could be due to the formation of a lower Schottky barrier with an Ag electrode, which has a lower work function than that of Au, the potential barrier height is a major factor in the resistive switching characteristics for planar thin-film devices as described by Kim et al.^[37]

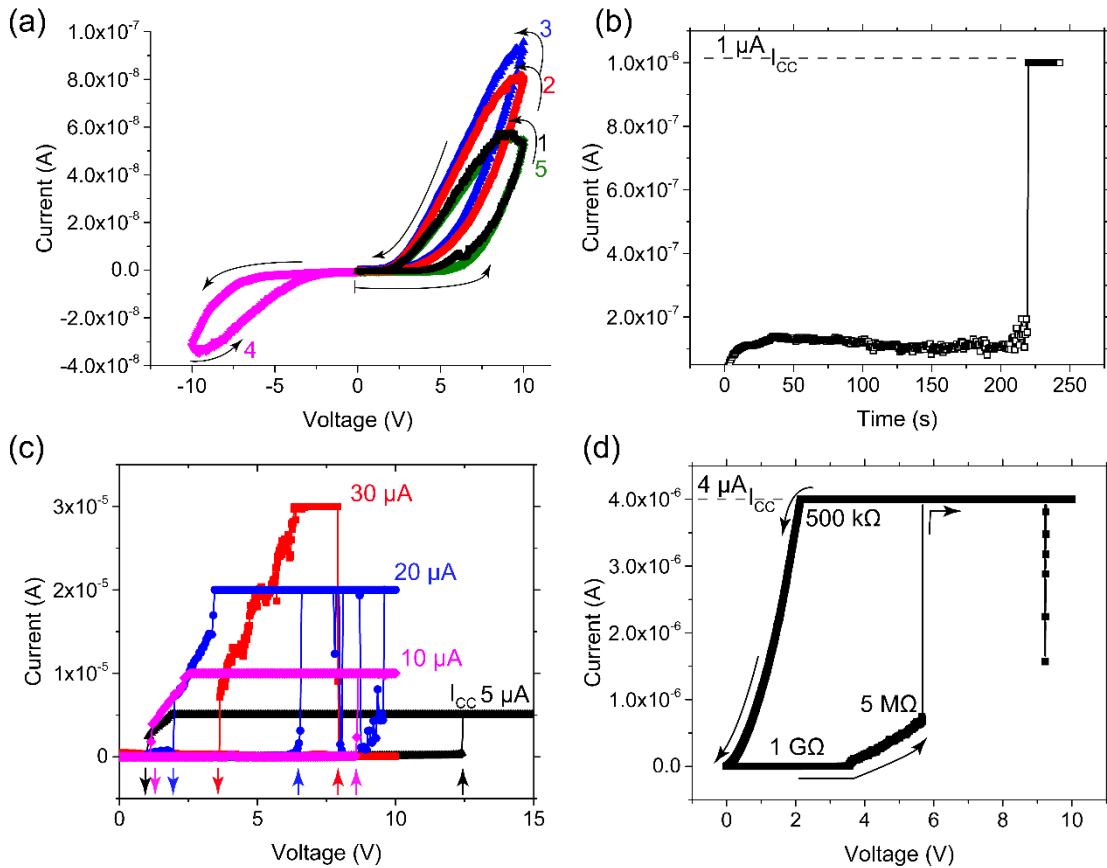


FIGURE 5.12. The electrical behaviours of a TiO₂ nanowire contacted by Ag electrodes at a separation of 2 μm. (a) Initial sweeps on a pristine wire shows typical memristive dynamic current response. (b) Electroforming shows a sudden jump from 150 nA to 1 μA (current compliance limit) at 220 s during a +10 V hold. (c) Threshold resistive switching behaviour after electroforming at increasing current compliance limits. (d) After multiple sweeps a stable resistive switch was observed, resulting in a resistance level of 500 kΩ, this low-resistance state was stable for minutes.

After interrogation of the pristine device, an electroforming step was run. A +10 V potential was held between the source and ground electrode with the current response of the nanowire monitored (Figure 5.12(b)). The current response of the nanowire was over 150 nA, quite high, but within the range previously measured for Au contacted nanowires. After 225 s, the system suddenly spiked in current and hit the 1 μA compliance restriction, reaching this limit corresponds to a resistance of 1 × 10⁶ Ω, one order of magnitude less than previously recorded with Au-Au contacts. Subsequent sweeps at increasing compliance current shown in Figure 5.12(c) as the black, magenta, blue and red I-V curves, representing current compliance limits of 5, 10, 20 and 30 μA respectively. For these experiments, a volatile threshold resistive

switching behaviour was observed in all cases. Non-volatile switching was achieved in the I-V trace presented in Figure 5.12(d), the I-V response shows an OFF resistance of $1 \times 10^9 \Omega$, decreasing to $5 \times 10^6 \Omega$ as the device gradually increases its current response to the applied voltage. At 5.9 V a resistive switching event occurs to the compliance limit of 4 μ A, resulting in a $5 \times 10^5 \Omega$ resistance, this low-resistance state showed a nonlinear response on its return from the current compliance limit to zero bias. Subsequent measurements showed that the low resistance state of 500 k Ω was not stable and decayed within 5 minutes, this type of semi-stable switch was not reproducible. Erratic threshold switching behaviours were observed for all further 12 devices which were electrically tested; no repeatable resistive switching could be demonstrated for TiO₂ nanowires contacted with Ag electrodes.

The electrical behaviours of Au contacted, and Ag contacted nanowires are seen to be very different, to capture both behaviours in a single device, individual TiO₂ nanowires were contacted with a combination of Au-Au, Ag-Ag and Au-Ag electrodes to summarise the various behaviours observed. The results of this study is shown in Figure 5.13. TiO₂ nanowires contacted with two Au electrodes demonstrate a gradually increasing hysteresis loops when interrogated with either a positive or negative voltage (Figure 5.13(a)). As previously shown, when contacted with Ag electrodes, this behaviour breaks down, and the device experiences a large abrupt change in current, rather than the smooth continuum of resistances displayed with Au contacts (Figure 5.13(b)). These contrasting behaviours indicate that the resistive switching mechanism is largely influenced by the composition of the electrode material.

When a single TiO₂ nanowire is contacted with one Au and one Ag electrode, the electrical behaviour is dependent on the voltage polarity and the electrode connected to the voltage source. When the Ag electrode is chosen as the voltage source (Figure 5.13(c)), resistive switching behaviours are seen in the positive quadrant of the I-V curve, with hysteretic loops shown during negative sweeps. The ability to operate the device in these two distinct regimes breaks down after multiple sweeps, possibly due to degradation of the wire, the reasons for which will be discussed below.

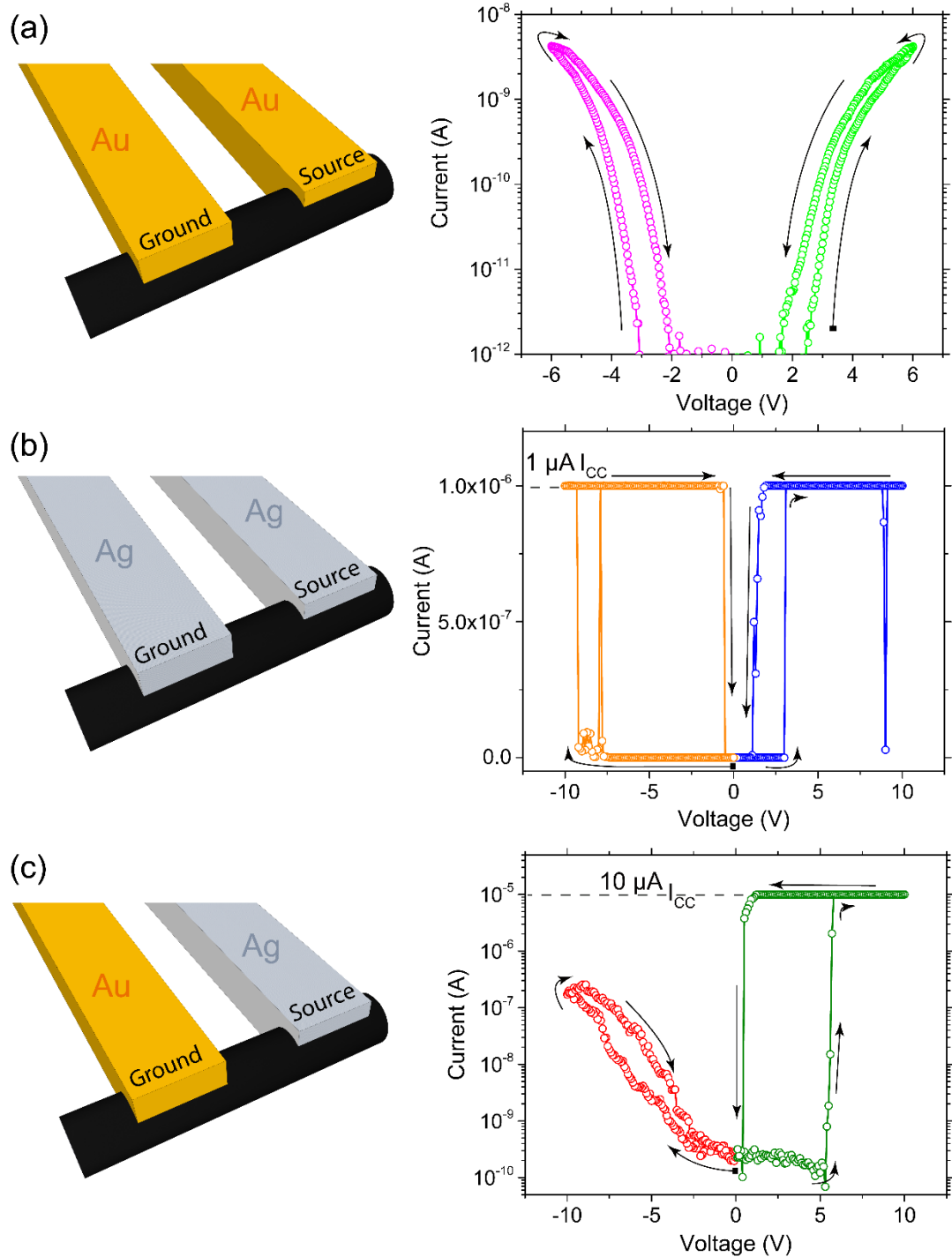


FIGURE 5.13. The electrical behaviours with Au and Ag electrode combinations (1 μm separation between electrodes). (a) Contacting with Au electrodes results in a dynamic current response, displaying a continuum of resistance levels as the current responds to the source voltage. (b) Using Ag as the contact, abrupt resistive switching is observed in both voltage polarities. (c) With mixed passive (Au) and active (Ag) electrodes, both resistive switching and nonlinear hysteresis loops can be demonstrated in a single device with a polarity dependence.

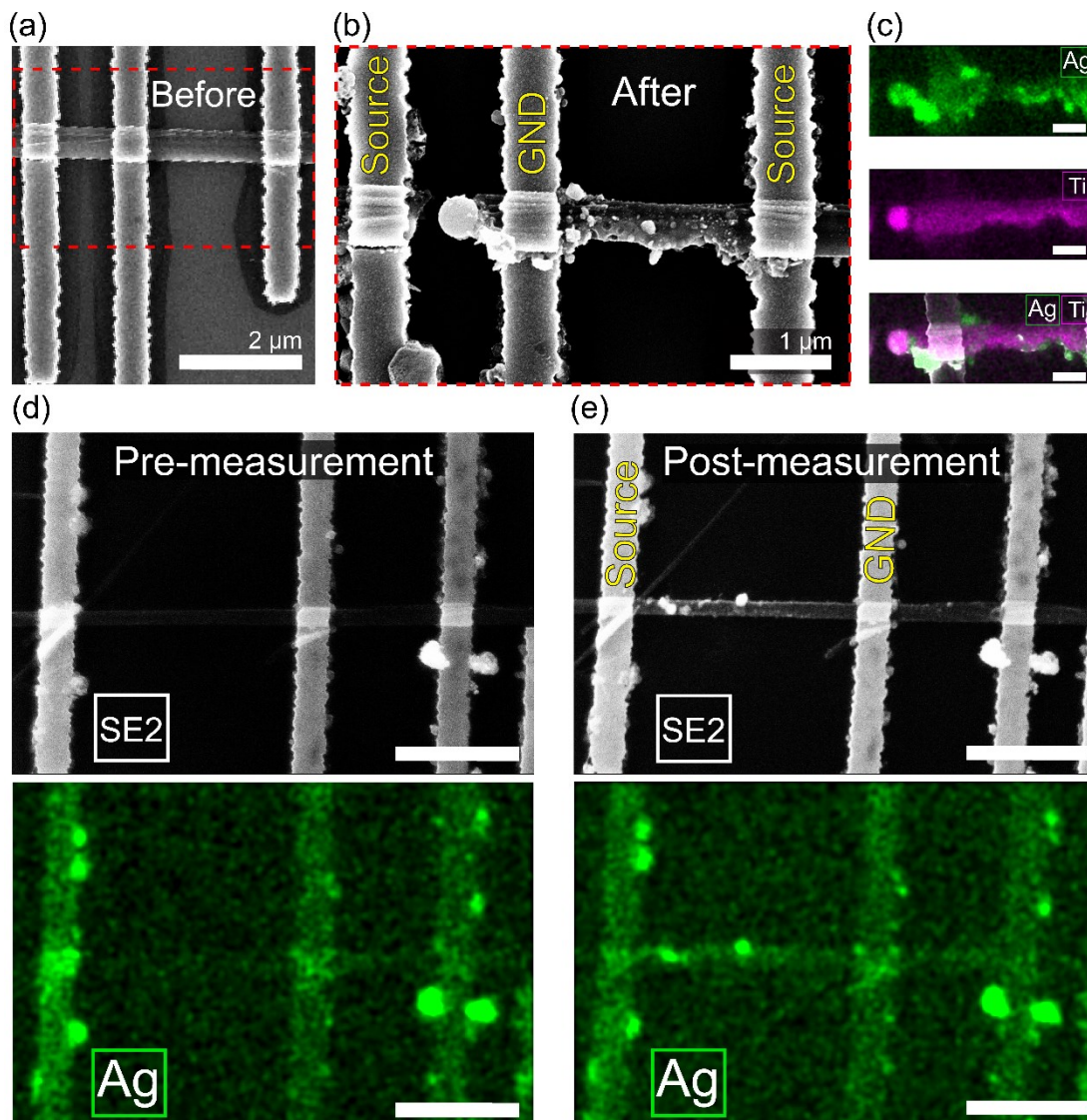


FIGURE 5.14 (a) SEM image of the pristine device and (b) after electrical measurement. The discontinuous device to the left failed on application of a +10 V electroforming step after a current spike to 500 nA. (c) EDX mapping of the Ag L α (green), Ti K α (purple) and composite image are show the presence of Ag along the TiO₂ nanowire. Scale bars represent 500 nm. (d) Ag contacted TiO₂ nanowire imaged with the SE2 detector (top) and EDX detector (bottom) prior to any electrical measurement. (e) The same nanowire post-electrical measurement where 1 μ A of current was flown through the device. Clearly visible are the additional nodules and Ag signals on the nanowire post-measurement. Scale bars represent 2 μ m.

To check for device degradation, devices were imaged using SEM before and after electrical measurement. Before electrical measurement, the nanowires appeared continuous and undamaged in their pristine state (Figure 5.14(a)). After electrical measurement, the damage was observed on all Ag contacted devices which were

electrically tested, an example of this can be seen in Figure 5.14(b), the 1 μm channel device experienced failure after a current spike of 500 nA was experienced during the 10 V hold of the electroforming step. The region of the nanowire which looks to be etched and pitted is the nanowire device for which electrical data is presented in Figure 5.12. Figure 5.14(c) shows an example of the EDX (30 KeV using a Bruker XFlash® 6|30 EDX detector) mapping which was performed on TiO_2 nanowire devices post electrical measurement. The Ag elemental map from the detection of the Ag $L\alpha$ signal (green) shows a weak Ag signal from underneath the Ni contacts as expected. Ag species are also detected along the length of the wire. The Ti $K\alpha$ signal (purple) shows the Ti composition of the nanowire, with regions etched out from the wire. Similar degradation and failure of devices were seen in all Ag contacted TiO_2 nanowires which had been electrically tested (Figure 5.14(c) and (d)), with separations between the electrodes ranging from 500 nm to 3 μm . The reason for the damage is unknown. One explanation for the damage to TiO_2 wires with Ag contacts could be that Ag electromigrates along the TiO_2 nanowire, as shown by the EDX mapping. The presence of the metallic ions causes the larger current flow which is observed in these devices. The increase of current and therefore power could contribute to thermal hot spots induced by the Joule heating.

It is worth mentioning that the fast diffusion of Ag atoms on the outmost surface of TiO_2 nanotubes during heating has been previously observed by Zhang et al.^[38] The activation energy for the diffusion of Ag atoms on the outmost surface of TiO_2 nanotubes at 400 °C was recorded as being less than that for the lattice diffusion of Ag and larger than that for the grain boundary diffusion through TiO_2 . No electrical results were presented, however, the group reported that the diffusion of TiO_2 lead to the formation of nanocrystals on the outmost surface of the TiO_2 nanotubes, similar to the results presented in this work.

In-situ electrical measurements and TEM imaging may provide additional insight into the conduction mechanisms, and observed degradation of Ag contacted TiO_2 nanowires, such experiments are planned as future work.

5.6 Conclusion

In conclusion, the memristive properties of single TiO₂ nanowires contacted with Au electrodes have been demonstrated. Through an electroforming step, the resistance of the wire was reduced from 10¹² Ω in the pristine state to 10⁸ Ω in the developed state. The effect of the forming voltage was shown to vary exponentially with the forming current. A forming process, either by a steady voltage hold, or subjecting the device to multiple voltage sweeps in a single direction is critical to develop an asymmetry and produce a population of charge carriers which modulate the Schottky-like barrier height and control the transport at the Au electrode-semiconductor interface.

The single TiO₂ nanowire device presented in this chapter used the same materials as conventional thin-film memory cells, but arranged in a lateral structure where the two electrodes lie in the same horizontal plane, and the current is conducted horizontally between them. The relatively large separations between the electrodes (μm scale), when compared to lateral cells (nm scale), separates the behaviours of the device and the two electrode regions. The generation of oxygen vacancies by electrochemical reactions allows for the dynamical evolutionary behaviour where the current level could be incremented and decremented using positive and negative voltages; this contrasts with most thin-film cells where abrupt changes in resistance level are experienced as large concentrations of charge carriers can span the short channel between the two electrodes.

The dynamical analogue response of the nanowire was exploited to demonstrate six and eleven memory levels in a single nanowire device by defining levels of conductance which could be reached through repeatedly pulsing the device. Voltage and optical stimuli were used to elicit an enhancement in the current response. The maximum enhancement factors varied between four and eight, with voltages required to reach this value ranging from 0.8 V to 1.6 V. The associative memory effects demonstrated with optical and voltage stimuli are unique and open the possibility for novel low- power sensors or neuromorphic hardware which rely on highly correlated inputs.

The effects of replacing one or more of the Au electrodes with Ag was also investigated. By contacting the TiO₂ nanowire with an Ag electrode threshold switching and degradation of the wire was observed, the movement of Ag species

along the single crystalline TiO₂ wire was characterised by EDX analysis of devices prior to and post electrical measurement.

The high-resistivity of TiO₂ nanowires makes realisation of TiO₂ nanowire networks impractical with extremely large voltages required to drive a small current response. The single wire TiO₂ system, as a simple two-terminal device spanning μm s in distance displays fascinating electronic and optical properties. The improvement of the current response could be obtained by shorting the separation between the electrodes. However this requires precise lithography. Work on TiO₂ nanowires was done in preparation of engineering core-shell nanowires which combined a highly conductive core with a TiO₂ shell, shortening the active switching region to the nm scale. The results of this will be presented in the next chapter.

5.7 References

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6

NONPOLAR SWITCHING OF **Ag@TiO₂ CORE-SHELL NANOWIRES**

Chapter 5 explored the memristive behaviours of TiO₂ nanowires; single nanowire devices displayed unique memristive and neuromorphic style behaviours. In this chapter, the TiO₂ element is incorporated into core-shell nanowires which combine a highly conductive Ag core with a TiO₂ shell, shortening the active switching region to the nm scale. Ag nanowires are coated in sheaths of TiO₂ of various crystalline qualities and contacted using both passive (Au) and active (Ag) electrodes to identify the ingredients necessary for engineering controllable resistive switching behaviours. My original contribution to knowledge in this chapter includes fabrication and measurement of core-shell single nanowire devices and the first demonstration of controlled nonpolar operation in a single nanowire system. Specifically, how the electrode metal and shell crystallinity plays a crucial role in tailoring the electrical polarity response resulting in nonpolar resistive switching behaviours. To conclude, a mechanism is presented which explains the nonpolar switching modes. Aspects of the work presented in this chapter have been published in *ACS Applied Materials & Interfaces*.^[1]

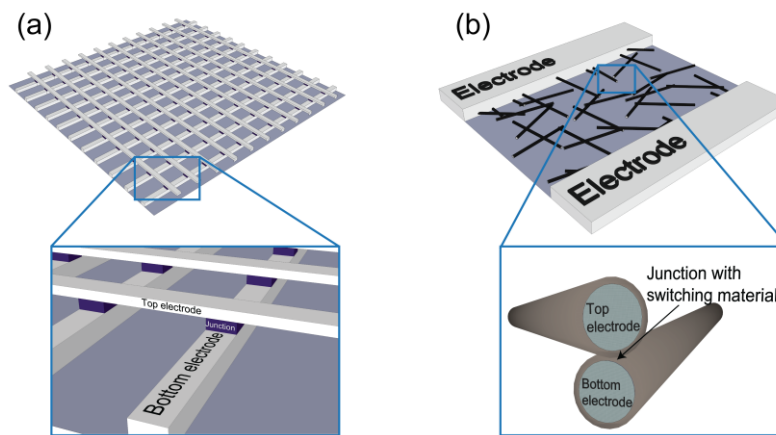


FIGURE 6.1. (a) A schematic of a traditional crossbar memory array, the blue box is a magnified area showing the bottom electrode separated from the top electrode by a junction with a resistive switching material. (b) Core-shell nanowire network with two lateral electrodes, the zoomed in image shows the analogous top and bottom electrode configuration.

6.1 Motivation

Ag is used as an active element in many redox based resistive random-access memory (ReRAM) cells. One ReRAM type is the cation-based bipolar resistive switch (BRS) introduced in chapter 1. In these technologies, a low-resistance state (LRS) is defined by the formation of nanoscale metallic filaments from an active electrode (typically Ag or Cu) through an insulator. The filament is dissolved by applying a voltage of the opposite polarity, returning the cell to a high-resistance state (HRS). These devices have low-power consumption and can display ultra-fast resistive switching.^[2-5]

On the other hand, Titanium dioxide (TiO₂) is widely used as a dielectric in thin-film unipolar resistive switching (URS) ReRAM devices. URS involves the formation of conductive filaments through an insulating material which is stable when the voltage bias is removed or inverted. During the application of large currents, Joule heating causes the dissolution of this connection. Due to the large currents needed to RESET the device, the power requirements for URS are much higher, and write-endurance lifetimes much shorter when compared to BRS. In addition to its potential in resistive switching and memristive memory devices (which was explored in chapter 5 for TiO₂ nanowires), TiO₂ has shown promise in the areas of photocatalysis, water treatment and solar energy conversion.^[6-13]

Core-shell nanowires represent a possible alternative to thin-film crossbar devices to fabricate nanoscale heterostructures (*e.g.* a metal-insulator-metal (MIM) stack) as shown in Figure 6.1(b). Connections made to the wire or junctions between

nanowires in a network will be MIM in nature. Core-shell nanowires can be obtained by core growth, followed by shell deposition, or for naturally occurring surface oxides, through heat treatment or exposure to ambient conditions. Core-shell nanowires were first investigated for resistive memory applications in 2007, where BRS was demonstrated for a monocrystalline Si core and an amorphous silicon shell nanowire.^[14] More recently, the resistive switching characteristics of core-shell nanowires have been investigated in Ni@NiO,^[15, 16] Cu@CuO_x,^[17] Cu@SiO₂,^[18] Sn-doped In₂O₃@HfO₂,^[19] Au@Ga₂O₃,^[20] and at the junction of Si@a-Si nanowires and crossing Ag electrodes.^[21] Recently, Ag@AgO_x CSNWs were designed in a nanowire network to augment transparent electrodes with resistive switching functionalities.^[22] Combinations of materials in a core-shell form-factor have been proposed for applications ranging from transparent conductors (characterised in chapter 4),^[23, 24] to fully printed memristors.^[18] In this chapter the unique properties that emerge by combining an Ag core with a TiO₂ shell, denoted as Ag@TiO₂ will be presented.

Ag and TiO₂ are two materials which can be readily combined through the synthesis of core-shell nanowires in either a single step solution process,^[25] or by coating previously synthesized Ag nanowires with TiO₂ shells.^[6] Ag@TiO₂ nanowires have been explored for use as stable and recyclable surface enhanced Raman spectroscopy (SERS) substrates, and as an efficient photocatalytic material.^[26, 27] However, to date, the electrical properties of Ag@TiO₂ core-shell nanowires have not been described, which is surprising given the interesting resistive switching and memristive properties of the individual materials. One advantage of the core-shell structure allows is the ability to control and engineer the properties of the shell (such as thickness and composition) which serves as the switching medium. The conductive core can act as both an interconnect and ion reservoir for the formation of nanofilaments. In this work Ag nanowires were coated with sheaths of TiO₂ of varying crystalline qualities depending on fabrication methods, and both polycrystalline^[28] and amorphous^[6] TiO₂ shells are investigated.

The presence of both URS and BRS is termed nonpolar switching.^[29] Multi-layered Ni/Pt nanowire arrays have demonstrated nonpolar operation.^[30] Metal-insulator-metal (MIM) and transition metal oxide (TMO) nanowire devices have shown one of either BRS or URS behaviour.^[4, 16, 31, 32] The original contribution to

knowledge in this chapter is the electrical characterisation of Ag@TiO₂ nanowires, and demonstration of controllable nonpolar resistive switching of these core-shell nanowires. Based on the results, we propose a switching mechanism based on filament theory to explain the existence of both BRS and URS behaviours.

6.2 Amorphous TiO₂ Shell Ag Core Nanowires

Ag core TiO₂ shell nanowires were grown by Dr Subhajit Biswas in the Materials Chemistry & Analysis Group (MCAG) in the Department of Chemistry and Tyndall National Institute situated in University College Cork, headed by Prof. Justin D. Holmes. Wires were synthesized using a solvothermal growth method reported by Du *et al.*,^[6] and transferred into IPA where they were stable in solution for over 24 months. Wires produced by this method and dropcast onto SiO₂ can be seen in the SEM image in Figure 6.2(a). An example of the TEM analysis, performed by Dr Eoin McCarthy using a FEI Titan microscope operated at 300 kV is shown in Figure 6.2(b), interestingly the presence of Ag regions in the TiO₂ shell was observed, which were further investigated using scanning TEM (STEM) and energy dispersive x-ray (EDX) elemental analysis. The orange line in Figure 6.2(c), shows a scan through; (i) a section of TiO₂ shell containing an inclusion (ii) the Ag core and (iii) through a section of the TiO₂ shell with no inclusion. The results of this line scan are shown in Figure 6.2(d), which shows the K α intensity plots for the Ti (red) and Ag (green) signals over the length of the line scan. This clearly shows that inclusions in the shell are composed of Ag. These inclusions are likely the result of Ag ion migration during the elevated temperature (~ 150 °C) of the solvothermal treatment. Further TEM analysis was used to determine that the Ag core was an average of 59 ± 11 nm in diameter with an amorphous TiO₂ shell (Ag@TiO₂(A)) on average 29 ± 8 nm thick. Measurements of core (green bars) and shell thicknesses (red bars) can be seen in Figure 6.2(e), with the inset showing a TEM image of nanowire sample 1, the first of ten measurements on the core (green) and shell (red) along the length of a single wire, which contribute to the error bars in the graph. The distribution of wire lengths from SEM imaging can be seen in Figure 6.2(f), the wires range in length from 2 – 40 μm , with a mean value of 10.8 ± 7.4 μm .

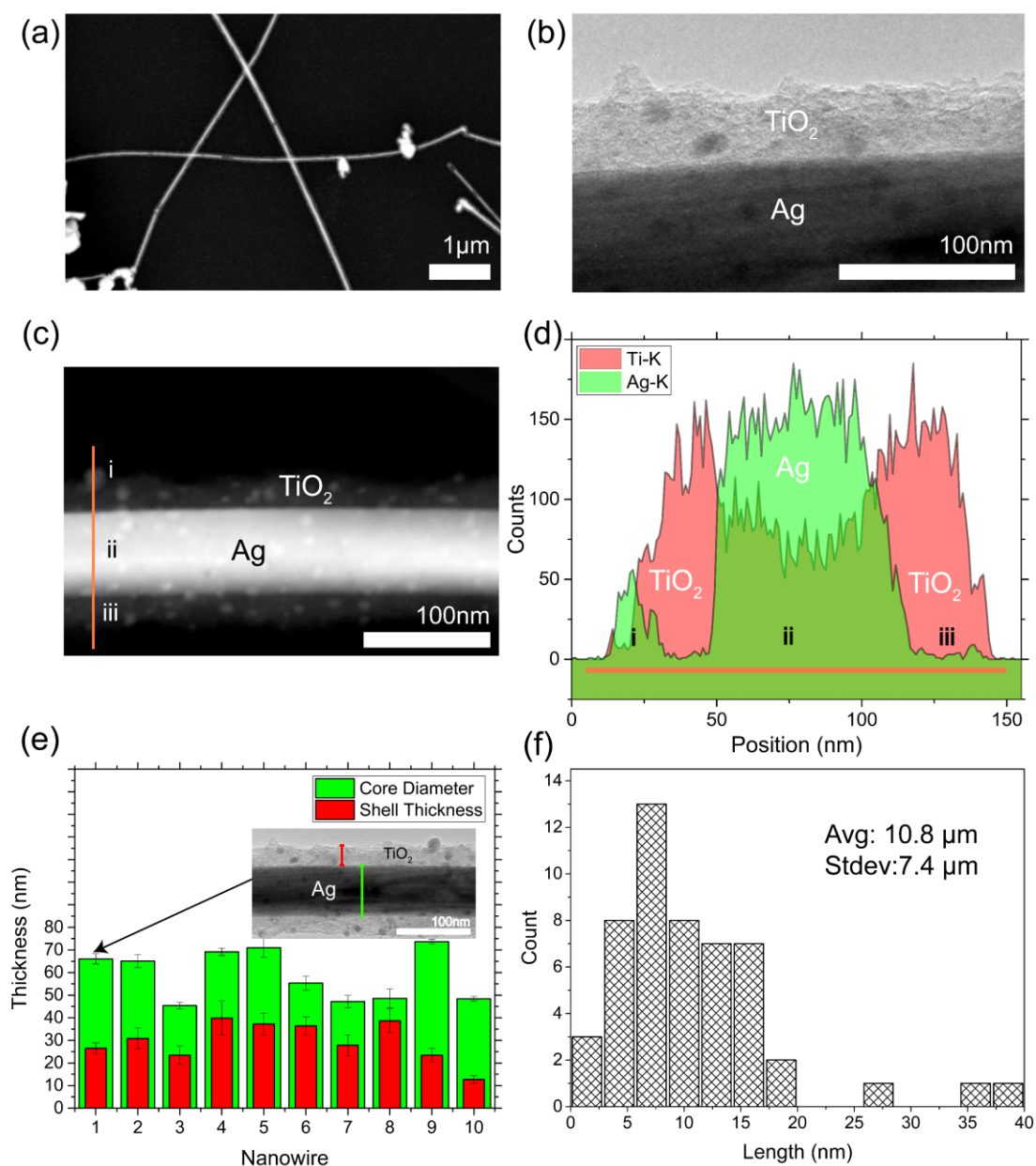


FIGURE 6.2. Characterisation of Ag@TiO₂(A) nanowires. (a) SEM image of dropcast nanowires. (b) High-resolution TEM image of Ag@TiO₂(A) core-shell nanowire. (c) STEM image of Ag@TiO₂(A) nanowire, the orange line shows the path of an EDX line scan with three regions; (i) an inclusion of Ag in the shell, (ii) the Ag core, and (iii) the TiO₂ shell. (d) EDX line scan confirming the composition of the inclusion and core by the Ag (green) and Ti (red) K α signal. (e) Core (green) and shell (red) diameters for ten individual nanowires, inset is a representative TEM showing one of ten core and shell measurements. (f) Length distribution of Ag@TiO₂(A) with an average wire length of 10.8 ± 7.4 μm.

6.3 Polycrystalline TiO₂ Shell Ag Core Nanowires

Polycrystalline Ag@TiO₂ (Ag@TiO₂(P)) core-shell nanowires were also synthesized by Dr Biswas, using a thioglycolic acid (TGA) mediated process.^[33] In particular he notes that, 5 μ L of TGA was added to 2.5 mg PVP capped AgNWs in anhydrous ethanol (8 ml) under stirring. After stirring for 30 min, 20 μ L of tetrabutyl titanate (TBT) was added dropwise as a TiO₂ source into the solution under an inert N₂ atmosphere. The solution was stirred for another 20 min. The final mixture was transferred into a 20 mL teflon-lined autoclave for solvothermal treatment at 150 °C for 10 h. The resulting sample was washed three times with water, then ethanol and centrifuged at 6000 rpm before being finally dispersed in IPA. In IPA, the wires were stable in solution for more than a year. SEM in Figure 6.3(a) shows the nanowires dropcast on a SiO₂ substrate. As with the amorphous shelled nanowires, these wires were fully characterised with TEM, operated by Dr Eoin McCarthy under the conditions detailed previously. TEM analysis showed the presence of inclusions in the shell of the nanowire, using EDX mapping of the K α edge they were confirmed to be Ag, this mapping can be seen in the inset of Figure 6.3(b), and once again the solvothermal treatment is believed to be the cause of the migration and gathering of Ag in these regions. The crystallinity of the TiO₂ shell was determined by diffraction and fast Fourier transform (FFT) performed by Dr Subhajt Biswas using a JEOL 2100 TEM operated at 200 kV. Figure 6.3(d) shows a high resolution TEM image of the core/shell interface, with the FFT pattern in the inset confirming the polycrystalline rutile crystal structure of the TiO₂ shell. Ag@TiO₂ nanowires grown by this method had a much narrower distribution of core and shell thicknesses. Figure 6.3(e) shows measurements taken from TEM analysis, the Ag core was an average of 63 ± 10 nm in diameter with a polycrystalline TiO₂ shell on average 14 ± 2 nm thick. The distribution of wire lengths from SEM imaging results in an average wire length of 4.4 ± 1.3 μ m (Figure 6.3(e)).

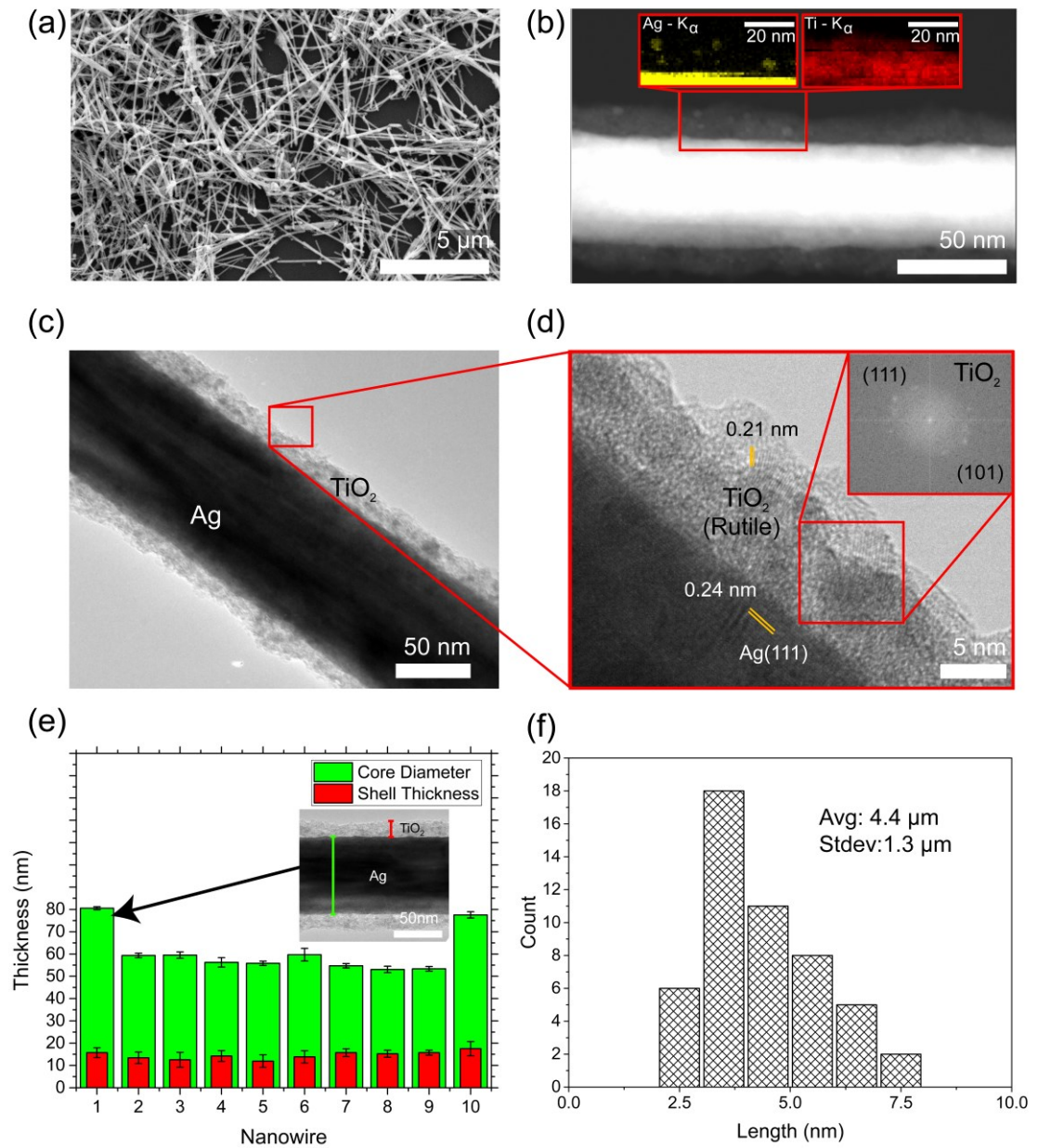


FIGURE 6.3. Characterisation of Ag@TiO₂(P) nanowires. (a) SEM image of dropcast nanowires on SiO₂. (b) STEM image of Ag@TiO₂(P) core-shell nanowire, insets showing an EDX area scan in the orange box of the core/shell interface. The map shows the Ag (yellow) and Ti (red) K α signal. (c) High-resolution TEM image. (d) Magnified area of the red box in (c) showing the single crystalline Ag core, and regions of the shell composed of rutile TiO₂, inset SAED pattern of the polycrystalline TiO₂ shell. (e) Core (green) and shell (red) diameters for ten individual nanowires, inset is a representative TEM showing one of ten core and shell measurements. (f) Length distribution of Ag@TiO₂(P) with an average wire length of 4.4 \pm 1.3 μ m.

6.4 Single Wire Device Fabrication

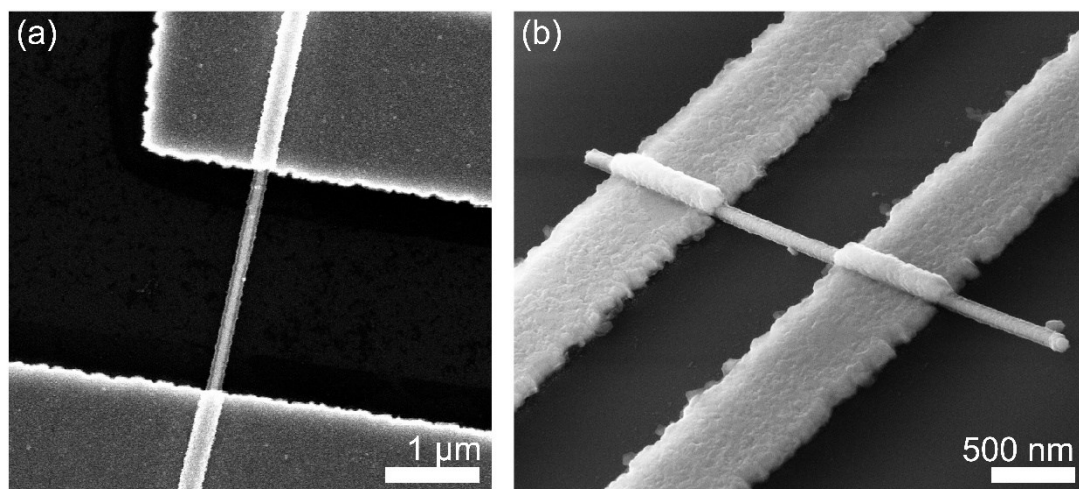


FIGURE 6.4. SEM images of 2-probe core-shell nanowire devices. (a) Ag@TiO₂(A) nanowire contacted with Ag electrodes separated by 2.4 μm. (b) Ag@TiO₂(P) nanowire contacted with Ag-Al electrodes, with a channel length of 900 nm.

Single core-shell nanowires were contacted by electron beam lithography (EBL) after drop casting the nanowire/IPA dispersion onto clean Si substrates (1 μm thermal oxide) with optical lithography defined Ti-Au contact pads (5-25 nm). EBL defined electrical contacts of Au-Al (30-130 nm), or Ag-Al (100-100 nm) were deposited by thermal evaporation. Details of the fabrication procedures are given in chapter 2. Typical examples of Ag@TiO₂ (A and P) nanowires with EBL defined metal contacts can be seen in Figure 6.4(a and b) respectively. The separations between the electrodes varied from 900 nm to 2.5 μm for both batches. Samples were capped by a micro droplet of EL8.5 methyl methacrylate (MMA) copolymer resist to protect the devices from reacting with the ambient, but leaving the large UV defined electrical pads open for electrical contact by the micro-probers. All electrical measurements were carried out at room temperature using a Keithley 4200-SCS.

6.5 Electrical Characterisation of Ag@TiO₂(A)

This section will detail the 2-probe direct current (DC) electrical behaviours of single *amorphous* TiO₂ shelled Ag core nanowires with passive (Au) and active (Ag) electrodes.

6.5.1 Au – Au Contacts

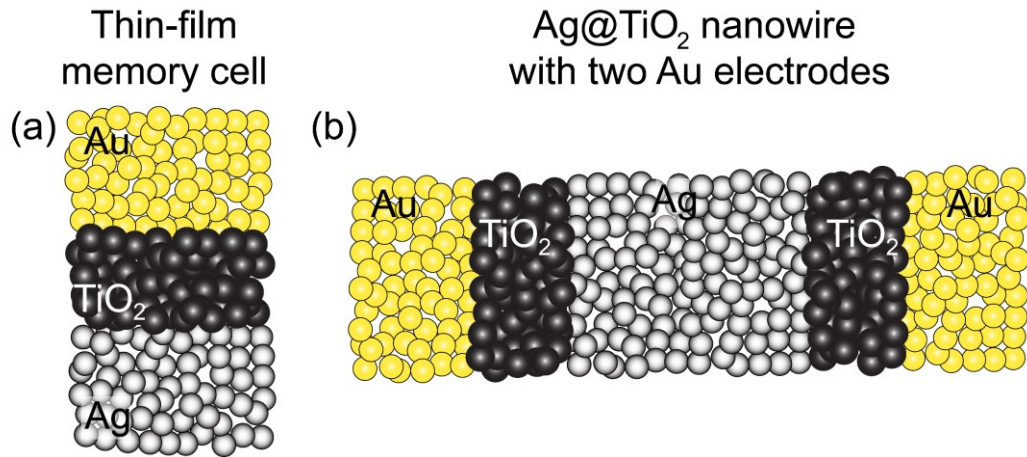


FIGURE 6.5. (a) Schematic of a traditional two-terminal thin-film memory cell and (b) the connections of an Ag@TiO₂ nanowire contacted with two Au electrodes (the length of the wire core is shown as an Ag electrode).

Core-shell nanowires were contacted with Au-Ni (30-170 nm) to investigate the electrical properties of nanowires contacted with a passive electrode opposite the inner core of the wire. The accepted mechanism for devices which use an oxidizable (soluble) active electrode is the growth of a metallic filament which bridges the insulating ion conductor and to form a low-resistance ON state.^[3, 34] Generally, two-terminal thin-film memory cells are fabricated with one active and one passive electrode separated by an insulating layer (Figure 6.5(a)). An Ag@TiO₂ nanowire contacted with two electrodes looks schematically like two traditional thin-film memory cells stacked head-to-head (Figure 6.5(b)).

Figure 6.6(a) shows the electrical response of the amorphous shelled Ag@TiO₂ nanowire contacted with Au electrodes. The black curve is the first measurement to a compliance current of 1 nA, I-V traces are shown as the red, blue and green curve with compliance currents of 10 nA, 100 nA and 1 μ A, respectively. In all cases the device failed to establish a low resistance state. Increasing the compliance to 10 μ A resulted in the magenta curve where the current through the nanowire abruptly dropped at 9 V (marked as 'failure' on the graph). After this, the inset I-V curve was measured, where negative voltage was sourced initially. The nanowire reached compliance (10 μ A) at -9.8 V but did not exhibit an ohmic return to 0 bias, consistent with threshold switching. On the positive side of the I-V curve, spikes of current were recorded and then another sudden drop in current (also marked as 'failure'). A further 0-40 V sweep

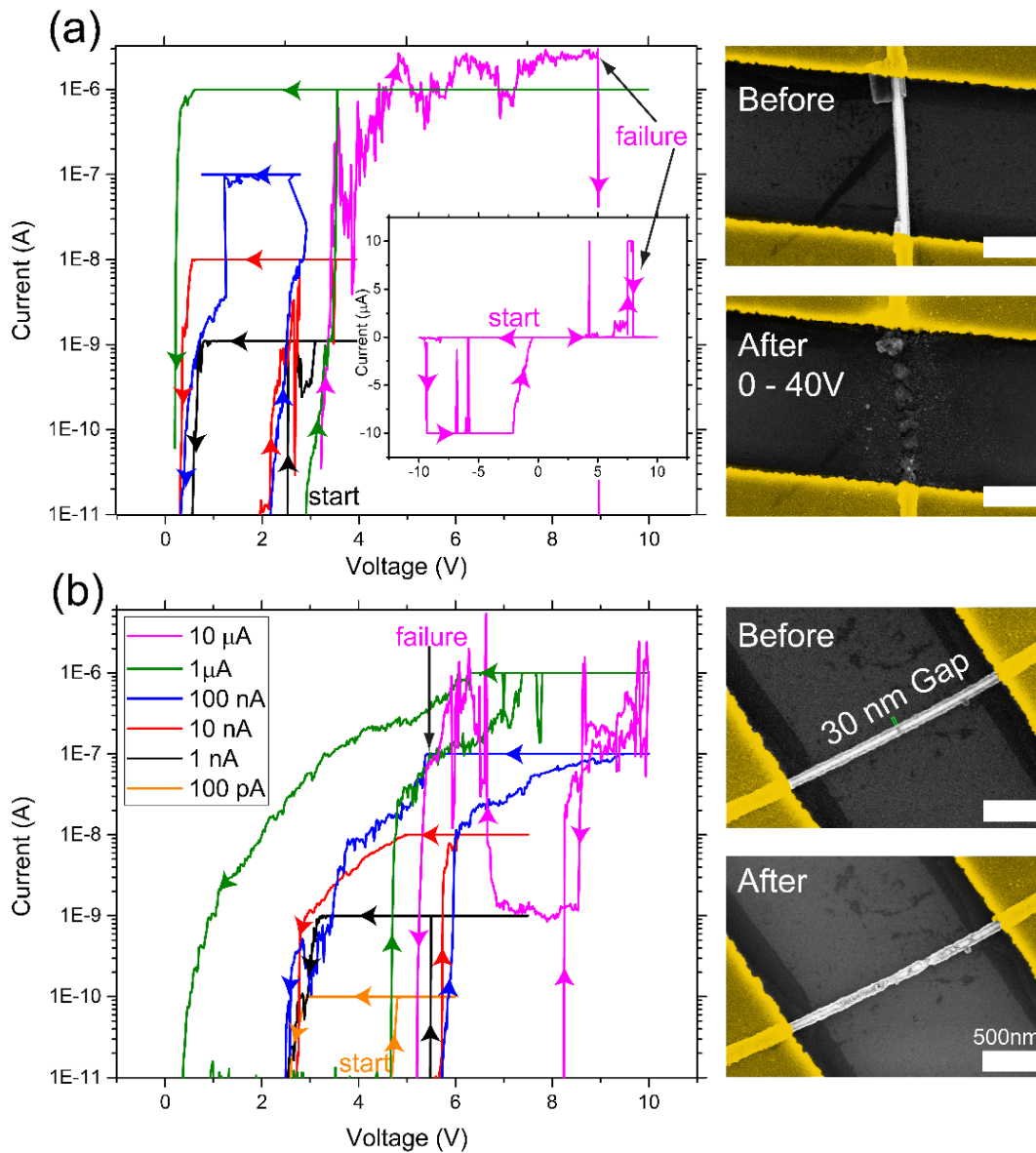


FIGURE 6.6. Poor electrical behaviour and SEM images of Au contacted Ag@TiO₂(A) core-shell nanowire with and without a continuous Ag core. (a) Low current, threshold switching, and failure of a device with a continuous Ag core prior to measurement. (b) Similar low current threshold switching from a nanowire with a 30 nm gap in the Ag core of the wire. Post measurement the core was found to be extremely fragmented and the morphology of the shell had been effected by the electrical measurements.

in the positive and negative direction with 10 μA compliance was applied, with very erratic current behaviour. Prior to electrical measurement the wire was observed to have a continuous core, after all electrical measurements were completed the wire had catastrophically failed, even though currents no larger than 10 μA were allowed flow through the device and no stable LRS was ever reached.

Figure 6.6(b) shows a nanowire which prior to electrical measurement had a 30 nm gap in the core of the wire. The main I-V plot shows electrical currents recorded while performing a 0-10 V dual sweep at increasing compliance currents. As the current compliance is increased the current response became more erratic, and the sample failed once again during the 10 μ A compliance measurement, shown by the magenta curve. SEM imaging after electrical measurement shows that the core had become very fragmented and the morphology of the TiO₂ shell had also been affected. We postulate that the Ag core is only capable of bridging one interface at a time due to the dynamic oxidation and reduction processes occurring at both electrodes, the Ag in the wire may also be unable to provide enough material to sustain a connection at each junction while maintaining a continuous core. Ag ions readily electromigrate under the application of electric fields, what was interesting to note is that parts of the Ag core had also migrated under ambient conditions. In many cases voids had formed in the core of the nanowire explaining the poor electrical behaviours.

To further investigate the movement of the core and the formation of voids. Au contacted Ag@TiO₂ nanowires were imaged shortly after contacting by EBL and metallisation, and then a week later, without having undergone any electrical measurements. Figure 6.7(a-c, left column) shows the 'before' SEM image of Ag@TiO₂ nanowires which are seen to have continuous Ag cores shortly after contacting. The after (a-c, right column) images, taken 7 days later, show the formation of gaps in the wire (a-c) measuring 450, 150 and 300 nm respectively. These voids may be formed in a process driven by electromigration due to galvanic corrosion. The formation of segmented nanowires, under ambient conditions and under electric fields causes Au contacted Ag@TiO₂ nanowires to have poor, short-lived electrical responses. The Ag core is used as an interconnect between the Au electrodes, segmentation and depletion of this pathway by using Ag ions to form a connection across the insulating TiO₂ shell disrupts the electrical conduction. To overcome this, another source of ions in the form of an active electrode must be used. The next section will detail the electrical behaviours of Ag contacted core-shell nanowires.

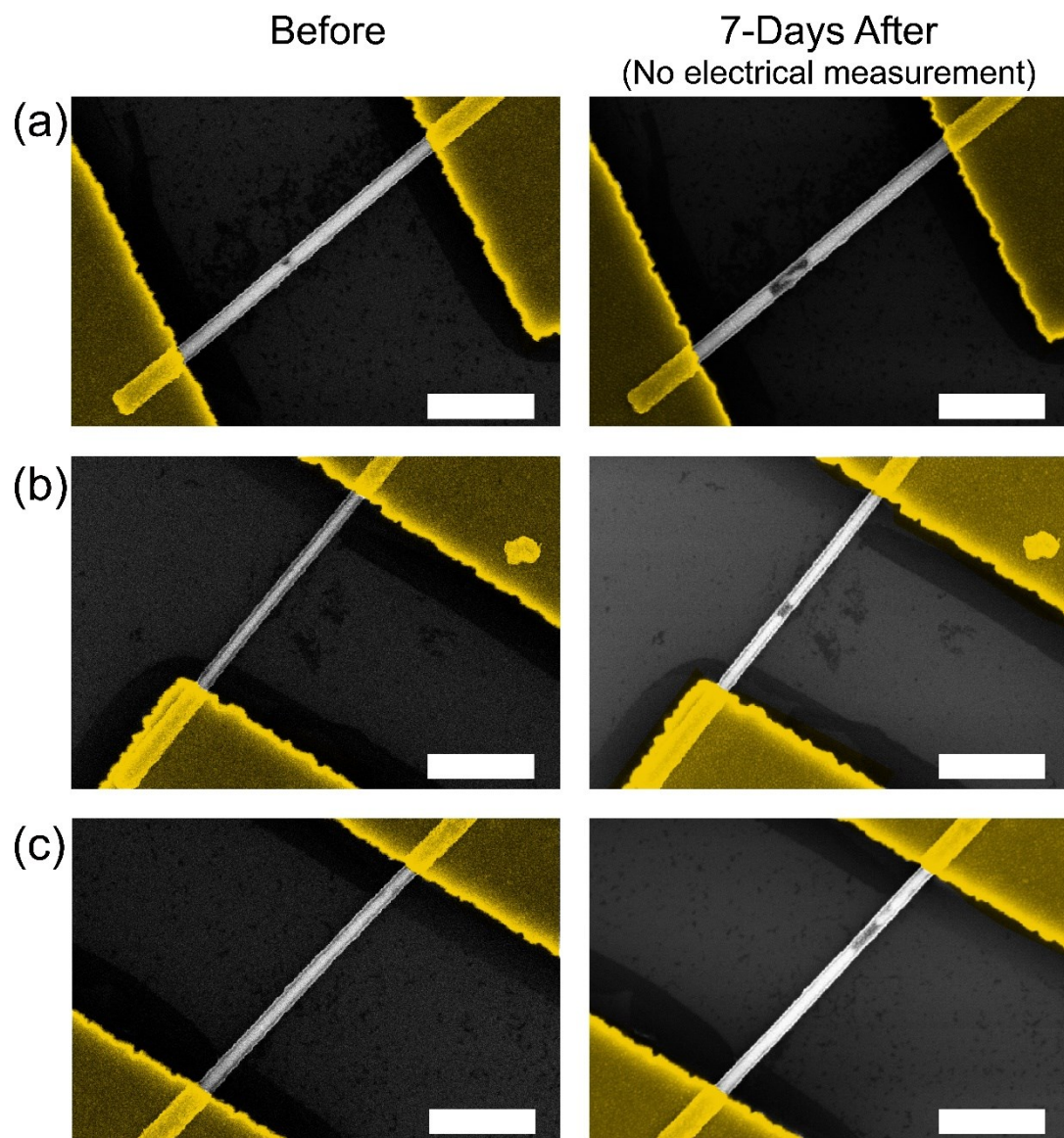


FIGURE 6.7. False coloured SEM image of amorphous TiO₂ shelled Ag nanowires contacted by two Au electrodes, shortly after metal deposition (left column a-c) and 7 days later (right column a-c). No electrical measurements had been performed on these samples between imaging, yet the movement of the Ag core is clearly visible by the formation of voids within the nanowire. All scale bars represent 1 μm

6.5.2 Ag – Ag Contacts

To provide another source of Ag ions and improve the electrical behaviours of *amorphous* TiO₂ shelled Ag core nanowires, the use of Ag as the contact electrode was investigated.

Devices were fabricated as detailed in section 6.4 with Ag (150 nm) thermally deposited into EBL defined electrodes. Initial results on the electrical behaviours were promising; using Ag electrodes resistive switching was observed at 900 mV to a 1 μ A compliance current (Figure 6.8(a)). The low-resistance state continued as the sourced voltage returned through the origin and goes negative. The polarity independent resistive switching is commonly known as unipolar resistive switching and has been discussed in detail in chapter 1 and previously shown for Cu and Ni nanowires in chapter 3. The lifetime of the low-resistance state, when the voltage is removed, is very short lived. This can be seen in Figure 6.8(b) where three successive voltage sweeps result in three activations to a compliance current of 100 μ A. It is only from sweep 4 onwards that the I-V response at the beginning of the experiment is semi-ohmic, at sweep 8 the device is in a semi-stable low-resistance state and displays a resistance of 900 Ω . The low-resistance state is defined as semi-stable due to the decay of current which is observed over the course of 80 s, as the current is read by a 25 mV read voltage pulses (Figure 6.8(c)). To investigate whether the low-resistance state could be reset by traditional and controllable methods a unipolar reset procedure was run on a nanowire device. A typical I-V response to this reset procedure was observed, where the current rose in response to a voltage, and then suddenly dropped, however, subsequent measurements showed no current response to voltage, after SEM imaging it was obvious that the device had failed (Figure 6.8(d)). The semi-stable low-resistance state is an undesirable and uncontrollable feature. The decay time can be controlled by limiting the current allowed to set the device through raising and lowering the compliance current. This is completely impractical for a memory device.

The resistive switching responses of amorphous TiO₂ shelled Ag core nanowires were not as expected. Controllable unipolar resistive switching with an amorphous TiO₂ dielectric spacer layer and Ag electrodes had previously been demonstrated in thin-film structures.^[35] The absence of controllable resistive switching in the core-shell devices can be explained by structural differences between

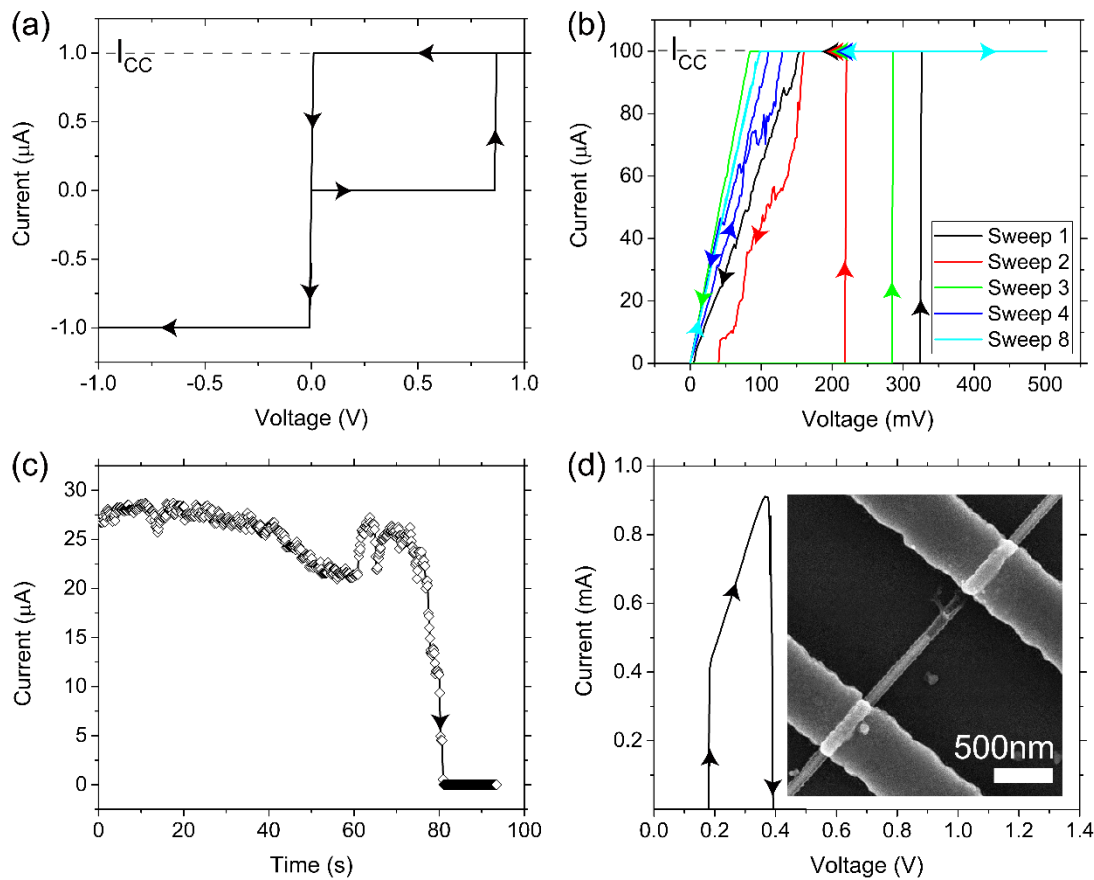


FIGURE 6.8. Electrical behaviour of Ag contacted Ag@TiO₂(A) nanowires. (a) An I-V curve of electrical activation at 1 V to a compliance current of 1 μA, the device remains in a low-resistance state on the return trace through 0 bias and into negative voltages demonstrating unipolar style behaviour. The arrows signify the direction of the sweep. (b) Multiple sweeps to 100 μA compliance, the first three sweeps require an activation at 330, 220 and 290 mV respectively, sweep 4 shows an ohmic, but noisy response, while at sweep 8 the device is in a semi-stable low-resistance state. (c) The decay of the low resistance state set at 100 μA over time using a read voltage of 25 mV. (d) Attempted unipolar reset of a low-resistance state without setting the current compliance, inset as a SEM image of the broken nanowire taken after the test.

these two systems and the ability of thin-film memory cells to withstand the large currents required in the reset process. The reset process in the thin-film cell required ~20 mA to complete, core-shell devices showed failure due to a combination of Joule heating and electromigration in the mA range.

In order to investigate the resistive switching characteristics of polycrystalline TiO₂ shelled Ag core nanowires an alternate synthesis approach was used, whereby previously synthesised Ag nanowires were coated in TiO₂ as described in the work of Changchao et al.^[33] detailed in section 6.3

6.6 Electrical Characterisation of Ag@TiO₂(P)

In this section, the 2-probe DC electrical behaviours of polycrystalline TiO₂ shell Ag core nanowires with passive (Au) and active (Ag) electrodes will be investigated.

6.6.1 Au - Au Contacts

Core-shell devices consisting of a single nanowire contacted with Au-Al (30-170 nm) were electrically tested using the Keithley 4200-SCS electrical system under ambient conditions. A representative I-V sweep is shown in Figure 6.9(a), the device is initially in a high-resistance state, with the polycrystalline TiO₂ shell separating the Ag core and the Au contact. With a positive voltage sweep the device reaches a compliance current of 100 nA at 6 V, this did not result in a stable low-resistance connection as the device could not sustain the required current with less than 2 V. Due to the symmetric construction of the device, a similar threshold switching event occurred when sourcing negative voltage. The volatile threshold switching demonstrated here is identical to behaviours observed on the amorphous shelled TiO₂ shelled Ag core nanowires contacted with Au electrodes. As with the amorphous shelled wires, the polycrystalline shelled wires contacted with Au were unable to sustain large flows of current. Figure 6.9(b) shows the electrical failure of a device after only passing 1 μ A of current for a short period. The inset of the figure shows a false coloured SEM image of the destroyed wire. This clearly shows that Ag electrodes are required to provide a source of ions to mitigate against void formation in the core of the nanowire.

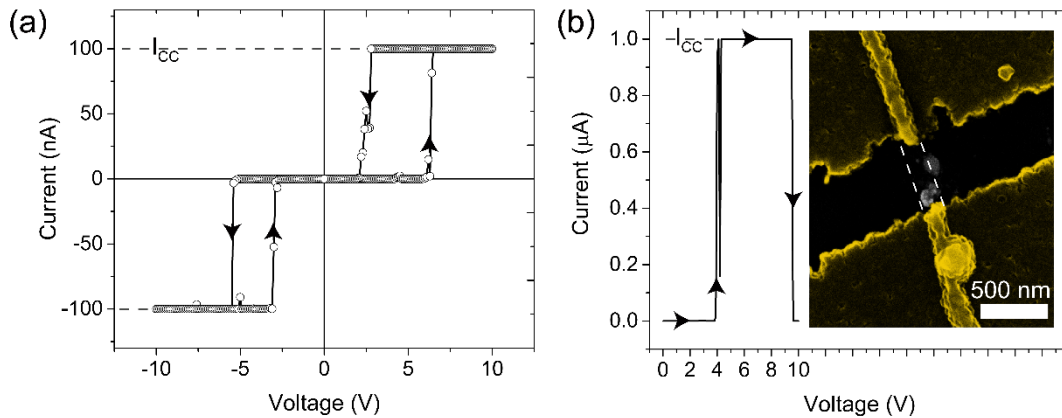


FIGURE 6.9. (a) An I-V curve of an Au contacted polycrystalline TiO₂ shelled Ag nanowire, a voltage of 6.5 V is required to reach the compliance current of 100 nA, this volatile connection cannot be sustained under 2 V. Due to the symmetric construction of the device the same behaviour is observed when sweeping through increasing negative voltages. (b) When increasing the current compliance to 1 μA the nanowire suddenly ceased to flow current. The inset shows a false coloured SEM image post measurement showing that the wire had failed. This behaviour was typical of all Au contacted polycrystalline Ag@TiO₂ nanowires which were tested.

6.6.2 Ag – Ag Contacts

Figure 6.10(a) (next page) shows a typical I-V curve for polycrystalline TiO₂ shelled Ag core nanowires with Ag electrodes for positive (black) and negative (red) voltage sweeps. As the voltage is swept in the positive direction no significant current is measured by the system until the device reaches a SET state at 0.4 V, the current then jumps six orders of magnitude to the predefined current compliance and enters a bipolar low-resistance state (LR^{BRS}), when the voltage is ramped back towards zero the device is ohmic on the return trace with a resistance of 1-2 kΩ. Then, as the voltage continues to be swept in the negative bias direction the current follows linearly until the device experiences a RESET event at -600 mV (1.8 μW of power) and enters the bipolar high-resistance state (HR^{BRS}) with a resistance >100 MΩ. Due to the symmetric construction of the device, continuing the sweep in the negative direction causes a second SET event, which will RESET with a sufficient positive voltage, this can be seen by the red curve of Figure 6.10(a).

The BRS is repeatable over hundreds of cycles and displays a LRS (ON) to HRS (OFF) ratio of 10⁵, shown in Figure 6.10(b). By setting the current compliance it is possible to control the resistance of the LR^{BRS}, though at the cost of a reduced

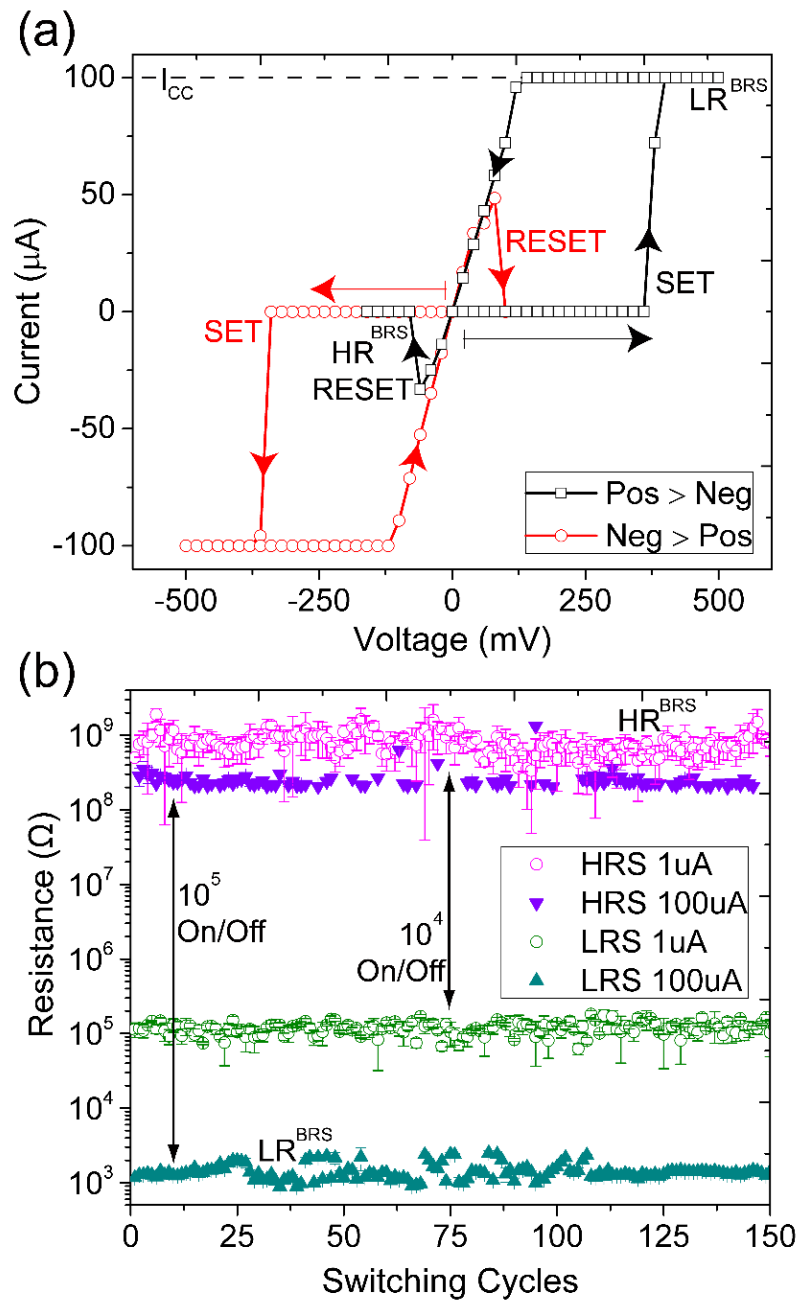


FIGURE 6.10. (a) Typical I-V characteristics of the individual Ag-TiO₂ core-shell nanowire device operating in the bipolar regime. Following the black curve, the device is SET (from a high-resistance state (HRS) to a low-resistance state (LRS)) at 400 mV at a current compliance limit of 100 μA. The device is RESET on application of a suitable negative bias. The red curve shows the same behaviour when the device is SET in the negative voltage direction. (b) Values of the HRS and LRS by cycling the forward bias test of (a) multiple times at 1 μA (hollow circle) and 100 μA (shaded triangle) compliance current.

ON/OFF ratio, when the same device was cycled using a 1 μ A current compliance it exhibited an ON/OFF ratio of 10^4 , which is still perfectly acceptable to distinguish the LRS from the HRS. However, reducing the current compliance has implications for the lifetime (retention) of the LRS, configuring the retention time by programming the current compliance will be discussed later in the chapter. From comparison with the amorphous devices, we can deduce that the polycrystalline TiO₂ shell is critical to the observed nonpolar resistive switching. A reason for this could be that the polycrystalline shell offers diffusion pathways which are necessary for the controlled resistive switching in polycrystalline TiO₂; these are not present in the homogeneous amorphous phase TiO₂ wires, this will be expanded upon later. Another consequence of this result is that for core-shell nanowire systems containing electrochemically active metals (Ag core/inclusions) the choice of electrode metal is just as important as it is for planar devices, obviously an active electrode is required to facilitate the resistive switching, which will assist in determining a mechanism for the observed behaviours.^[11, 34, 35]

As mentioned previously, the current compliance can limit the resistance of the ON state, to further investigate this successive I-V sweeps were performed and the current compliance limit was raised after each SET/RESET cycle. The results of this test are summarised in Figure 6.11. Clearly the ON-state resistance of the device is controlled by the magnitude of the current compliance, this can be seen in the change in the slopes of the return current trace from the compliance limit down to zero bias. Interestingly, BRS behaviour was available for current compliance settings of up to 125 μ A. At a current compliance value of 150 μ A the device remained in a low-resistance state at negative voltages, consistent with a transition to the URS regime. This is an unexpected result, the coexistence of bipolar and unipolar resistive switching and its control via a current compliance has only been shown in the literature for a Pt/nanocrystalline anatase TiO₂/Pt stack where Ti interstitial ions were believed to form filament like regions connecting the top and bottom electrode.^[36] Ti interstitial ions cannot explain the dual mode behaviour in Ag@TiO₂ nanowires as no resistive switching was seen with Au electrodes, providing further evidence that the switching mechanism must therefore be reliant on filamentary mechanism involving Ag in the core, inclusions and contacts.

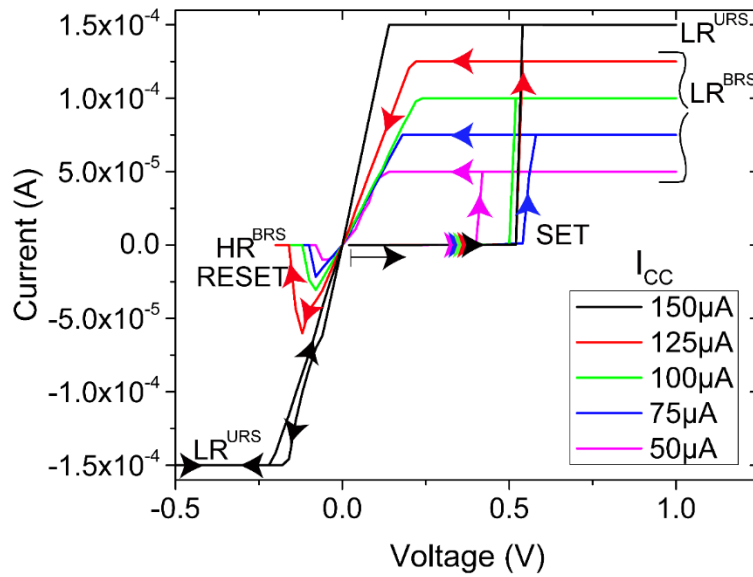


FIGURE 6.11. (a) I-V curves with increasing current compliance showing the transition from bipolar resistive switching to unipolar resistive switching regime. Up to 125 μA current compliance the device RESETS from a LRS to a HRS at a negative voltage. For a current compliance of 150 μA the LRS continues for negative voltages signifying a transition into the URS regime. The arrows signify the sweep direction.

This shows that an alternative unipolar switching regime for Ag@TiO₂ nanowires can be accessed by using a high current compliance for setting the device ($>125 \mu\text{A}$). A URS I-V trace using a compliance current of 250 μA is shown in Figure 6.12(a). The black trace at the bottom of the graph describes an increasing positive voltage is until a SET event is reached at 0.88 V, at which point the device switches to the unipolar low-resistance state (LR^{URS}) which is typically $\sim 300 \Omega$. The RESET procedure of the LR^{URS} is as follows, the current compliance is removed and the device is driven to reach high current levels by increasing the voltage. At a few 100 μAs to mAs the current level suddenly drops to establish the high-resistance state (HR^{URS} , which is of a higher resistance than the HR^{BRS}). For the sweep shown in Figure 6.12(a), the device RESET at 1.3 mA and 0.51 V resulting in a power of 663 μW , 300 times more power than required for the bipolar RESET and consistent with a Joule heating dependent mechanism. After the device is RESET to the HR^{URS} it may be SET to the LR^{URS} in the opposite voltage direction, as illustrated by the red curve in Figure 6.12(a). Furthermore, by reducing the compliance current the BRS regime can be restored, this will be demonstrated shortly. Cycling the URS in Figure 6.12(b) displays an ON/OFF ratio of 10^7 .

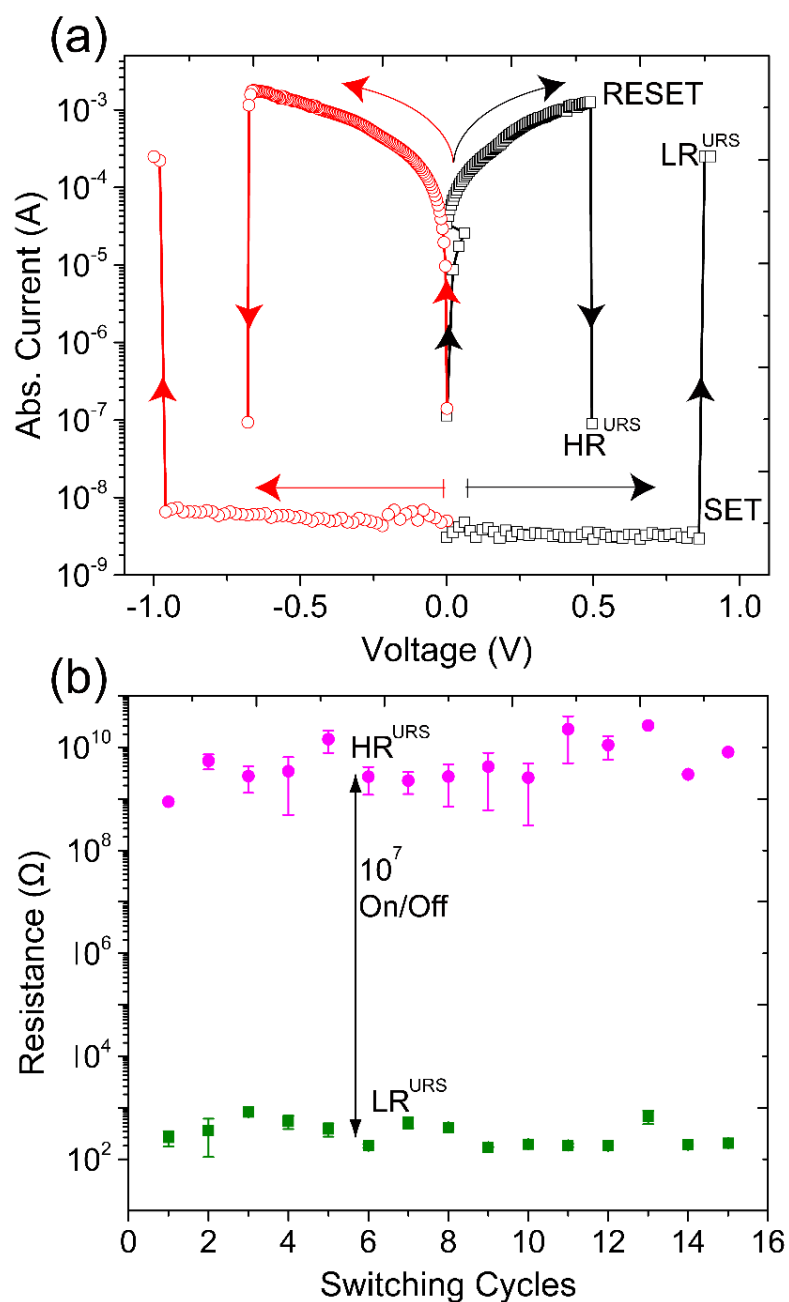


FIGURE 6.12. (a) Typical I-V characteristic in the unipolar regime. The black curve with the hollow boxes depicts the I-V curve for a SET compliance of 250 μA . To RESET the device the current compliance was removed and an increasing voltage sourced across the device. The increasing current response abruptly stopped and the test was ended. The red curve shows the same behaviour when the device is SET to the LR^{URS} with negative voltages. (b) Repeating the SET and RESET protocol of (a) in the forward bias multiple times gives an ON/OFF ratio of 10^7 . Resistances were read multiple times at 0.5 mV between SET and RESET events.

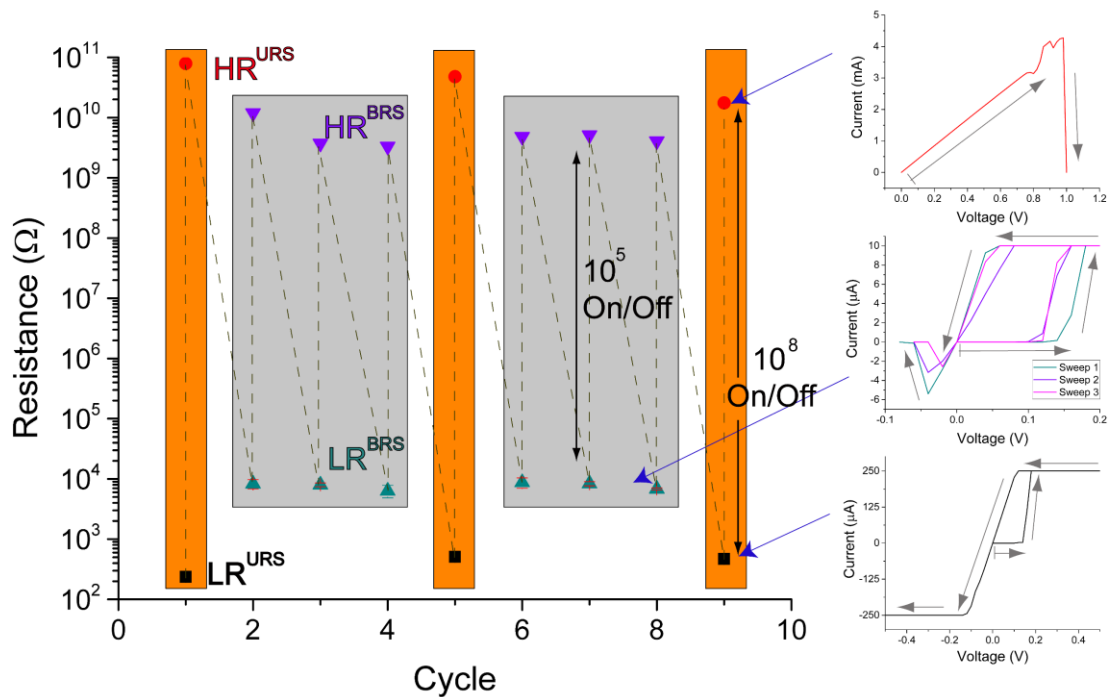


FIGURE 6.13 Controlled operation of URS and BRS by setting a current compliance of 200 μA and 10 μA respectively. The orange panels identify URS operation with the grey panels signifying BRS operation. The inset I-V curves to the right of the main panel are taken from the experimental data and show the typical URS RESET (top), BRS (middle) and URS (bottom) I-V response.

Through manipulation of the current compliance, controllable URS and BRS operation was demonstrated (Figure 6.13). URS was achieved with a current compliance value of 200 μA which resulted in a LR^{URS} of 200-400 Ω (bottom right inset I-V curve). The LR^{URS} was RESET by removing the current compliance and following the top right inset I-V curve. Using a low current compliance value of 10 μA , repeatable BRS was possible, displaying a LR^{BRS} of 7-8 $\text{k}\Omega$, as shown by the I-V curves in the middle-inset panel. After this, the current compliance could be raised to 200 μA and the sequence was repeated. The coexistence of the URS and BRS modes, in addition to the large ON/OFF ratio is highly desirable from a device perspective. Combining the advantages of the two modes can extend the application scope of the device and flexibility in memory architectures.

Operating in the threshold between the bipolar and unipolar regime (100 μA) results in interesting and unique behaviours, whereby the device can enter a semi-stable unipolar state after a repeated stimulus is applied. The current controlled transition is explored in Figure 6.14(a), after initially undergoing resistive switching

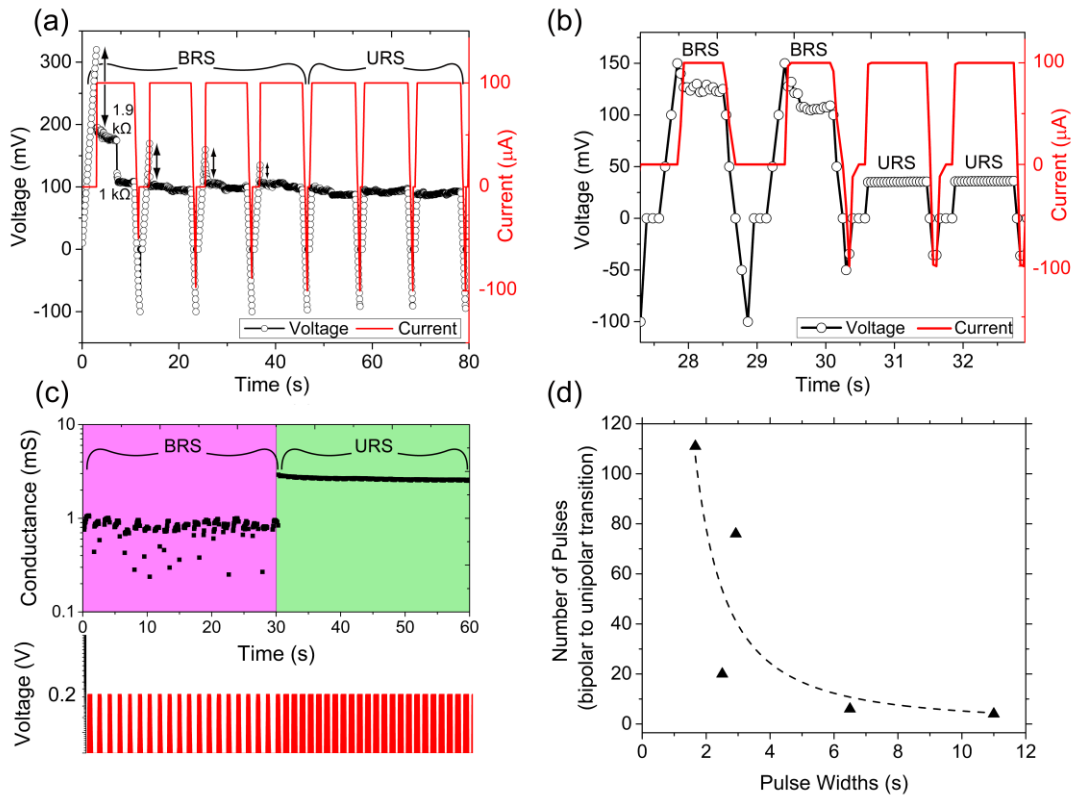


FIGURE 6.14. (a) V-t-I graph showing the initial and subsequent activation and transition of the low-resistance bipolar state to the low-resistance unipolar state. On the first sweep the device switches at a voltage of 300 mV to a current compliance of 100 μ A and a low-resistance state of 1.9 k Ω , after 4.2 s at current compliance the low-resistance state falls to 1 k Ω . Subsequent sweeps reach compliance at lower voltages until by sweep 5 the device is in a low-resistance unipolar state. (b) The signature of the transition from bipolar to unipolar mode. (c) Twenty positive (200 mV) and negative (-100 mV) pulses causing the device to transition from a bipolar mode to a unipolar mode with a noticeable change of the conductance after the transition. (d) By decreasing the pulse width, the number of pulses needed to transition from the bipolar to unipolar regime (at 100 μ A compliance current) follows a power law trend shown by the dashed line.

at 320 mV, the voltage drops to 200 mV to maintain the 100 μ A compliance current. After sustaining the current for 4 s, the resistance level drops to 1 k Ω , and a negative 100 mV pulse is then used to RESET the low resistance state. Repeating this procedure, the voltages required to reach the compliance current is observed to decrease until the device transitions into the unipolar regime. The signature for this transition is that the LRS can no longer be RESET by the negative pulse and the device remains ON (Figure 6.14(b)). The conductance of the device is observed to shift upwards as the device transitions from the BRS to a URS (Figure 6.14(c)). The power-law dependence of this transition is shown in Figure 6.14(d) where the pulse width

was varied and the number of pulses needed to transition counted. Another way to consider this is that the BRS to URS transition depends on the cumulative charge that flows through the system.

To determine the effect of the current compliance level on the lifetime of the low-resistance state (both BRS and URS), a sequence of ten (1.7 s) SET pulses were launched into the device each reaching a predetermined current compliance, which was 10 μ A in the case shown in Figure 6.15 (a). Each SET pulse was then followed by a series of 0.5 mV read pulses to interrogate the evolving resistance of the device. After the first two SET pulses, the device conductance quickly drops, however following the 7th through to the 10th SET pulse the device shows a stable response which was continuously monitored by a series of 0.5 mV read voltage until it completely decayed. The experiment was then repeated using a range of current compliances. Figure 6.15(b) shows the dependence of the device conductance with the current compliance value in a range from 1 nA to 10 mA. Immediately obvious is the power-law relationship between the device conductance and the current compliance. The universal relationship between switching parameters in ReRAM devices has been discussed in chapter 1, and has previously reported for a large variety of materials.^[37-40] The same power law relationship is seen to hold for unipolar, bipolar and threshold switching. The blue shaded box in Figure 6.15(b) highlights the volatile threshold switching regime that occurs at low current compliance where the device does not retain the LRS after the voltage is removed and subsequently read, the associated memory retention time is zero. At higher current compliance, the device enters the bipolar switching regime (grey shaded box), where the conductance of the device and the retention time can be programmed by setting a current compliance limit. The low-resistance state in the bipolar regime decays over time as previously described, and the rate of decay is controlled by the current that flows through the device, enabling retention times of seconds, minutes and hours. As the compliance is increased further, the device enters the URS regime (orange shaded box), where the conductance level and retention time start to saturate. A number of devices could be SET to a compliance current of over 1 mA, the retention time of all URS devices were stable for over 10⁶ s.

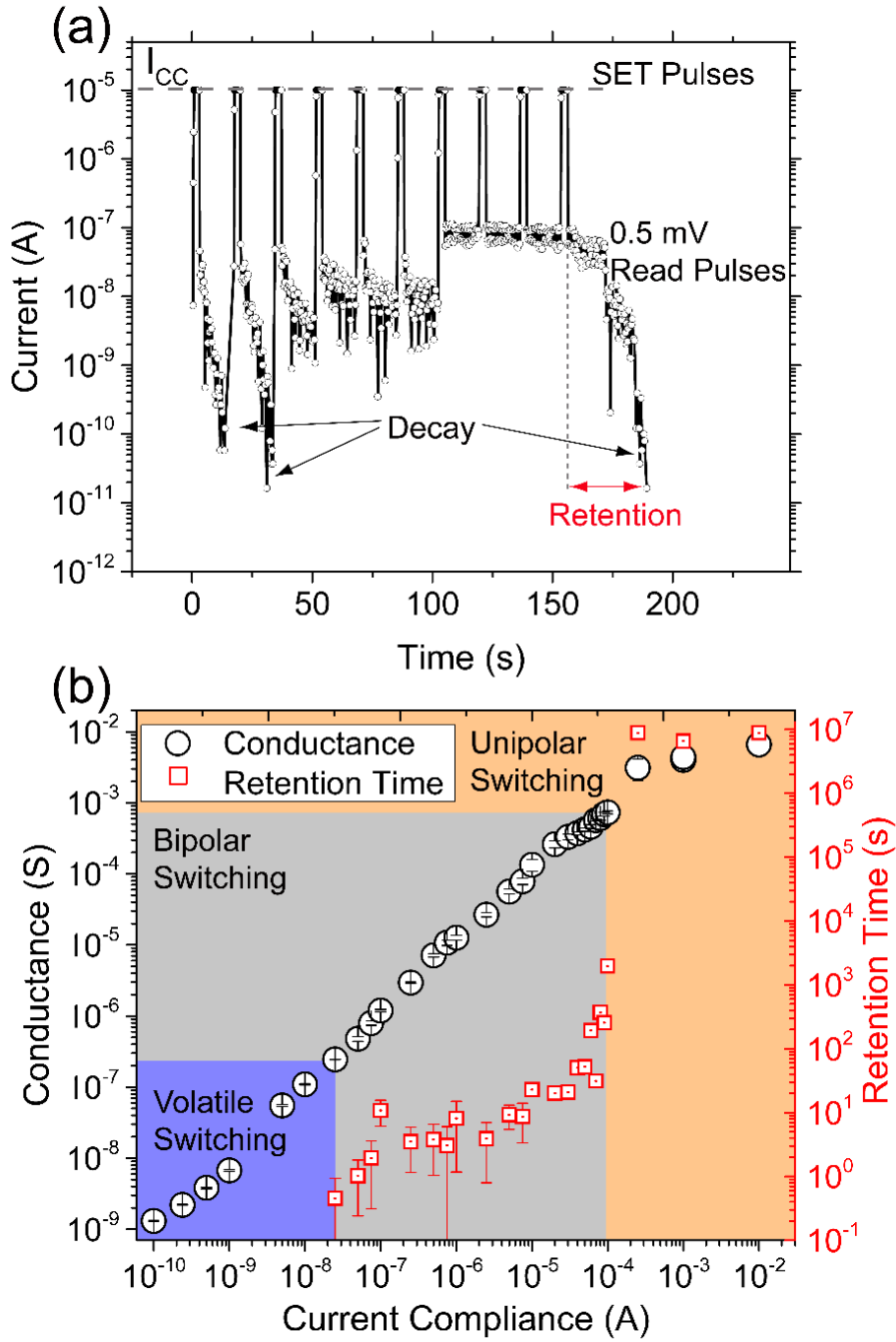


FIGURE 6.15. (a) I-t curve of ten 1.7 s pulses 15 s apart at different current compliance settings, between each SET pulse a (150 ms) 0.5 mV read pulse was applied, and used to monitor the decay of the LRS after the last SET pulse. (b) Incrementally increasing the current compliance in (a) and plotting the retention time and conductance of the average of 10 SET pulses versus the current compliance. For longer retention times, the conductance of the low-resistance unipolar state was checked each few days, then weeks at 0.5 mV.

The coexistence of a polarity dependent and independent regime retention times could allow for interesting new possibilities in a single device which can be programmed with both short-term and long-term memories depending on the current allowed to flow through the system. It provides flexible and adaptable responses which are necessary for implementing neuromorphic systems in hardware. Further work is necessary in developing control systems to take full advantage of the unique resistive switching behaviours.

6.7 Proposed Mechanism for Nonpolar Switching.

Many factors were considered in this study to elucidate the resistive switching mechanism, a diagram which illustrates the relationships between the structures, the current compliance level, the electrode composition and the I-V performances can be found in Figure 6.16. Due to the lack of controllable resistive switching for Au contacted amorphous and polycrystalline core-shell nanowires we do not consider oxygen vacancy species to be a determining factor in the resistive switching mechanism though their presence is expected. Furthermore, a continuous core is critical for current conduction. The Ag electrodes are required to provide a source of ions to mitigate against void formation in the core of the nanowire. These voids appear in core-shell nanowires contacted with Au electrodes as discussed in section 6.5.1

Based on the experimental evidence of resistive switching when contacted with Ag electrodes only, it is most likely that the switching mechanism is dominated by the formation of Ag CFs facilitated by the Ag inclusions and the Ag contacts. A schematic of the SET and RESET behaviours are outlined in Figure 6.17. We propose that under the application of a voltage bias, nanoionic redox processes occur, as described previously in other Ag systems.^[4, 34, 39, 40] Ag⁺ ions are formed via oxidation at the Ag anode and then migrate through the polycrystalline TiO₂ shell before being reduced at the Ag cathode. The tip of the electrodeposited filament grows back towards the anode as new Ag⁺ ions arrive through the lower activation energy pathways found at the grain boundaries of the polycrystalline TiO₂.^[40, 41] The growth of this filament is likely to occur in a ‘winner takes all’ scenario, with the favored CF extending out from the cathode and bridging the core and contact, as visualised by in situ studies.^[4] Once a CF bridges the Ag electrode and the Ag core of the wire, the second junction is

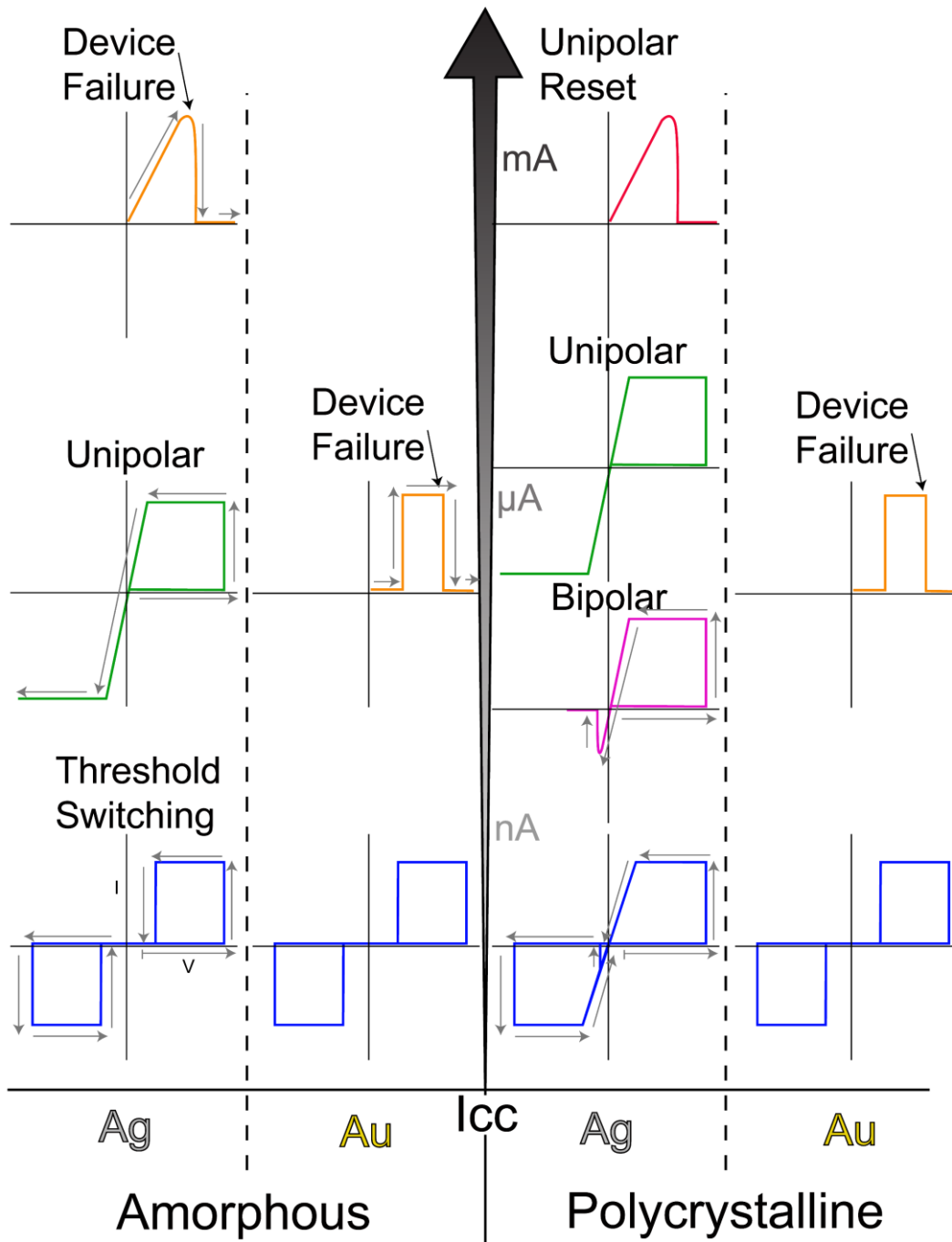


FIGURE 6.16. A schematic of the variables involved in characterising the nonpolar resistive switching behaviour in Ag@TiO₂ systems. The relationship between the amorphous (left) and polycrystalline (right) TiO₂ shell of the nanowires. The current compliance level increases from the bottom to the top of the diagram. The effect of the Ag (active, left) and Au (passive, right) electrode metal are also shown. All systems contacted with Au devices displayed volatile threshold switching. Only polycrystalline TiO₂ shell Ag core nanowires contacted with Ag electrodes displayed controllable URS and BRS behaviour.

polarised and the filament growth process occurs, as shown schematically in Figure 6.17(a). Once both junctions are bridged by a CF current suddenly increases to reach the current compliance limit and the LRS is established. The voltages depicted in the schematic only relate to the second CF growth, the transition voltages corresponding to the two-building processes are not shown. Once both junctions are bridged by a CF current flows to reach the current compliance and a LRS is established. The formation of the first and then the second junction sets an asymmetry in the system which at low current compliance allows for the bipolar behavior.

A key factor for the nonpolar operation is setting the device resistance and limiting CF growth by setting the current compliance. At very low settings, an incomplete CF forms which reduces the tunneling gap causing the threshold switching behavior. Increasing the current compliance limit slightly causes the formation of a bridging CF which is not pronounced enough to be stable to reoxidation and can be dissolved by applying a voltage of the opposite polarity, returning the device to a HRS state (Figure 6.17(b)). Application of an increasingly negative voltage causes the filaments to regrow, but in the opposite direction as before (not shown schematically) due to the symmetric construction of the device. When a voltage is applied with a high current compliance, the CF which physically bridges the Ag electrode and core can supply electrons for subsequent ion reduction allowing the CF to grow radially according to previously developed models.^[42] This is expected to result in a conical shape to the CF which is wider at the base and narrows along its length,^[4] as depicted in Figure 6.17(c). It has been previously shown for other Ag CF systems (Ag/Ge_xS_y/W thin-film cells) that the retention time of the ON-state improves as the value of LRS decreases.^[43] A feature which is evident from the retention times presented here. We also attribute the increased stability of the LRS with the formation of a more robust CF at larger current compliance values.^[44]

The proposed mechanism relies on the interplay between a field-driven bipolar device behaviour and the combined roles of field and thermal-driven behaviour during the URS regime.^[45] The URS CF formed at high current compliance requires an increased contribution from Joule heating/thermal diffusion to break the connection as illustrated by the thermally dominated hotspot in Figure 6.17(d). The effect of Joule

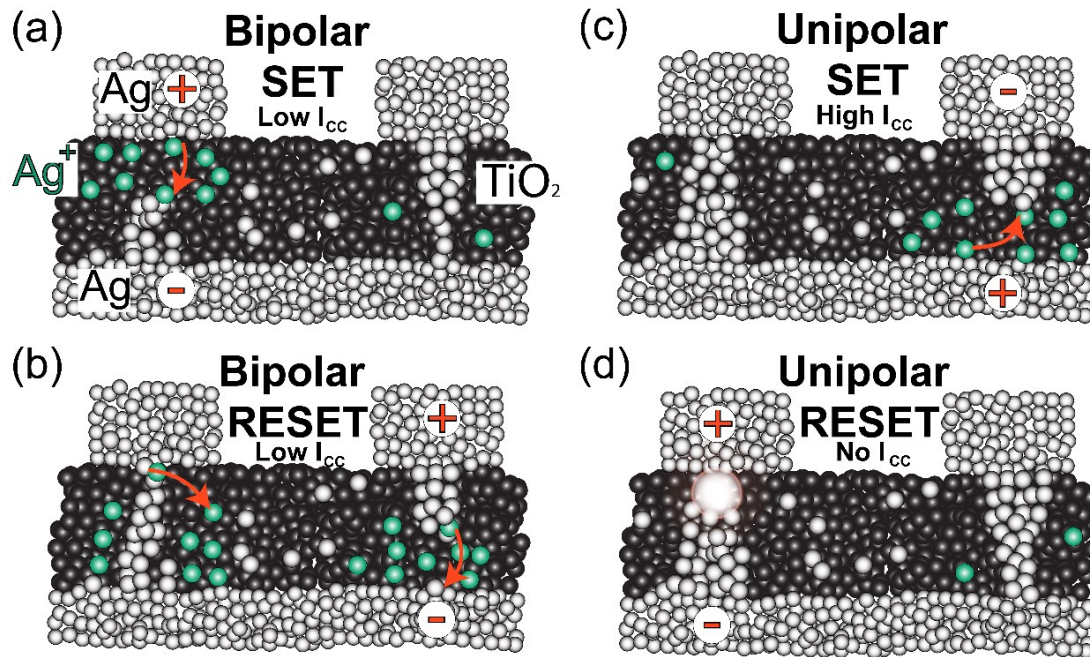


FIGURE 6.17. A Schematic of SET and RESET conditions in Ag@TiO₂(P) core-shell nanowires. (a) Under low current compliance conditions, bipolar SET is caused by the growth of Ag conductive filaments from the cathode toward the anode due to oxidation and subsequent electrodeposition of Ag to Ag⁺ ions (shown as the movement of green spheres via red arrows). (b) When the voltage bias is inverted, the conductive filament is withdrawn due to the same redox processes as given above and breaks. (c) With a higher current compliance imposed, a stronger filament can form, which is believed to be thicker and more robust than that formed with lower current limits. (d) RESET of the URS due to thermal breakdown (depicted as a radial hot spot) of the conductive filament caused by Joule heating under high current flow with no current compliance.

heating will be greatest at the narrowest part of the bridging CF, which is expected to be at the anode interface.^[4] Experimental evidence presented in this chapter shows that polycrystalline TiO₂ core-shell nanowires undergo controllable nonpolar resistive switching sustaining the large currents required for the URS RESET process. Grain boundaries in polycrystalline layers are known to provide favorable diffusion pathways and enhanced charge transport for migrating species^[40, 41, 44, 46] which are absent in amorphous layers. This is expected to result in the formation of well-defined, discrete CFs. The same cannot be said for amorphous TiO₂ shelled nanowires, where the shell is more homogeneous, and the nanowires ruptured when subjected to large current densities, as shown in section 6.5.2 .

It is interesting to contrast our results with those reported in the literature, where Ag/TiO₂ combinations have been explored in conventional thin-film two-

terminal memory cells, examples of these can be found in Table 6.1. In the work by Hu et al. URS switching was reported with $200 \mu\text{m}^2$ Ag contacts and an amorphous 50 nm TiO_2 dielectric spacer. SET voltages of 1 V were observed, with SET and RESET currents of 10 mA and 20 mA respectively reported.^[35] This work was mentioned previously in the chapter, where large currents were needed to induce unipolar switching in amorphous TiO_2 layer. Using a 100 μm diameter Ag top electrode and an inert Pt bottom electrode, Tsunoda et al. demonstrated BRS in 40 nm polycrystalline/rutile TiO_2 films, with SET voltages of 0.23 V.^[40] The voltages required in this study are similar to those observed in this work, the large diameter Ag top electrode, and antisymmetric nature of the device is expected to result in bipolar operation. Finally, Ghenzi et al. reports a device with a polycrystalline anatase TiO_2 layer with millimetre sized contacts showing initial URS behaviour which lasts for a hundred cycles then transforms into a BRS only device. This system is interesting as it also displays both unipolar and then bipolar switching. While this system demonstrates nonpolar operation, switching between these BRS and URS was not controllable, and the resistive switching mechanism offered to explain the results questionable.^[11]

TABLE 6.1. Two terminal thin-film memory cells that have been reported in the literature, resistive switching types and ON/OFF ratios.

author	cell composition	switching type	ON/OFF ratio
Hu et al. ^[35]	Ag/50 nm TiO_2 /Ag	URS	10^2
Tsunoda et al. ^[40]	Ag/40 nm TiO_2 /Pt	BRS	10^8
Ghenzi et al. ^[11]	Ag/100 nm TiO_2 /Si	BRS & URS	10^1 (BRS) 10^4 (URS)

The nonpolar switching observed in our study has some significant advantages over the previously reported thin-film devices given in Table 6.1. It is the only system to show controllable nonpolar operation. Furthermore, it is the first observation of controllable nonpolar operation in a core-shell nanowire device, the SET and RESET currents observed for the core-shell nanowires are significantly lower than those detailed previously for the relatively larger thin-film devices. This is attributed to the reduced contact area over which the applied electric field acts, which in turn leads to a focused CF growth and a reduced number of competing leakage channels. Scaling

effects were shown to have a consequence on the unipolar and bipolar behaviours of thin-film devices, as demonstrated in the work of Yanagida et al.^[47] core-shell nanowires also require the formation of two junctions, the asymmetry set in the device by formation of one connection and then the other could facilitate the BRS behaviors at low current compliance values and URS responses at higher current compliance values.

Further work is required to fully explore the benefits of the core-shell structure and its unique dual mode operation. Finally, core-shell nanowires provide an alternative platform to study the resistive switching phenomenon at nanoscale that allow the ability to tailor the electrical behaviours by engineering the properties of the outer dielectric layer.

6.8 Conclusions

In summary, we have investigated the requirements for resistive switching in Ag@TiO₂ core-shell nanowire devices. Core-shell nanowires were synthesized by two methods resulting in either amorphous or polycrystalline rutile TiO₂ shells surrounding an Ag core. HRTEM and EDX analysis identified the presence of Ag inclusions in the shell of both batches of core-shell nanowires. Neither nanowire system showed controllable resistive switching when contacted with Au electrodes, while dual mode operation of BRS and URS, known as nonpolar resistive switching was observed in core-shell nanowires with polycrystalline TiO₂ coatings contacted with Ag electrodes. The absence of resistive switching in Au contacted Ag@TiO₂(P) demonstrates that the interplay between the Ag electrodes, Ag inclusions and the Ag core is key to device operation. Operation of BRS and URS could be selected by defining the current compliance, resistance levels differed between URS and BRS modes, allowing them to be readily distinguished, and we postulate the Ag conductive filament associated with the two switching modes are directly related, with an increased current limit allowing for a more stable bridge of Ag atoms across the oxide which transitions from an electric field dominating mechanism (BRS) to a thermally dominant mechanism (URS). BRS was demonstrated with over 150 cycles and a tuneable retention time up to 10³ seconds; the conductance of the SET state could also be controlled by programming the pre-defined compliance current. ON/OFF ratios

were dependent on the compliance current as were memory retention times, ON/OFF ratios and memory retention were found to be highest in URS modes of 10^7 and 10^6 s respectively. These findings are important in the development of core-shell nanowire systems and highlight the influence of the shell microstructure and electrode composition. Moreover, the core-shell nanowire system is complimentary to thin-film studies, displaying how resistive switching behaviours can be unpredictable as devices are scaled to nm dimensions. Furthermore, it is the first report of controllable nonpolar operation in a single nanowire system; nonpolar operation allows for functional flexibility between short-term and long-term memory which is important for hardware based neuromorphic applications. Future work will include assembly of these core-shell nanowires into nanowire networks, the development of control systems to take advantage of the dual-mode switching and considering other core/shell material combinations to engineer resistive and memristive behaviors.

6.9 References

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7

CONCLUSIONS AND FUTURE WORK

This thesis has investigated the potential of metallic nanowires as transparent electrodes, semiconducting nanowires as memristive systems, and combined the two materials in a core-shell structure which presents unique resistive switching behaviours. Single nanowire systems, and networks of nanowires are objects and materials of growing technological interest due to the unprecedented level of control that is currently possible in synthesizing nanowires of various materials, diameters, lengths, and coatings. Randomly dispersed nanowires, known as nanowire networks allow for nanowires to be used as a functional material. Metallic nanowire networks appear to be promising substitutes to conventional transparent conducting materials such as ITO, while possessing major advantages such as ease of fabrication and flexibility. The large-scale integration of metallic nanowire networks in commercial devices could revolutionise display, touch screen, as well as numerous emerging applications including: flexible lighting, thin-film solar cells, electrostatic shielding, antistatic coatings and thin-film heaters.

The study of metallic nanowire networks has been typically focused on characterising and optimizing properties such as nanowire geometry, synthesis techniques, deposition methods, and post-fabrication processing. These approaches represent a top-down method to optimization and seeking out of new materials other than Ag to compete with ITO. Combining simulation with experiment provides a useful tool to better understand all the parameters which combine and influence the performance of the network. However, to date, these simulations have neglected to incorporate the resistance component of the material and operated on assumptions of a junction dominated resistance. This thesis has presented a bottom-up approach to studying networks, by focusing on the individual components of the network, the nanowire and the junction, and using a part-to-whole approach in the development of a model which can predict the performance of metallic nanowire network systems. By

developing our understanding of the nanowire junction and its role in determining network behaviour, it is then possible to design materials for specific purposes, or recommend currently available materials for targeted applications.

In this work, a systematic characterisation of the resistivity and junction resistance of three metallic nanowire systems was performed. This includes work published in the most comprehensive study on the fundamental electrical properties of single Ag nanowires to date. The resistance contribution from the nanowires was accounted for by firstly measuring the resistivity of individual Ag nanowires which was found to be slightly higher than bulk values. Measurements of the two overlapping nanowires were then performed using the four-probe method, which removes the system and lead resistance from the measurement. After high-resolution SEM imaging of the nanowire geometry an accurate value for the resistance of the junction was extracted. A distribution of junction resistances was established by this method, having an average of 33 Ω and median of 11 Ω . Using a thermal annealing step post-deposition, it was revealed that, at an individual junction level, both electrical activation and thermal annealing can form low-resistance junctions with morphological changes induced by annealing providing no benefit to conduction. The electrical properties of electroformed Cu nanowires and nanowire junctions were also measured. This nanowire system has been reported to have optoelectronic performances which rival Ag nanowire networks but suffers from the formation of native oxides making measurement of individual junctions difficult. The native oxide provides for interesting resistive switching behaviours, while not investigated in this work, should also be considered as an opportunity to develop programmable materials. Cu nanowires were found to exhibit an average resistivity slightly higher than bulk and a junction resistance of 205 Ω . To prevent the formation of the native copper oxides, Cu nanowires were coated 5-10 nm of Ag, the electrical behaviours of these metallic core-shell systems were also studied. Investigating individual nanowires allowed for the observation of interesting electrical resistive switching behaviours which may not be evident in network scale measurements. When electrically characterised, resistivity values were found to be much higher than either the Cu or Ag system, and junction resistance measurements yielded values over twice that of Cu nanowire junctions with an average resistance of 424 Ω . These results represent a step

towards the development of a rigorous computational model and a materials-by-design approach for nanowire networks, investigating the fundamental material properties of individual nanowires to chase the limits of performance of a collective network.

These results have significant implications for research on metallic nanowire networks. It is the first study to systematically characterise the material and junction resistance of a range of metallic nanowire materials. Particularly for Ag nanowires where previous studies have consistently overestimated the resistance contributions from the junctions, either by assuming a junction dominated resistance component in simulation work, or through failure to perform multiple 4-probe measurements and failing to take contact resistances into account. With this said, the results obtained for Ag nanowires align well with those from by Selzer et al. which were published shortly after our work in 2016. Junction resistance values of $25\ \Omega$ were reported for annealed samples, and $529\ \Omega$ for non-annealed junctions. This spread in junction resistance values is also observed for the junctions described in this work, where resistive junctions were found to exist regardless of electrical or thermal processing. The origin of these outliers is unknown; however, their presence, even at small percentages has the effect of limiting the ultimate sheet resistance of the film. Hopefully, this work will motivate and inform the search for fabrication and processing techniques that optimise network connectivity, reduce the presence of outliers, and ultimately see the full potential of nanowire network based transparent conductors realised.

To combine experiment and simulation, a selective area spray deposition method was used to fabricate isolated Ag nanowire networks. Topographical replicas of these networks were made in a virtual space by digitising the coordinates of each nanowire to simulate the networks electrical properties accurately. A multi-nodal representation method was employed which not only accounts for the resistance of the junction component of the sheet resistance but also determines the contribution of the network skeleton. The network skeleton allows for an ultimate performance of the network to be established, this considers all the junctions as perfectly conducting. This treatment of the network is important as it sets fundamental limits for conducting for each network. By varying the average junction resistance and aligning the simulated sheet resistance with the experimentally measured sheet resistance, an excellent agreement was observed with respect to the junction resistance values measured in

chapter 3 for Ag nanowires. The deconvolution of material and junction resistance allows for a deeper analysis of the network to be performed; it also allows the model to be flexible to materials other than Ag.

Using the multi-nodal model and the electrical properties measured in chapter 3; Ag, Cu and Cu@Ag nanowire networks were simulated with aspect ratios inspired by the literature values in a range from 166 to 1000. To relate the nanowire density of the network to an optical transmittance parameter and enable to comparison of simulated and experimental results, an optical model based on Mie light scattering was used. This calculated the optical transmittance of the metallic nanowire networks with respect to their geometrical aspect ratio and area coverage. Using this first principles approach, which depends on Ohm's law, Kirchhoff's system of equations, experimentally measured resistivity and junction resistance values, simulated Ag nanowire networks accurately matched the literature reported networks over a range nanowire aspect ratios. It was also shown that there was no correlation between a linear fitting factor required to unite experimental and simulated data across a range of literature reported data making it impossible to predict the performances of these methods using a semi-empirical approach.

These results present an important combination of experimental, simulation and theory, we demonstrate that simulation of metallic nanowire networks is a viable approach for exploring the potential applications of a range of materials and guiding the synthesis of systems for specific needs. Metallic nanowire networks are well suited as replacements for ITO in a wide variety of transparent conducting applications. The development of a first-principles model which describes the optoelectronic performances of metallic nanowire networks represents a step towards a materials-by-design approach for transparent conductor applications. Future work will focus on incorporating Mie theory into the computational model so that it reports a transmittance value for the simulated networks, and determining adjustments to more accurately describe the behaviour over the entire spectrum of nanowire aspect ratios

The metallic nanowires considered in the development of the computational model possessed either a polymeric (PVP), native (oxide), or engineered (Ag on Cu nanowires) passivation layer. Passivation layers are ubiquitous and necessary in the field of nanoscience for directing growth, preventing aggregating in solution, or

functionalising the nanowire. The electrical breakdown of PVP is an irreversible switch, resulting in a permanent breakdown of the insulating layer. It has been previously shown by our group that the controlled electrical breakdown of this polymeric layer can be used to produce materials with tuneable conductivities and emergent behaviours. It is therefore our goal to engineer the coating of Ag nanowires to add new and novel functionality and incorporate these materials into networks. One highly desirable response is the memristive behaviour demonstrated by the TiO₂ material.

Single TiO₂ nanowire devices use the same materials as conventional thin-film memory cells but arranged in a lateral structure, where the two electrodes lie in the same horizontal plane, and the current is conducted horizontally between them. The relatively large separations between the electrodes (μm scale), when compared to lateral cells (nm scale), separates the behaviours of the device and the two electrode regions. The generation of oxygen vacancies by electrochemical reactions allows for the dynamical evolutionary behaviour where the current level could be incremented and decremented using positive and negative voltages; this contrasts with most thin-film cells where abrupt changes in resistance level are experienced as large concentrations of charge carriers can span the short channel between the two electrodes.

Through an electroforming step, the resistance of the wire was reduced from $10^{12} \Omega$ in the pristine state to $10^8 \Omega$ in the developed state. The effect of the forming voltage was shown to vary exponentially with the forming current. A forming process, either by a steady voltage hold, or subjecting the device to multiple voltage sweeps in a single direction is critical to develop an asymmetry and produce a population of charge carriers which modulate the Schottky-like barrier height and control the transport at the Au electrode/semiconductor interface. The dynamical analogue response of the nanowire was exploited to demonstrate six and eleven memory levels in a single nanowire device by defining levels of conductance which could be reached through repeatedly pulsing the device. Voltage and optical stimuli were used to elicit an enhancement in the current response. The maximum enhancement factors varied between four and eight, with voltages required to reach this value ranging from 0.8 V to 1.6 V. The associative memory effects demonstrated with optical and voltage

stimuli are unique and open the possibility for novel low-power smart sensors or neuromorphic hardware which rely on highly correlated inputs.

The effects of replacing one or more of the Au electrodes with Ag was also investigated. By contacting the TiO₂ nanowire with an Ag electrode threshold switching and degradation of the wire was observed, the movement of Ag species along the single crystalline TiO₂ wire was characterised by EDX analysis of devices prior and post electrical measurement. The single wire TiO₂ system, as a simple two terminal devices spanning μm s in distance displays fascinating electronic and optical properties. The improvement of the current response could be obtained by shorting the separation between the electrodes. However this requires precise lithography. The highly resistive nature of the TiO₂ material makes realisation of TiO₂ nanowire networks impractical with large voltages required to drive a small current response. TiO₂ was incorporated as the active element of core-shell nanowires which combined a highly conductive Ag core with a TiO₂ shell, shortening the active switching region to the nm scale.

Core-shell nanowires were synthesized by two methods resulting in either amorphous or polycrystalline rutile TiO₂ shells surrounding an Ag core. Transmission electron microscopy and elemental analysis identified the presence of Ag inclusions in the shell of both batches of core-shell nanowires. Neither nanowire system showed controllable resistive switching when contacted with Au electrodes, while dual-mode operation of a voltage polarity dependent and independent mode, known as nonpolar resistive switching was observed in core-shell nanowires with polycrystalline TiO₂ coatings contacted with Ag electrodes. The absence of resistive switching in Au contacted Ag@TiO₂(P) demonstrates that the interplay between the Ag electrodes, Ag inclusions and the Ag core is key to device operation. Operation of bipolar and unipolar resistive switching could be selected by defining the current compliance during activation of the device, resistance levels differed between both modes, allowing them to be readily distinguished. We postulate the Ag conductive filament associated with the two switching modes are directly related, with an increased current limit allowing for a more stable bridge across the oxide which transitions from an electric field dominating mechanism (bipolar mode) to a thermal dominating mechanism (unipolar mode). Bipolar resistive switching was demonstrated with over

150 cycles and a tuneable retention time up to 10^3 seconds; the conductance of the low-resistance state could also be controlled by programming the pre-defined compliance current. ON/OFF ratios were dependent on the compliance current as were memory retention times, ON/OFF ratios and memory retention were found to be highest in unipolar mode of 10^7 and $>10^6$ s respectively. These findings are important in the development of core-shell nanowire systems and highlight the influence of the shell microstructure and electrode composition. Moreover, the core-shell nanowire system is complimentary to thin-film studies, displaying how resistive switching behaviours can be unpredictable as devices are scaled to nm dimensions. Furthermore, it is the first report of controllable nonpolar operation in a single nanowire system; nonpolar operation allows for functional flexibility between short-term and long-term memory which is important for neuromorphic applications. Future work will include assembly of these core-shell nanowires into nanowire networks, the development of control systems to take advantage of the dual-mode switching and considering other core and shell material combinations to engineer resistive and memristive behaviors.