npj | 2D Materials and Applications

www.nature.com/npj2dmaterials

ARTICLE OPEN

Electrical devices from top-down structured platinum diselenide films

Chanyoung Yim[1,2], Vikram Passi[1,3], Max C. Lemme[1,3], Georg S. Duesberg[2,4,5], Cormac Ó Coileáin[4], Emiliano Pallecchi[6], Dalal Fadil[6] and Niall McEvoy[4,5]

Platinum diselenide ($PtSe_2$) is an exciting new member of the two-dimensional (2D) transition metal dichalcogenide (TMD) family. It has a semimetal to semiconductor transition when approaching monolayer thickness and has already shown significant potential for use in device applications. Notably, $PtSe_2$ can be grown at low temperature making it potentially suitable for industrial usage. Here, we address thickness-dependent transport properties and investigate electrical contacts to $PtSe_2$, a crucial and universal element of TMD-based electronic devices. $PtSe_2$ films have been synthesized at various thicknesses and structured to allow contact engineering and the accurate extraction of electrical properties. Contact resistivity and sheet resistance extracted from transmission line method (TLM) measurements are compared for different contact metals and different $PtSe_2$ film thicknesses. Furthermore, the transition from semimetal to semiconductor in $PtSe_2$ has been indirectly verified by electrical characterization in field-effect devices. Finally, the influence of edge contacts at the metal–$PtSe_2$ interface has been studied by nanostructuring the contact area using electron beam lithography. By increasing the edge contact length, the contact resistivity was improved by up to 70% compared to devices with conventional top contacts. The results presented here represent crucial steps toward realizing high-performance nanoelectronic devices based on group-10 TMDs.

npj 2D Materials and Applications (2018)2:5 ; doi:10.1038/s41699-018-0051-9

INTRODUCTION

Over the last decade, the need for further miniaturization and increased functionality of electronic devices has triggered massive research in two-dimensional (2D) channel materials such as graphene and transition metal dichalcogenides (TMDs).[1–3] Reliable electrical contacts between devices/materials and metal electrodes are crucial, as the contact resistance can strongly influence or dominate the behavior of the entire device. Depending on the contact status at the metal–channel junction, Ohmic or Schottky, the flow of charge carriers across the device can be decisively deteriorated.[4] Thus, the reliable formation of contacts to each new channel material proves challenging and has to be investigated in detail.

Graphene has been considered one of the most promising candidates for future nanoelectronics due to its unique electrical properties.[5] Contact resistivity in graphene devices has been widely studied and a wide range of contact resistances (~10^2 to ~10^3 Ω µm) has been reported, depending on the contact metal, surface states, and contact geometry.[6–9] Following the impressive advances in graphene, various layered 2D TMDs have been tested in a wide range of device applications, including field-effect transistors (FETs),[10,11] photodetectors,[12–14] and sensors.[15,16] Up to now, molybdenum and/or tungsten-based materials have been the main focus of 2D TMD research, and the majority of studies on electrical contacts to 2D TMDs have concentrated on these materials.[17–19] However, compared to classical silicon-based devices, these TMDs still show relatively inferior performance and less environmental stability in device applications.[20–23] Moreover, the high growth temperature (>600 °C) associated with TMD synthesis by chemical vapor deposition (CVD), which is typically used for large-scale TMD film synthesis,[24–26] can limit their compatibility with current semiconductor processing.

On the other hand, there are other relatively unexplored members of the TMD family such as group-10 TMDs. Recently, the electronic structure and properties of these materials have been theoretically evaluated and, as a consequence of their promising characteristics, they have been proposed for use in electronic device applications.[27,28] Platinum diselenide ($PtSe_2$) is one such group-10 TMD which is known to be a semimetal in bulk form with zero bandgap.[29] Theoretical calculations suggested a transition from semimetal to semiconductor with reduced $PtSe_2$ thickness[27,30] and it was shown experimentally by Wang et al. that monolayer $PtSe_2$ has a bandgap of ~1.2 eV.[31] In addition, we recently reported that layered $PtSe_2$ can be synthesized in a scalable manner at low temperature (400 °C) by thermally assisted conversion (TAC) of pre-deposited Pt layers and utilized as the active material in optoelectronic and gas-sensor devices.[32,33] Such low-temperature synthesis may potentially have a high impact on practical device applications since it allows integration of $PtSe_2$ with standard semiconductor back-end-of-line processing.[34–36] In this regard, it is critical to evaluate electrical properties and contacts to $PtSe_2$ in electronic devices.

[1]Department of Electrical Engineering and Computer Science, University of Siegen, Hölderlinstraße 3, 57076 Siegen, Germany; [2]Institute of Physics, EIT 2, Faculty of Electrical Engineering and Information Technology, Universität der Bundeswehr München, Werner-Heisenberg-Weg 39, 85577 Neubiberg, Germany; [3]Faculty of Electrical Engineering and Information Technology, RWTH Aachen University, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany; [4]Centre for the Research on Adaptive Nanostructures and Nanodevices (CRANN) and Advanced Materials and BioEngineering Research (AMBER), Trinity College Dublin, Dublin 2, Ireland; [5]School of Chemistry, Trinity College Dublin, Dublin 2, Ireland and [6]Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN), 59652 Villeneuve d'Ascq, France
Correspondence: Niall McEvoy (nmcevoy@tcd.ie)

Received: 28 November 2017 Revised: 31 January 2018 Accepted: 2 February 2018
Published online: 28 February 2018

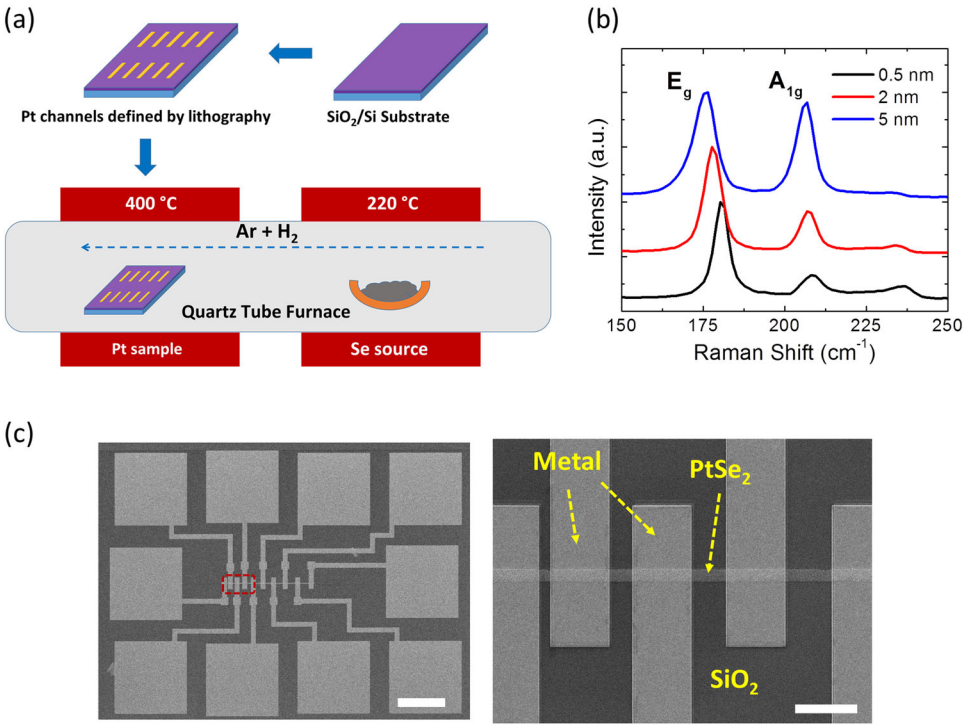

Fig. 1 Device fabrication and characterization. **a** Schematic diagram of the $PtSe_2$ channel synthesis process using a TAC method. **b** Raman spectra of $PtSe_2$ films of different Pt deposition thickness normalized to the E_g mode intensity. Initial Pt deposition thicknesses are 0.5, 2, and 5 nm. **c** SEM image of the fabricated $PtSe_2$ channel device with a TLM structure (left, scale bar 50 μm) and its enlarged image (right, scale bar 5 μm). The contact spacing increases from 1 to 9 μm with a step of 1 μm

Here, $PtSe_2$ channels with controlled dimensions and thicknesses were grown using a TAC method. Electron beam lithography (EBL) was used to fabricate transmission line method (TLM) structures to extract contact resistivity and sheet resistance of the $PtSe_2$ devices. In addition, electrical characterization of $PtSe_2$ FETs was conducted to study the charge-transport characteristics of the $PtSe_2$ devices. Finally, we investigated the effect of "edge" or side contacts on the contact resistivity using well-defined hole patterns in the contact region of the $PtSe_2$ channel.

RESULTS AND DISCUSSION

$PtSe_2$ device channels were synthesized by direct selenization of pre-deposited Pt layers with different thicknesses. As reported in our previous studies,[32,33] the $PtSe_2$ synthesized by a TAC process has a polycrystalline structure, which is also observed in scanning electron microscopy (SEM) images (Fig. S1 of the Supplementary Information) of the $PtSe_2$ film surface. According to atomic-force microscopy (AFM) measurements of the thicknesses of Pt layers before and after selenization, it has been found that the initial Pt thickness expands approximately four times after selenization. Details of the AFM characterization are presented in Figs. S2 and S3 of the Supplementary Information. Previous studies on TAC growth of TMDs have shown that the orientation of the resultant films depends on the starting metal thickness with thicker metal films leading to horizontal growth, perpendicular to the growth substrate.[37] A recent study on the electrocatalytic properties of $PtSe_2$ indicated that this holds true for TAC growth of $PtSe_2$, with significant contributions from perpendicular growth seen for $PtSe_2$ thicknesses >20 nm.[38] This is consistent with our observations, our $PtSe_2$ films looked "cloudy" if thick (>5 nm) Pt films were used and so for the purpose of this study only Pt films with thickness of 5 nm or less were used. In this thickness regime we expect the growth to be mostly vertical, or parallel to the growth substrate. A schematic diagram of the film growth process is presented in Fig. 1a. First, the channel area was defined on the substrates by EBL. After Pt deposition and lift-off, the Pt samples were selenized via a TAC method. Raman spectra of the $PtSe_2$ layers grown from various Pt thicknesses (0.5, 2, and 5 nm) are shown in Fig. 1b. Two prominent peaks at ~177 cm^{-1} and ~210 cm^{-1} can be seen in the spectra. They represent the typical Raman fingerprint of layered $PtSe_2$ with a 1T type crystal structure and are related to the E_g (~177 cm^{-1}) and A_{1g} (~210 cm^{-1}) Raman active modes, respectively.[32] The E_g mode indicates an in-plane vibrational mode of Se atoms and the A_{1g} mode is an out-of-plane vibration of Se atoms. As the films get thicker, a slight red shift of the E_g mode is observed, alongside an increase in the relative intensity of the A_{1g} mode, consistent with previous reports.[32,33] Such an increase in the relative intensity of the A_{1g} mode implies a greater out-of-plane contribution, which may be due to enhanced van der Waals interactions in the thicker films. Additionally, we investigated the sulfurization of Pt films using a S source in place of Se. Interestingly, our preliminary studies suggest the formation of PtS rather than PtS_2 as detailed in Fig. S4 of the Supplementary Information.

TLM measurements were used at room temperature to determine the contact resistance of the $PtSe_2$ devices in this work.[39] TLM structures were patterned on the substrates with predefined $PtSe_2$ channels by EBL. The contact spacing was varied from 1 to 9 μm in 1 μm steps. SEM images of a TLM structure on a $PtSe_2$ channel are shown in Fig. 1c. Two representative metals with low and high work functions, Ti and Ni, were chosen and used to contact the $PtSe_2$ channels, both of which were selenized from 5 nm thick initial Pt layers. The contact resistances of these were compared through dc current–voltage (I–V) measurements of the TLM structures. Figure 2a and b shows I–V data measured from Ti and Ni-contacted $PtSe_2$ TLM structures with a channel

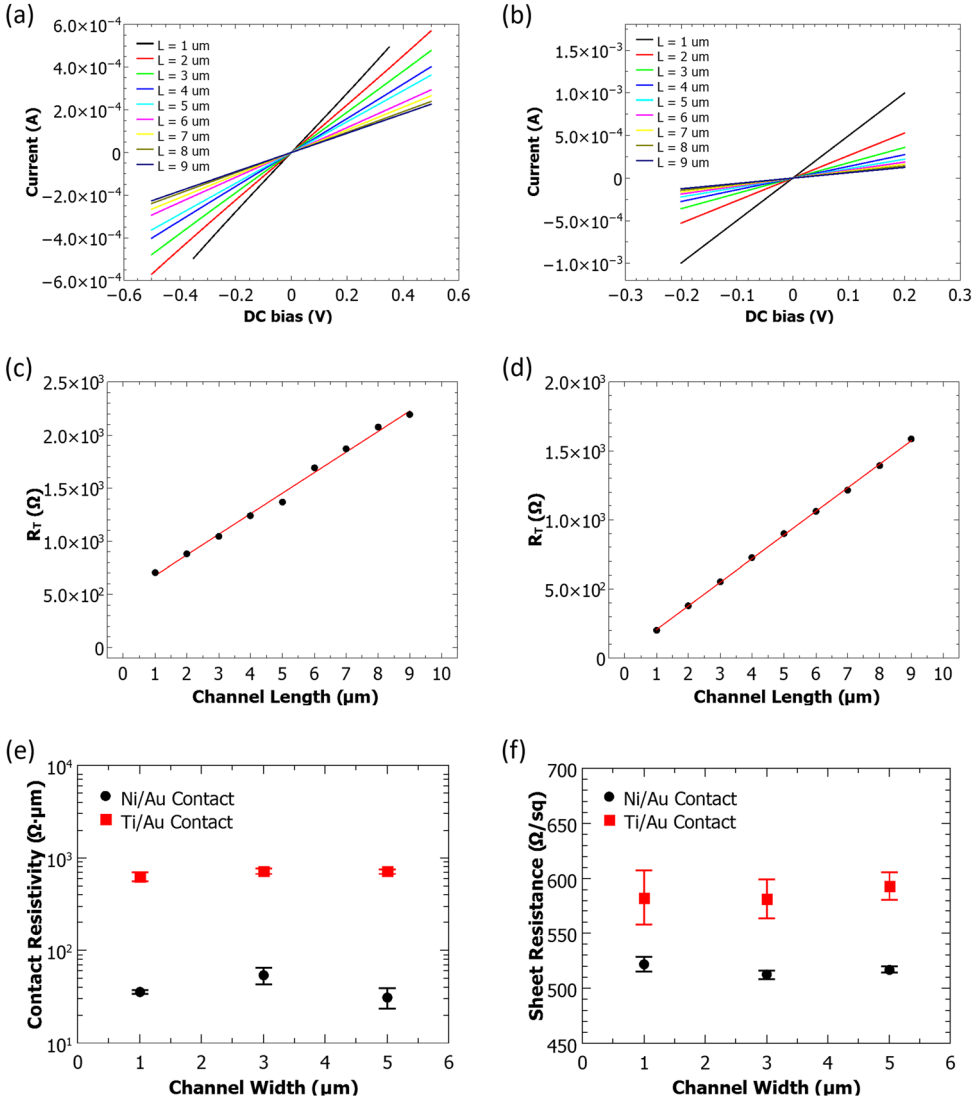

Fig. 2 Electrical characterization of $PtSe_2$ TLM devices. I–V plots of the TLM structure with various $PtSe_2$ channel length values (L) for **a** Ti/Au and **b** Ni/Au-contacted devices, and the associated plots of the total resistance (R_T) vs. $PtSe_2$ channel length for the **c** Ti/Au and **d** Ni/Au-contacted devices. The initial Pt deposition thickness and the channel width of the devices are 5 and 3 μm, respectively. **e** Contact resistivity and **f** sheet resistance values extracted from the TLM measurements for the Ti/Au and Ni/Au-contacted devices with different $PtSe_2$ channel width values

width of 3 μm, respectively. The linear I–V curves indicate that both Ti and Ni electrodes form good ohmic contacts with $PtSe_2$ channels. Values of the contact resistance for each metal and the sheet resistance of the $PtSe_2$ channel can be extracted by extrapolation from linear fits of the plots of the total resistance (R_T) vs. the contact spacing (Fig. 2c, d), wherein the *y*-intercept and the slope of the fits provide information on the contact resistance and sheet resistance. Figure 2e shows contact resistivity values of each metal for different $PtSe_2$ channel widths, where the contact resistance values were normalized to channel width for direct comparison. It was found that the Ti-contacted device had a contact resistivity more than one order of magnitude higher than the Ni-contacted device. Considering the work function values of the contact metals (Ti: 4.3 eV, Ni: 5.2 eV), we observe that the metal with a higher work function has a lower contact resistance with $PtSe_2$. The sheet resistance values of the $PtSe_2$ channels in Fig. 2f are quite similar to each other (500–600 Ω/□) for both contact metals, which can be expected from the identical $PtSe_2$ channel thicknesses for both devices.

Ni-contacted TLM structures were then fabricated on $PtSe_2$ channels with different thicknesses, which were selenized from 0.5, 2, and 5 nm thick initial Pt layers. The Ni–$PtSe_2$ contact resistivity and sheet resistance were extracted by analyzing the TLM measurement data, R_T vs. contact spacing, in Fig. 3a and b. The extracted values of the contact resistivity and sheet resistance are plotted against the film thickness in Fig. 3c and d. When the same Ni electrodes were deposited on the $PtSe_2$ channels with various thicknesses, devices with thinner $PtSe_2$ channels show much higher contact resistivity and larger sheet resistance. This can be attributed to the nature of layered $PtSe_2$, whereby the electronic character changes from semimetallic to semiconducting as the number of layers decreases.[27,30,31] The thinner $PtSe_2$ can be expected to be more semiconducting than the thicker, resulting in higher contact resistivity with metal electrodes as well as larger sheet resistance. The semiconducting characteristics of the thinner $PtSe_2$ are also supported by the results of electrical measurements at low temperatures. The I–V plots of a $PtSe_2$ film, derived from a 0.5 nm thick Pt layer and measured in a temperature range of 78–340 Kelvin (K), reveal clear temperature dependence. As the

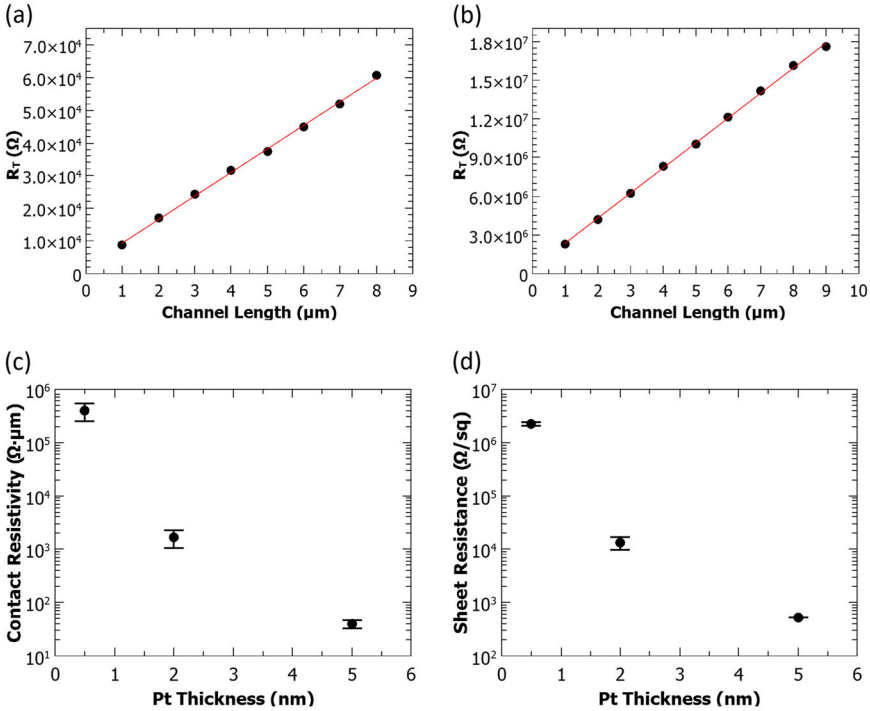

Fig. 3 Investigation of the effect of $PtSe_2$ thickness on device performance. Plots of the total resistance (R_T) vs. $PtSe_2$ channel length for the Ni-contacted TLM structures with different $PtSe_2$ thicknesses, synthesized from the **a** 2 nm and **b** 0.5 nm thick Pt layers with 1 μm of channel width. Summary of **c** contact resistivity and **d** sheet resistance values extracted using TLM method for the different $PtSe_2$ thicknesses

temperature is reduced there is a consistent rise in resistance, indicating the semiconducting nature of the $PtSe_2$. Details of the temperature-dependence measurements are presented in Fig. S5 of the Supplementary Information.

Charge-transport measurements of $PtSe_2$ FETs were carried out at room temperature in ambient conditions to further investigate the electrical properties of $PtSe_2$ films with different thicknesses. $PtSe_2$ channels with a length of 5 μm and a width of 1 μm were probed via two separate metal source and drain electrodes, with gate biases applied to the silicon substrate in a back-gate configuration. The output characteristics of the FETs with $PtSe_2$ channels synthesized from 5, 2, and 0.5 nm thick initial Pt layers are plotted in Fig. 4a–c, respectively. For all devices, the drain–source current (I_{ds}) increases linearly with the applied dc drain–source voltage (V_{ds}), implying good ohmic contact of the Ni electrodes with the $PtSe_2$ channels. As expected, the device with a thicker $PtSe_2$ layer shows higher conductivity. The gating characteristics of the FETs were examined under a dc back-gate bias (V_{gs}) in the range of −80 to +80 volts (V). While the FETs with $PtSe_2$ channels synthesized from the 5 and 2 nm thick Pt layers show hardly any gate dependence, the $PtSe_2$ FET from the 0.5 nm thick initial Pt layer shows a clear gate dependence with p-type conduction. This is consistent with the previous results that contact formation with a high work function metal reduces the contact resistance at the metal-$PtSe_2$ junction. Also, this data supports the hypothesis that $PtSe_2$ becomes more semiconducting as it gets thinner. The field-effect mobility (μ) was extracted from the transfer characteristics of the $PtSe_2$ FETs selenized from the 0.5 nm thick Pt layer in Fig. 4d, using the expression $\mu = [L/(W \times C_{ox} \times V_{ds})] \times [\partial I_{ds}/\partial V_{gs}]$, where L is the channel length, W is the channel width, C_{ox} is the capacitance of the insulating layer between the gate and the channel. The mobility was estimated to be a maximum of 0.6 $cm^2 V^{-1} s^{-1}$, which is lower than previously reported values (7–210 $cm^2 V^{-1} s^{-1}$) obtained from high-temperature CVD-grown single crystalline, or mechanically exfoliated $PtSe_2$.[40,41] However, considering the benefits of our growth process, namely, the low synthesis temperature, scalability and ease of controlling layer thickness, this is quite striking. Such a relatively low mobility likely originates from the polycrystalline structure, with randomly distributed $PtSe_2$ grains, observed for TAC-grown $PtSe_2$.[32,33] This polycrystallinity, and associated thickness variation over large areas, is also the most likely cause of the relatively poor gate control seen in our gate-response curves. Additional efforts to optimize the synthesis process, through the use of epitaxially deposited Pt or highly crystalline substrates, and the realization of local top-gates with high-k dielectrics, are expected to improve the mobility. Furthermore, better control over the Pt deposition conditions, and the use of post-growth treatments such as annealing, can be expected to improve the film uniformity leading to better gate control. In order to assess the stability of $PtSe_2$ channels, we repeated I–V measurements on the same device ($PtSe_2$ channel with a length of 5 μm and a width of 1 μm) in ambient conditions with an interval of 20 days and monitored the variation of R_T of the device for 40 days. As presented in Fig. S6 of the Supplementary Information, the measured R_T was 8.1 MΩ from the first measurements, 8.3 MΩ from the second measurements after 20 days, and 9.4 MΩ from the last measurements after 40 days. This indicates that the $PtSe_2$ channel is quite stable with a resistance increase of 15% of the initial value after 40 days without any passivation or post-treatment.

Lastly, we investigated the effect of "edge contacts" on the contact resistance of $PtSe_2$ TLM structures. There have been continuous efforts to achieve low contact resistance in 2D-material-based devices, including local plasma or ultraviolet/ozone treatment of the contact area[42,43] and molecular doping of the channel materials.[44] However, these methods require additional processes and can cause damage to the channel materials. Forming an "end-contacted" interface between metal and graphene was proposed as another way to reduce contact

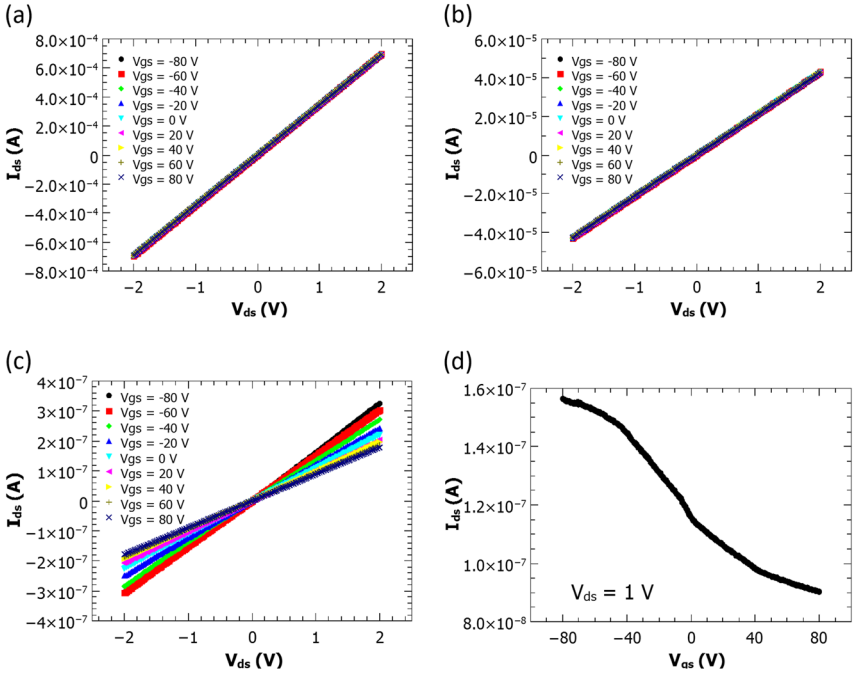

Fig. 4 Gate-dependent electrical measurements of $PtSe_2$ devices. Output characteristics (I_{ds} vs. V_{ds}) of $PtSe_2$ FET devices with $PtSe_2$ channels selenized from **a** 5 nm, **b** 2 nm, and **c** 0.5 nm thick Pt layers under various back-side gate biases (V_{gs}) from −80 to 80 V. **d** Transfer characteristics (I_{ds} vs. V_{gs} at $V_{ds} = 1$ V) of the $PtSe_2$ FET device with a $PtSe_2$ channel selenized from a 0.5 nm thick Pt layer

resistance,[45] wherein the end-contacted structure at the graphene–metal contacts facilitates chemical bonding between the graphene and the contact metal, enhancing the carrier injection at the contact area. Such an approach has previously been experimentally adopted for graphene-based devices, resulting in a significant improvement in the contact resistance.[46–48] Based on this principle, we expect that the edge-contacted structure shown here improves the carrier injection at the metal–$PtSe_2$ interface. Arrays of holes with a hole size of 200 × 200 nm were included on the contact area of the Pt channel design for EBL, generating channel patterns with empty holes on the contact areas by EBL, as presented in Fig. 5a and b. As the $PtSe_2$ is aligned parallel to the growth substrate these holes leave many edges exposed. The contact metal fills in these holes leading to the formation of edge contacts between the $PtSe_2$ channel and metal electrodes and increasing the total area of exposed channel edges at the contact region in the TLM structures. The $PtSe_2$ channels of all the devices were selenized from 0.5 nm thick Pt layers with a width of 2 µm, and three different types of hole array patterns (side 1-line, side 2-line, and center 2-line) were fabricated with Ni electrodes. The contact resistivity of the normal $PtSe_2$ TLM device without holes and the device with holes at the contact region were extracted and are compared in Fig. 5c. While there is no clear dependence of the contact resistivity on the number and location of hole arrays at the contact region, distributed between 2×10^5 and 6×10^5 Ω µm, all the devices with the hole patterns at the contact region exhibit 50–70% lower contact resistivity than the conventional device. In contrast, no significant difference in the sheet resistance was observed for all the $PtSe_2$ channel devices in Fig. 5d, indicating that the quality of the $PtSe_2$ channels is nearly constant for all devices.

In summary, we have investigated the electrical contact properties of $PtSe_2$ channels by the TLM method. Initial Pt layers with thicknesses of 0.5, 2, and 5 nm were selenized at low temperature using a TAC method, realizing robust $PtSe_2$ layers with different thicknesses. When comparing the contact resistivity values of the $PtSe_2$ TLM devices with two different contact metals, Ti and Ni, it was found that Ni forms a better electrical contact to the $PtSe_2$ channel. We also observed that the thinner $PtSe_2$ films have a higher contact resistivity and larger sheet resistance from the TLM measurements, implying that thinner $PtSe_2$ films become more semiconducting. In addition, the charge transport characteristics of $PtSe_2$ FETs were investigated. Only the device derived from the thinnest $PtSe_2$ layer (0.5 nm) showed a clear gate dependence with p-type conduction, which confirms the transition of $PtSe_2$ from semimetal to semiconductor with decreasing thickness. Furthermore, the effect of edge-contacted structures on the contact resistance was examined. Arrays of holes were patterned in $PtSe_2$ to increase the "edge-contacted" area of the layered $PtSe_2$ film at the metal interface. We found that the edge-contacted structures reduce the contact resistivity, which we attribute to enhancement of the carrier injection at the contacts. Though more comprehensive studies should be carried out in the future to fully understand the fundamentals of the electrical contact properties, our findings provide a quick insight into the realization of high-performance nanoelectronic devices based on layered $PtSe_2$.

METHODS

P-type silicon wafers (boron, 3×10^{15} cm^{-3}, <100>) with a thermally grown silicon dioxide (SiO_2, thickness: 290 nm) layer were prepared as substrates for the devices. An EBL system (Raith EBPG-5000Plus) was used to pattern the $PtSe_2$ channels and contacts. Initial Pt layers with different thicknesses were sputtered onto the substrates using a Gatan coating system (Gatan 682 PECS) with a deposition rate of <0.1 nm per second, followed by a lift-off process.

A TAC process was used to synthesize layered $PtSe_2$ thin films, as described in our previous work.[32,33] The sputtered Pt samples and the Se source (Sigma-Aldrich) were placed in two separate, independently controlled heating zones of a quartz tube furnace. The primary heating zone where the Pt samples were located was heated to 400 °C and the second heating zone for the Se source was heated to the melting point of Se (~220 °C) under Ar/H_2 (9:1) gas flow, leading to the formation of layered $PtSe_2$ thin films. Different metal electrodes of titanium/gold (Ti/Au,

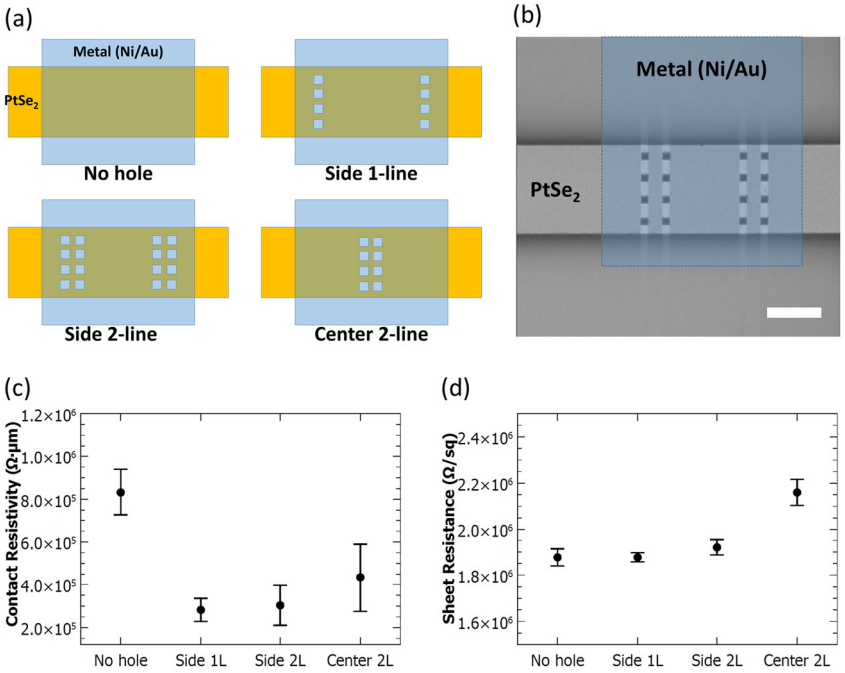

Fig. 5 Edge contacting of $PtSe_2$ TLM structures. **a** Schematic diagram of the metal (Ni)–$PtSe_2$ contact area with/without holes on the $PtSe_2$ channel. **b** SEM image of the $PtSe_2$ channel with 2-line holes at the side of the metal contact area before metal electrode deposition (scale bar, 1 μm). Extracted **c** contact resistivity and **d** sheet resistance values from the $PtSe_2$ TLM structures (0.5 nm of starting Pt thickness, 2 μm of channel width) with and without holes on the $PtSe_2$ channel at the metal-$PtSe_2$ contact area

20/150 nm) and nickel/gold (Ni/Au, 20/150 nm) were deposited to form TLM structures using an electron beam evaporation system (Plassys) without doing any additional process before evaporation, followed by a lift-off process.

Edge-contacted structures between the channel and metal electrodes were realized by including arrays of holes (a hole size of 200 × 200 nm) in the contact area of the channel design for EBL. The channel patterns, with hole arrays on the contact area, were generated by EBL, resulting in a contact area with empty holes on the channel after Pt deposition. These holes remain in the channel area post selenization. The metal electrodes were patterned by EBL after the selenization of the Pt. The contact metal was evaporated on to the contact region of the $PtSe_2$ channel with holes, without doing any additional processing at the contact area before evaporation. Further information on the formation of the edge contacts is given in Fig. S7 of the Supplementary Information.

Raman spectra were recorded with a Witec Alpha 300R confocal Raman microscope, using an excitation wavelength of 532 nm and a spectral grating with 1800 lines/mm. SEM images were taken using a JEOL SEM (JSM-IT300) at a high-vacuum mode with an accelerating voltage of 2 kV. Electrical measurements were performed at room temperature under ambient conditions using a Karl Süss probe station connected to a Keithley semiconductor analyzer (SCS4200).

Data availability

The data sets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

ACKNOWLEDGEMENTS

Support from an ERC grant (InteGraDe, 307311), the German Research Foundation (DFG, LE 2440/2-1), European Regional Funds (HEA2D), the French RENATECH network and Science Foundation Ireland (15/SIRG/3329; 15/IA/3131; 12/RC/2278) is gratefully acknowledged. V.P. would like to acknowledge Prof. Henri Happy for providing access to the cleanroom facilities and fruitful discussions.

AUTHOR CONTRIBUTIONS

C.Y. wrote the paper and designed the experiments. C.Y., V.P., E.P., and D.F. made devices. C.Y. and C.O.C. measured devices. C.O.C. performed AFM measurements. N.M. grew films and performed spectroscopy. M.C.L. and G.S.D. supervised the research. All authors contributed to the discussion of the results and improvement of the manuscript.

ADDITIONAL INFORMATION

Supplementary Information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-018-0051-9).

Competing interests: The authors declare no competing financial interests.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

REFERENCES

1. Novoselov, K. S. et al. Electric field effect in atomically thin carbon films. *Science* **306**, 666–669 (2004).
2. Chhowalla, M. et al. The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. *Nat. Chem.* **5**, 263–275 (2013).
3. Fiori, G. et al. Electronics based on two-dimensional materials. *Nat. Nanotechnol.* **9**, 768–779 (2014).
4. Rhoderick, E. H. Metal-semiconductor contacts. *IEE Proc. Solid State Electron Devices* **129**, 1–14 (1982).
5. Castro Neto, A. H., Guinea, F., Peres, N. M. R., Novoselov, K. S. & Geim, A. K. The electronic properties of graphene. *Rev. Mod. Phys.* **81**, 109–162 (2009).
6. Robinson, J. A. et al. Contacting graphene. *Appl. Phys. Lett.* **98**, 053103 (2011).
7. Malec, C. E., Elkus, B. & Davidović, D. Vacuum-annealed Cu contacts for graphene electronics. *Solid State Commun.* **151**, 1791–1793 (2011).
8. Zhong, H. et al. Realization of low contact resistance close to theoretical limit in graphene transistors. *Nano Res.* **8**, 1669–1679 (2015).
9. Gahoi, A. et al. Contact resistance study of various metal electrodes with CVD graphene. *Solid State Electron.* **125**, 234–239 (2016).
10. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **6**, 147–150 (2011).
11. Ovchinnikov, D., Allain, A., Huang, Y.-S., Dumcenco, D. & Kis, A. Electrical transport properties of single-layer WS_2. *ACS Nano* **8**, 8174–8181 (2014).
12. Lopez-Sanchez, O., Lembke, D., Kayci, M., Radenovic, A. & Kis, A. Ultrasensitive photodetectors based on monolayer MoS_2. *Nat. Nanotechnol.* **8**, 497–501 (2013).

13. Koppens, F. H. L. et al. Photodetectors based on graphene, other two-dimensional materials and hybrid systems. *Nat. Nanotechnol.* **9**, 780–793 (2014).
14. Yim, C. et al. Heterojunction hybrid devices from vapor phase grown MoS_2. *Sci. Rep.* **4**, 5458 (2014).
15. Lee, K., Gatensby, R., McEvoy, N., Hallam, T. & Duesberg, G. S. High performance sensors based on molybdenum disulfide thin films. *Adv. Mater.* **25**, 6699–6702 (2013).
16. Perkins, F. K. et al. Chemical vapor sensing with monolayer MoS_2. *Nano Lett.* **13**, 668–673 (2013).
17. Das, S., Chen, H.-Y., Penumatcha, A. V. & Appenzeller, J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett.* **13**, 100–105 (2013).
18. Allain, A., Kang, J., Banerjee, K. & Kis, A. Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* **14**, 1195–1205 (2015).
19. Chuang, H.-J. et al. Low-resistance 2D/2D Ohmic contacts: a universal approach to high-performance WSe_2, MoS_2, and $MoSe_2$ transistors. *Nano Lett.* **16**, 1896–1902 (2016).
20. Yoon, Y., Ganapathi, K. & Salahuddin, S. How good can monolayer MoS_2 transistors be? *Nano Lett.* **11**, 3768–3773 (2011).
21. Kwon, H.-J., Jang, J., Kim, S., Subramanian, V. & Grigoropoulos, C. P. Electrical characteristics of multilayer MoS_2 transistors at real operating temperatures with different ambient conditions. *Appl. Phys. Lett.* **105**, 152105 (2014).
22. Chen, B. et al. Environmental changes in $MoTe_2$ excitonic dynamics by defects-activated molecular interaction. *ACS Nano* **9**, 5326–5332 (2015).
23. Shimazu, Y., Tashiro, M., Sonobe, S. & Takahashi, M. Environmental effects on hysteresis of transfer characteristics in molybdenum disulfide field-effect transistors. *Sci. Rep.* **6**, 30084 (2016).
24. Lee, Y.-H. et al. Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition. *Adv. Mater.* **24**, 2320–2325 (2012).
25. Elías, A. L. et al. Controlled synthesis and transfer of large-area WS_2 sheets: from single layer to few layers. *ACS Nano* **7**, 5235–5242 (2013).
26. Gatensby, R. et al. Controlled synthesis of transition metal dichalcogenide thin films for electronic applications. *Appl. Surf. Sci.* **297**, 139–146 (2014).
27. Miró, P., Ghorbani-Asl, M. & Heine, T. Two dimensional materials beyond MoS_2: noble-transition-metal dichalcogenides. *Angew. Chem. Int. Ed.* **53**, 3015–3018 (2014).
28. Huang, Z., Zhang, W. & Zhang, W. Computational search for two-dimensional MX_2 semiconductors with possible high electron mobility at room temperature. *Materials* **9**, 716 (2016).
29. Guo, G. Y. & Liang, W. Y. The electronic structures of platinum dichalcogenides: PtS_2, $PtSe_2$ and $PtTe_2$. *J. Phys. C Solid State Phys.* **19**, 995 (1986).
30. Zhuang, H. L. & Hennig, R. G. Computational search for single-layer transition-metal dichalcogenide photocatalysts. *J. Phys. Chem. C* **117**, 20440–20445 (2013).
31. Wang, Y. et al. Monolayer $PtSe_2$, a new semiconducting transition-metal-dichalcogenide, epitaxially grown by direct selenization of Pt. *Nano Lett.* **15**, 4013–4018 (2015).
32. O'Brien, M. et al. Raman characterization of platinum diselenide thin films. *2D Mater.* **3**, 021004 (2016).
33. Yim, C. et al. High-performance hybrid electronic devices from layered $PtSe_2$ films grown at low temperature. *ACS Nano* **10**, 9550–9558 (2016).
34. Sedky, S., Witvrouw, A., Bender, H. & Baert, K. Experimental determination of the maximum post-process annealing temperature for standard CMOS wafers. *IEEE Trans. Electron Devices* **48**, 377–385 (2001).
35. Takeuchi, H., Wung, A., Sun, X., Howe, R. T. & King, T.-J. Thermal budget limits of quarter-micrometer foundry CMOS for post-processing MEMS devices. *IEEE Trans. Electron Devices* **52**, 2081–2086 (2005).
36. Lee, Y. H. D. & Lipson, M. Back-end deposited silicon photonics for monolithic integration on CMOS. *IEEE J. Sel. Top. Quantum Electron.* **19**, 8200207 (2013).
37. Jung, Y. et al. Metal seed layer thickness-induced transition from vertical to horizontal growth of MoS_2 and WS_2. *Nano Lett.* **14**, 6842–6849 (2014).
38. Lin, S. et al. Tunable active edge sites in $PtSe_2$ films towards hydrogen evolution reaction. *Nano Energy* **42**, 26–33 (2017).
39. Reeves, G. K. & Harrison, H. B. Obtaining the specific contact resistance from transmission line model measurements. *IEEE Electron Device Lett.* **3**, 111–113 (1982).
40. Wang, Z., Li, Q., Besenbacher, F. & Dong, M. Facile synthesis of single crystal $PtSe_2$ nanosheets for nanoscale electronics. *Adv. Mater.* **28**, 10224–10229 (2016).
41. Zhao, Y. et al. High-electron-mobility and air-stable 2D layered $PtSe_2$ FETs. *Adv. Mater.* **29**, 1604230 (2017).
42. Choi, M. S., Lee, S. H. & Yoo, W. J. Plasma treatments to improve metal contacts in graphene field effect transistor. *J. Appl. Phys.* **110**, 073305 (2011).
43. Li, W. et al. Ultraviolet/ozone treatment to reduce metal-graphene contact resistance. *Appl. Phys. Lett.* **102**, 183110 (2013).
44. Yang, L. et al. Chloride molecular doping technique on 2D materials: WS_2 and MoS_2. *Nano Lett.* **14**, 6275–6280 (2014).
45. Matsuda, Y., Deng, W.-Q. & Goddard, W. A. Contact resistance for "end-contacted" metal−graphene and metal−nanotube interfaces from quantum mechanics. *J. Phys. Chem. C* **114**, 17845–17850 (2010).
46. Smith, J. T., Franklin, A. D., Farmer, D. B. & Dimitrakopoulos, C. D. Reducing contact resistance in graphene devices through contact area patterning. *ACS Nano* **7**, 3661–3667 (2013).
47. Leong, W. S., Gong, H. & Thong, J. T. L. Low-contact-resistance graphene devices with nickel-etched-graphene contacts. *ACS Nano* **8**, 994–1001 (2014).
48. Passi, V. et al. Contact resistance study of "edge-contacted" metal-graphene interfaces. *46th European Solid-State Device Research Conference* (*ESSDERC*) 236–239. https://doi.org/10.1109/ESSDERC.2016.7599629 (IEEE, 2016).